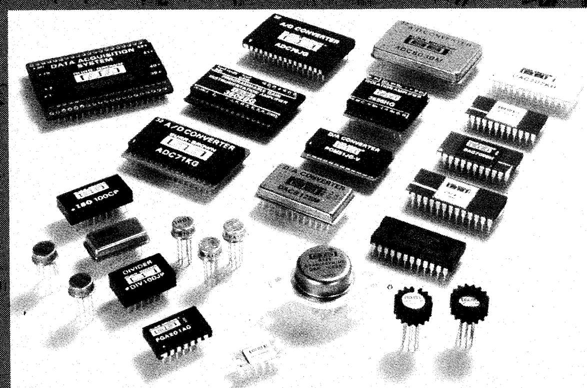

product data book supplement

BURR-BROWN®

BB

MODEL INDEX

BURR-BROWN®

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SUPPLEMENT TO PRODUCT DATA BOOK

LI-323

Printed in Holland July, 1985

INTRODUCTION

This supplement to the Burr-Brown Product Data Book contains product data sheets on new products that have been developed and introduced since the Data Book was published. Product lines such as Operational, Instrumentation, and Isolation Amplifiers, Analog-to-Digital and Digital-to-Analog Converters, Sample/Hold Amplifiers, Voltage-to-Frequency Converters, Military Products, Modular Power Supplies, Data Entry and Display Terminals, Microcomputer I/O Systems, Data Acquisition and Control Systems, and Personal Computer Instrumentation.

The Model Index list on the inside of the front cover refers to models and page numbers in both the Product Data Book and this supplement. Products in this supplement are set in bold type.

A Selection Guide on page iii contains a summary of performance characteristics of all products in both the Product Data Book and this supplement.

A complete list of all Burr-Brown offices and sales representatives can be found on the inside of the back cover. If you have questions on any of our products please contact the nearest Burr-Brown office or sales representative.

SELECTION GUIDE

DATA ENTRY AND DISPLAY TERMINALS

MICROTERMINAL

If your system's data entry/control/display requirements are sophisticated, but limited in volume, you don't need to buy big, expensive and fragile CRTs or printing terminals to do the job efficiently.

"Microterminal" is uniquely flexible in application versatility and is designed expressly to fill the human interface demands of widely dispersed control and communications networks—in machine and process control, energy management systems, inventory control and factory floor data collection and information processing systems. Microterminal, because of its interface flexibility, appearance, size, durability and easy installation, functions equally well as consoles and control centers for instruments and small systems. It also performs as I/O terminals in diagnostic applications.

Tough, water-resistant front panel protects LED displays and indicators as well as keyboard. Tactile feedback confirms operator entry.

Buffered data features reduce on-line input/output time with the CPU and improve accuracy of operator inputs. And, because of its design simplicity, the Microterminal concept doesn't require special operator skills or training. Depressing a single function key initiates complex preprogrammed action by the CPU. These functions are defined in your CPU's software.

Microterminal offers very compact design and simple mounting on any flat surface, making it quickly adaptable to new or existing applications. It measures only 216mm × 114mm × 15mm (8.5" × 4.5" × 0.6"). When ordered in OEM quantities the front panel can contain your corporate or system logo.

Products in this *Supplement* are indicated by a ● next to model numbers; others are in the *Product Data Book*.

MICROTERMINALS

Description	Model Number	Display Type[1]	Number of Characters in Display	Internal Buffer Size (I/O)	Keypad Type[1]	Data Transmission[2] (Nonpolled Mode)	Communications Interface[3]	Multidrop Capacity	Function Keys[4]	Baud Rate	Digital Inputs	Digital Outputs w/LEDs	User EPROM	8-Bit Port: Output w/LEDs	8-Bit Port: Bidirectional	Power Supply Required	Page
Low Cost	TM25-300-XX	Hex	8	8	Hex & Num	Block	RS-232 & C/L	8	7	300	No	No	No	No	No	15VDC	13-5
	TM27	Hex	8	8	Hex	[5]	RS-232 or RS-422	63	6	300 to 4800[6]	3	5	No	No	No	8-12VDC voltage regulator	13-5
General	TM70	A/N	12	36	A/N	Echo	RS-232 & C/L	15	8	300 & 1200	No	2	No	No	No	5VDC	13-4
	TM76	A/N	12	36	Num[7]	Echo	RS-232 & C/L	15	8	300 & 1200	No	2	No	No	No	5VDC	13-4
	TM71	A/N	16	80 + 80	A/N	Block	RS-232 & C/L or RS-422	15	14	110 to 19,200	No	2	Yes	No	No	5VDC	13-2
	TM77	A/N	16	80 + 80	Num	Block	same as TM71	15	14	110 to 19,200	No	2	Yes	No	No	5VDC	13-2
Digital I/O	TM71-I/O	A/N	16	80 + 80	A/N	Block	same as TM71	15	14	110 to 19,200	No[8]	2[8]	Yes	Yes	Yes	5VDC	13-3
	TM77-I/O	A/N	16	80 + 80	Num	Block	same as TM71	15	14	110 to 19,200	No[8]	2[8]	Yes	Yes	Yes	5VDC	13-3
MIL Spec	TM71M	A/N	16	80 + 80	A/N	Block	RS-232	NA	14	110 to 9600	No	2	No	No	No	5VDC	13-3
Bar Code Reader [9] [10] [11]	TM71B -XX	A/N	16	80 + 80	A/N	Block	RS-232 or C/L or RS-422	63	16	110 to 19,200	No	2	No	No	Yes	5VDC or 20-30VDC + 15-28VAC	13-3
	TM77B -XX	A/N	16	80 + 80	Num	Block	same as TM71B	63	16	110 to 19,200	No	2	No	No	Yes	same as TM71B	13-3
	● TM200	A/N	40	80 + 80	Num	Block	same as TM71B	63	16	110 to 19,200	No	10	Yes	Yes	No[12]	5VDC	192
Mag Stripe Reader [9] [13]	TM71MS -XX	A/N	16	80 + 80	A/N	Block	same as TM71B	63	16	110 to 19,200	No	2	No	No	Yes	same as TM71B	13-3
	TM77MS -XX	A/N	16	80 + 80	Num	Block	same as TM71B	63	16	110 to 19,200	No	2	No	No	Yes	same as TM71B	13-3

NOTES: (1) A/N = alphanumeric, Hex = hexadecimal, Num = numeric. (2) In echo mode each character is sent upon key press. In block mode the entire line is sent when Enter key is pressed; no echo is needed. (3) C/L = current loop with optical isolation. For TM71, 77, 71-I/O, and 77-I/O add "-21" for RS-422. No suffix for RS-232 and C/L. (4) On all but TM25, the function keys can be programmed. (5) TM27 with RS-422 interface operates in polled mode only. Add "-12" for RS-232 interface that operates in nonpolled mode. (6) 300, 1200, 2400, 4800. (7) TM71K and TM77K models have full-travel keyswitch-type keyboards. (8) TM71-I/O and TM77-I/O have 8-bit I/O ports. (9) Re: two-digit suffix "-xx". The first digit designates communications interface: 1 = RS-232, 2 = RS-422, 3 = C/L. The second digit is for power supply: 1 = 5VDC, 2 = 20-30VDC or 15-28VAC. (10) Bar code readers include industrial bar code wand. Five major symbologies are switch-selectable. (11) Optional with TM200. (12) Centronics printer port. (13) Magnetic stripe readers include slot type and reader. ABA Track 2 code.

DATA CONVERSION
DATA ACQUISITION

Products in this *Supplement* are indicated by a ● next to model numbers; others are in the *Product Data Book*.

Designing, assembling and testing high performance data converters and data acquisition systems—including models that have become industry standards—allows us to offer you complete, practical, easily applied solutions to difficult problems.

We have established a full line of interrelated digital and analog products whose functions are complementary and thereby give you one-stop shopping—Burr-Brown! We simplify your design task by applying powerful analog and digital expertise—employing high level integration to create complete products that don't require extensive external components. Our application of microcomputer technology and compatibility makes it much easier for you to interface our products. Even engineers with limited analog experience design-in these versatile circuits with confidence.

ANALOG-TO-DIGITAL CONVERTERS

These designs will meet your most demanding applications. We employ monolithic technology to support the high performance offered. The successive-approximation design approach produces ADC's that give 12-bit conversion in as low as 1.5µsec, and low cost 12-bit designs with microprocessor interface that convert in 15µsec. High resolution 16-bit converters in small DIL packages give conversions to 0.003% accuracy in 15µsec at a very reasonable price. Harsh temperature environments can be handled as well with 12-bit converters that operate to +200°C.

ANALOG-TO-DIGITAL CONVERTERS

Description	Model[1]	Resolution (Bits)	Conversion Time, max (µsec)	Linearity Error, max (% of FSR)	Gain Drift, max (ppm/°C)	Zero Drift, max (ppm FSR/°C)	Input Ranges (V)	Temp Range[2]	Package	Page
Micro-Processor Interface, Low Cost, Compatible	●ADC574AJH	12	25	±0.024	±45[3]	±10U, ±10B[4]		Com	24-pin DIP	9
	●ADC574AKH	12	25	±0.012	±25[3]	±5U, ±5B[4]	±5, ±10,	Com	Hermetic	9
	●ADC574ASH	12	25	±0.024	±50[3]	±5U, ±10B[4]	+10, +20	MIL	Ceramic	9
	●ADC574ATH	12	25	±0.012	±25[3]	±2.5U, ±5B[4]		MIL		9
	●ADC674AJH	12	15	±0.024	±45[3]	±10U, ±10B[4]		Com	24-pin DIP	18
	●ADC674AKH	12	15	±0.012	±25[3]	±5U, ±5B[4]	±5, ±10,	Com	Hermetic	18
	●ADC674ASH	12	15	±0.024	±50[3]	±5U, ±10B[4]	+10, +20	MIL	Ceramic	18
	●ADC674ATH	12	15	±0.012	±25[3]	±2.5U, ±5B[4]		MIL		18
Low Cost, ADC80 Compatible	●ADC80H-AH-12, (Q)	12	25	±0.012	±30	±3U typ, ±15B[5]	±2.5, ±5, ±10, +5, +10	Ind	32-pin DIP Hermetic Ceramic	1
Standard ADC80	ADC80AG-10	12	21	±0.048	±30	±3U typ, ±15B[5]	±2.5, ±5,	Ind	32-pin DIP	5-54
	ADC80AG-12	12	25	±0.012	±30	±3U typ, ±15B[5]	±10, +5, +10	Ind	Ceramic	5-54
High Speed Standard	ADC82AG	8	2.8	±0.2	±40	±20U typ, ±35B[5]	±2.5, ±5, ±10, +5, +10, +20	Ind	24-pin DIP Ceramic	5-62
	ADC82AM, (Q)	8	2.8	±0.2	±40	±20U typ, ±35B[5]	±2.5, ±5, ±10, +5, +10, +20	Ind	24-pin DIP Hermetic Metal	5-62
	ADC84KG-10	12	6	±0.048	±40	±3U, ±15B typ[5]	±2.5, ±5, ±10,	Com	32-pin DIP	5-70
	ADC84KG-12	12	10	±0.012	±30	±3U, ±15B typ[5]	+5, +10	Com	Ceramic	5-70
High Speed, Low Drift Standard	ADC85C-12, (Q)	12	10	±0.012	±25	±3U, ±12B typ[5]	±2.5, ±5, ±10,	Com	32-pin DIP	5-70
	ADC85-10	10	6	±0.048	±20	±3U, ±10B typ[5]	+5, +10	Ind	Hermetic	5-70
	ADC85-12, (Q)	12	10	±0.012	±15	±3U, ±7B typ[5]		Ind	Metal	5-70
Very High Speed	ADC803BM, (Q)	12	1.5	±0.020	±30	±7U, ±10B[5]	±5, ±10, −10	Ind	32-pin DIP	5-86
	ADC803CM, (Q)	12	1.5	±0.012	±30	±7U, ±10B[5]	±5, ±10, −10	Ind	Hermetic	5-86
	ADC803SM, (Q)	12	1.5	±0.012	±30	±7U, ±10B[5]	±5, ±10, −10	MIL	Metal	5-86
Serial Output Small Package	●ADC804BH, (Q)	12	17	±0.012	±30	±3U typ, ±15B[5]	±2.5, ±5, ±10, +5, +10	Ind	32-pin DIP Hermetic	27
	●ADC804SH, (Q)	12	17	±0.012	±30	±3U typ, ±15B[5]	±2.5, ±5, ±10, +5, +10	Ind	Ceramic	27
High Resolution, High Accuracy	ADC73J	16	170	±0.0015	±10	±2U, ±5B[5]	±5, ±10,	Com	Module	5-35
	ADC73K	16	170	±0.00075	±10	±2U, ±5B[5]	+10, +20	Com	Module	5-35
	ADC731J	16	170	±0.0015	±10	±2U, ±5B[5]	±5, ±10,	Com	Module	5-35
	ADC731K	16	170	±0.00075	±10	±2U, ±5B[5]	+10, +20	Com	Module	5-35
High Resolution, Industry Standard Pinout	ADC71JG	16	50	±0.006	±15	±4U, ±10B[5]	±2.5, ±5, ±10,	Com	32-pin DIP	5-19
	ADC71KG	16	50	±0.003	±15	±4U, ±10B[5]	+5, +10, +20	Com	Ceramic	5-19
	ADC72AM	16	50	±0.006	±15	±2U, ±10B[5]		Ind	32-pin DIP	5-27
	ADC72BM	16	50	±0.003	±15	±2U, ±10B[5]	±2.5, ±5, ±10,	Ind	Hermetic	5-27
	ADC72JM	16	50	±0.006	±20	±4U, ±10B[5]	+5, +10, +20	Com	Metal	5-27
	ADC72KM	16	50	±0.003	±20	±4U, ±10B[5]		Com		5-27
	ADC76JG	16	15	±0.006	±15	±4U, ±10B[5]	±2.5, ±5, ±10	Com	32-pin DIP	5-46
	ADC76KG	16	15	±0.003	±15	±4U, ±10B[5]	±2.5, ±5, ±10	Com	Ceramic	5-46
High Speed	ADC60-12	12	3.5	±0.0244	±15[6]	—	±2.5, ±5, ±10, +5, +10, +20	Com	Module	5-13
Very-Wide Temperature Range	ADC10HT	12	50	±0.012	±35	±2U, ±35B typ[5]	±5, ±10	−55°C to	28-pin	5-3
	ADC10HT-1	12	50	±0.048	±100	±10U, ±100B typ[5]	±5, ±10	+200°C	Hermetic Ceramic	5-3
MIL-STD-883	See Military Products, page xxi									

NOTES: (1) "Q" indicates product available with screening for enhanced reliability. See High Reliability Screening, page xxi. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) Full Scale Drift. (4) U = Unipolar Zero Drift, B = Bipolar Offset Drift. For ADC574A and ADC674A only, Bipolar Offset is defined at Bipolar Zero; that is, at 0V − 1/2LSB, rather than the more conventional definition at − Full Scale + 1/2LSB. (5) U = Unipolar Zero Drift, B = Bipolar Offset Drift. 6) Total Drift: Gain, Offset, and Linearity; ppm of FSR/°C.

PCM ANALOG-TO-DIGITAL CONVERTERS FOR AUDIO

Description	Model	Resolution (Bits)	Total Harmonic Distortion (max)	Conversion Time (max)	Input Range (V)	Temp Range[1]	Dynamic Range	Page
PCM Audio A/D Converter[3]	PCM75KG	16	0.02% at −15dB	17µsec[2]	±2.5, ±5, ±10	Com	90dB	5-98
	PCM75JG	14[4]	0.05% at −15dB	15µsec[2]	±2.5, ±5, ±10	Com	90dB	5-98

NOTES: (1) Com = 0 to +70°C. (2) Can be reduced to 8µsec. (3) Internal 16-bit DAC available to user. (4) Can be operated at 16 bits.

DIGITAL-TO-ANALOG CONVERTERS

Our DAC80 is a standard in 12-bit performance. DAC800—a monolithic IC—continues this proven product offering the same pinout, functions and improved performance at a lower price. DAC811, a complete 12-bit D/A, provides microprocessor interface.

16-bit designs from Burr-Brown have also set industry standards: DAC71 is the industry standard low-cost 16-bit D/A; DAC701 and DAC703 are complete 16-bit monolithics with op amps and voltage reference on the chip. DAC705 through DAC709 provide several microprocessor interface options including serial data for 16-bit D/A converters

ECL-compatible DAC63 employs new technology and higher levels of integration to achieve 40nsec (typ to ±0.012) settling time and excellent temperature and time stability at low cost.

DIGITAL-TO-ANALOG CONVERTERS

Description	Model[1]	Resolution (Bits)	Linearity Error, max (% of FSR)	Gain Drift, max[2] (ppm/°C)	Zero Drift, max (ppm FSR/°C)	Output Ranges	Settling Time max[3]	Temp Range[4]	Package	Page
High Resolution Monolithic Industry Standard DAC 70, 71, 72 Compatible	DAC700KH	16	±0.003	±25	±5	0 to −1mA	1μsec	Com	24-pin DIP	6-107
	DAC700BH, (/QM)	16	±0.003	±15	±3	0 to −1mA	1μsec	Ind	Hermetic	6-107
	DAC700SH, (/QM)	16	±0.003	±15	±3	0 to −1mA	1μsec	MIL	Ceramic	6-107
	DAC700BL, (/QM)	16	±0.003	±15	±3	0 to −1mA	1μsec	Ind	28-term. LCC	6-107
	DAC700SL, (/QM)	16	±0.003	±15	±3	0 to −1mA	1μsec	MIL	Hermetic,	6-107
									Ceramic	
	DAC701KH	16	±0.003	±25	±5	0 to +10V	8μsec	Com	24-pin DIP	6-107
	DAC701BH, (/QM)	16	±0.003	±15	±3	0 to +10V	8μsec	Ind	Hermetic	6-107
	DAC701SH, (/QM)	16	±0.003	±15	±3	0 to +10V	8μsec	MIL	Ceramic	6-107
	DAC701BL, (/QM)	16	±0.003	±15	±3	0 to +10V	8μsec	Ind	28-term. LCC	6-107
	DAC701SL, (/QM)	16	±0.003	±15	±3	0 to +10V	8μsec	MIL	Hermetic	6-107
									Ceramic	
	DAC702JP	16	±0.006	±30	±15	±1mA	350nsec, typ	Com	24-pin DIP	6-107
	DAC702KP★	16	±0.003	±25	±12	±1mA	1μsec	Com	Plastic	6-107
	DAC702KH	16	±0.003	±25	±12	±1mA	1μsec	Com	24-pin DIP	6-107
	DAC702BH, (/QM)	16	±0.003	±15	±10	±1mA	1μsec	Ind	Hermetic	6-107
	DAC702SH, (/QM)	16	±0.003	±15	±10	±1mA	1μsec	MIL	Ceramic	6-107
	DAC702BL, (/QM)	16	±0.003	±15	±10	±1mA	1μsec	Ind	28-term. LCC	6-107
	DAC702SL, (/QM)	16	±0.003	±15	±10	±1mA	1μsec	MIL	Hermetic,	6-107
									Ceramic	
	DAC703JP	16	±0.006	±30	±15	±10V	4μsec, typ	Com	24-pin DIP	6-107
	DAC703KP★	16	±0.003	±25	±12	±10V	8μsec	Com	Plastic	6-107
	DAC703KH	16	±0.003	±25	±12	±10V	8μsec	Com	24-pin DIP	6-107
	DAC703BH, (/QM)	16	±0.003	±15	±10	±10V	8μsec	Ind	Hermetic	6-107
	DAC703SH, (/QM)	16	±0.003	±15	±10	±10V	8μsec	MIL	Ceramic	6-107
	DAC703BL, (/QM)	16	±0.003	±15	±10	±10V	8μsec	Ind	28-term. LCC	6-107
	DAC703SL, (/QM)	16	±0.003	±15	±10	±10V	8μsec	MIL	Hermetic,	6-107
									Ceramic	
High Resolution Micro-Processor Interface, 16-bit port	●DAC705KH	16	±0.003	±25	±12	±5V	8μsec	Com	28-pin DIP	35
	●DAC705BH, (/QM)	16	±0.003	±15	±10	±5V	8μsec	Ind	Hermetic	35
	●DAC705SH, (/QM)	16	±0.003	±15	±10	±5V	8μsec	MIL	Ceramic	35
	●DAC706KH	16	±0.003	±25	±12	±1mA	350nsec, typ	Com	28-pin DIP	35
	●DAC706BH, (/QM)	16	±0.003	±15	±10	±1mA	350nsec, typ	Ind	Hermetic	35
	●DAC706SH, (/QM)	16	±0.003	±15	±10	±1mA	350nsec, typ	MIL	Ceramic	35
	●DAC707KH	16	±0.003	±25	±12	±10V	8μsec	Com	28-pin DIP	35
	●DAC707BH, (/QM)	16	±0.003	±15	±10	±10V	8μsec	Ind	Hermetic	35
	●DAC707SH, (/QM)	16	±0.003	±15	±10	±10V	8μsec	MIL	Ceramic	35
High Resolution Micro-Processor Interface, 8-bit Port	●DAC708KH	16	±0.003	±25	±5U, ±12B[5]	±1, −2mA	350nsec, typ	Com	24-pin DIP	35
	●DAC708BH, (/QM)	16	±0.003	±15	±3U, ±10B[5]	±1, −2mA	350nsec, typ	Ind	Hermetic	35
	●DAC708SH, (/QM)	16	±0.003	±15	±3U, ±10B[5]	±1, −2mA	350nsec, typ	MIL	Ceramic	35
	●DAC709KH	16	±0.003	±25	±5U, ±12B[5]	±5, ±10,	8μsec	Com	24-pin DIP	35
	●DAC709BH, (/QM)	16	±0.003	±15	±3U, ±10B[5]	+10V	8μsec	Ind	Hermetic	35
	●DAC709SH, (/QM)	16	±0.003	±15	±3U, ±10B[5]		8μsec	MIL	Ceramic	35
Motor Control Monolithic	●DAC710KH	16	±0.0015	±50		±1mA	350nsec, typ	Com	24-pin DIP	45
	●DAC711KH	16	DLE around	±50		±10V	8μsec	Com	Hermetic	45
			BP Zero						Ceramic	
12-Bit Monolithic, Low Cost, Industry Standard Pinout	DAC800P-CBI-I	12	±0.012	±30	±3U, ±15B[6]	±1, −2mA	300nsec, typ	Com	24-pin DIP	6-126
	DAC800P-CBI-V	12	±0.012	±30	±3U, ±15B[6]	±2.5, ±5, ±10,	5μsec	Com	Plastic	6-126
						+5, +10V				
	DAC800-CBI-I	12	±0.012	±30	±3U, ±15B[6]	±1, −2mA	300nsec, typ	Com	24-pin DIP	6-126
	DAC800-CBI-V	12	±0.012	±30	±3U, ±15B[6]	±2.5, ±5, ±10,	5μsec	Com	Hermetic	6-126
						+5, +10V			Ceramic	
	DAC850-CBI-I, (/QM)	12	±0.012	±20	±3U, ±10B[6]	±1, −2mA	300nsec, typ	Ind	24-pin DIP	6-147
	DAC850-CBI-V, (/QM)	12	±0.012	±20	±3U, ±10B[6]	±2.5, ±5, ±10,	5μsec	Ind	Hermetic	6-147
						+5, +10V			Ceramic	
	DAC850BL-I, (/QM)	12	±0.012	±20	±3U, ±10B[6]	±1, −2mA	300nsec, typ	Ind	28-term. LCC	6-147
	DAC850BL-V, (/QM)	12	±0.012	±20	±3U, ±10B[6]	±2.5, ±5, ±10,	5μsec	Ind	Hermetic	6-147
						+5, +10V			Ceramic	
	DAC851-CBI-I, (/QM)	12	±0.012	±25	±3U, ±15B[6]	±1, −2mA	300nsec, typ	MIL	24-pin DIP	6-147
	DAC851-CBI-V, (/QM)	12	±0.012	±25	±3U, ±15B[6]	±2.5, ±5, ±10,	5μsec	MIL	Hermetic	6-147
						+5, +10V			Ceramic	
	DAC851SL-I, (/QM)	12	±0.012	±25	±3U, ±15B[6]	±1, −2mA	300nsec, typ	MIL	28-term. LCC	6-147
	DAC851SL-V, (/QM)	12	±0.012	±25	±3U, ±15B[6]	±2.5, ±5, ±10,	5μsec	MIL	Hermetic	6-147
						+5, +10V			Ceramic	
12-Bit Monolithic Micro-Processor Interface, Low Cost	DAC811JP★	12	±0.012	±30	±10U, ±10B[5]	±5, ±10, +10	4μsec	Com	28-pin DIP	6-133
	DAC811KP	12	±0.006	±20	±7U, ±7B[5]	±5, ±10, +10	4μsec	Com	Plastic	6-133
	DAC811AH, (/QM)	12	±0.012	±30	±10U, ±10B[5]	±5, ±10, +10	4μsec	Ind	28-pin DIP	6-133
	DAC811BH, (/QM)	12	±0.006	±20	±7U, ±7B[5]	±5, ±10, +10	4μsec	Ind	Hermetic	6-133
	DAC811RH, (/QM)	12	±0.012	±30	±10U, ±10B[5]	±5, ±10, +10	4μsec	MIL	Ceramic	6-133
	DAC811SH, (/QM)	12	±0.006	±20	±7U, ±7B[5]	±5, ±10, +10	4μsec	MIL		6-133
	DAC811AL, (/QM)	12	±0.012	±30	±10U, ±10B[5]	±5, ±10, +10	4μsec	Ind	28-term. LCC	6-133
	DAC811BL, (/QM)	12	±0.006	±20	±7U, ±7B[5]	±5, ±10, +10	4μsec	Ind	Hermetic	6-133
	DAC811RL, (/QM)	12	±0.012	±30	±10U, ±10B[5]	±5, ±10, +10	4μsec	MIL	Ceramic	6-133
	DAC811SL, (/QM)	12	±0.006	±20	±7U, ±7B[5]	±5, ±10, +10	4μsec	MIL		6-133

DIGITAL-TO-ANALOG CONVERTERS (continued)										
Description	Model[1]	Resolution (Bits)	Linearity Error, max (% of FSR)	Gain Drift, max[2] (ppm/°C)	Zero Drift, max (ppm FSR/°C)	Output Ranges	Settling Time max[3]	Temp Range[4]	Package	Page
Standard DAC80	DAC80-CBI-I[7]	12	±0.012	±30	±3U, ±15B[6]	±1, −2mA	300nsec, typ	Ind		6-77
	DAC80-CBI-V	12	±0.012	±30	±3U, ±15B[6]	±2.5, ±5, ±10, +5, +10V	5µsec, typ	Ind	24-pin DIP Ceramic	6-77
	DAC80-CCD-I	3 Digit	±0.025	±30	±3U, ±15B[6]	0 to −2mA	300nsec, typ	Ind		6-77
	DAC80-CCD-V	3 Digit	±0.025	±30	±3U, ±15B[6]	0 to +10V	5µsec, typ,	Ind		6-77
Standard DAC85	DAC85-CBI-I, (Q)	12	±0.012	±20	±1U, ±10B[6]	±1, −2mA	300nsec, typ	Ind	24-pin DIP	6-94
	DAC85-CBI-V, (Q)	12	±0.012	±20	±1U, ±10B[6]	±2.5, ±5, ±10,	5µsec, typ	Ind	Hermetic	6-94
	DAC85C-CBI-V, (Q)	12	±0.012	±20	±1U, ±10B[6]	+5, +10V	5µsec, typ	Com	Metal	6-94
Low Drift	DAC85LD-CBI-V, (Q)	12	±0.012	±10	±1U, ±5B[6]	±2.5, ±5, ±10, +5, +10V	5µsec, typ	Ind	24-pin DIP Hermetic Metal	6-94
High Resolution	DAC70-CSB-I	16	±.003	±7	±1U, ±5B[6]	0 to −2mA	50µsec, typ	Ind	24-pin DIP	6-26
	DAC70-COB-I	16	±.003	±7	±1U, ±5B[6]	±1mA	50µsec, typ	Ind	Hermetic Metal	6-26
High Resolution Standard DAC71	DAC71-CSB-I	16	±.003	±45	±1	0 to −2mA	1µsec	Com		6-34
	DAC71-COB-I	16	±.003	±45	±40	±1mA	1µsec	Com		6-34
	DAC71-CCD-I	4 Digit	±0.005	±45	±1	0 to −2mA	1µsec	Com	24-pin DIP	6-34
	DAC71-CSB-V	16	±.003	±15	±2	0 to +10V	10µsec	Com	Ceramic	6-34
	DAC71-COB-V	16	±.003	±15	±10	±10V	10µsec	Com		6-34
	DAC71-CCD-V	4 Digit	±0.005	±15	±1	0 to +10V	10µsec	Com		6-34
High Resolution Standard DAC72	DAC72-CSB-I	16	±.003	±35	±1	0 to −2mA	1µsec	Ind	24-pin DIP	6-44
	DAC72-COB-I	16	±.003	±35	±35	±1mA	1µsec	Ind	Hermetic	6-44
	DAC72-CSB-V	16	±.003	±7/±15[8]	±2	0 to +10V	10µsec	Ind	Metal	6-44
	DAC72-COB-V	16	±.003	±7/±15[8]	±8	±10V	10µsec	Ind		6-44
High Resolution High Accuracy	DAC73J	16	±0.0015	±10[9]	±2U, ±5B[9]	±1, −2mA	50µsec, typ	Com	Modular	6-54
	DAC73K	16	±0.00075	±10[9]	±2U, ±5B[9]	±2.5, ±5, ±10,	50µsec, typ	Com	Modular	6-54
	DAC736J	16	±0.0015	±10[9]	±2U, ±5B[9]	+5, +10V	50µsec, typ	Com	Modular	6-54
	DAC736K	16	±0.00075	±10[9]	±2U, ±5B[9]		50µsec, typ	Com	Modular	6-54
Ultra-High Speed, ECL Input	DAC63BG	12	±0.012	±40	±1U, ±15B[6]	±5, −10mA	55nsec[10]	Ind	24-pin DIP	6-18
	DAC63CG	12	±0.012	±30	±0.6U, ±10B[6]	±5, −10mA	50nsec[10]	Ind	Ceramic	6-18
	DAC63BM	12	±0.012	±40	±1U, ±15B[6]	±5, −10mA	55nsec[10]	Ind	24-pin DIP	6-18
	DAC63CM	12	±0.012	±30	±0.6U, ±10B[6]	±5, −10mA	50nsec[10]	Ind	Hermetic	6-18
	DAC63SM	12	±0.012	±40	±1U, ±15B[6]	±5, −10mA	55nsec[10]	MIL	Metal	6-18
	DAC63TM	12	±0.012	±30	±0.6U, ±10B[6]	±5, −10mA	50nsec[10]	MIL		6-18
Ultra-High Speed, TTL Input	DAC812BM	12	±0.012	±40	±1U, ±15B[6]	±5, −10mA	65nsec	Ind	24-pin DIP	6-141
	DAC812CM	12	±0.012	±20	±0.5U, ±10B[6]	±5, −10mA	80nsec	Ind	Hermetic	6-141
Very-High Speed	DAC60-10	12	±0.048	±15[11]		±2.5, −5mA	40nsec, typ	Com	Module	6-13
	DAC60-12	12	±0.012	±15[11]		±2.5, −5mA	150nsec, typ	Com	Module	6-13
8-bit Monolithic	DAC90BG, (Q)	8	±0.2	±50, typ.	±1U,	±1, −2mA	200nsec, typ	Ind	16-pin DIP	6-102
	DAC90SG, (Q)	8	±0.2	±50, typ.	±50B typ[6]	±1, −2mA	200nsec, typ	MIL	Hermetic Ceramic	6-102
	DAC82KG	8	±0.16	±50	±1U typ, ±20B[6]	±2.5, ±5, ±10, +5, +10V, ±0.8, −1.6mA	2.5µsec, typ	Com	18-pin DIP Ceramic	6-87
Very-Wide Temperature Range	DAC10HT	12	±0.012	±10	±2U, ±10B[6]	±2.5, ±5, ±10,	200nsec, typ	−55°C	24-pin DIP	6-5
	DAC10HT-1	12	±0.048	±25	±5U, ±25B[6]	+5, +10V	200nsec, typ	to 200°C	Hermetic Ceramic	6-5
Military MIL-STD-883	See Military Products, page xxi									

★Die available. See page 223.

NOTES: (1) "Q" or "/QM" indicates product is also available with screening for increased reliability. See High Reliability Screening, page xxi. (2) This spec applies to current output D/A converters when used with an external output amplifier and also using the internal feedback resistor of the D/A converter. (3) For 12-bit converters: settling to within ±0.012% of FSR (±1/2LSB). For 16-bit converters: settling to within ±0.003% of FSR. (4) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (5) U = Unipolar Zero; B = Bipolar Zero. (6) U = Unipolar Zero; B = Bipolar Offset. (7) DAC80Z models are available that operate from ±12V power supplies. (8) Hot/cold. (9) Exclusive of Reference Drift. (10) Settling time to within±1LSB. (11) Total: Gain, Offset, and Linearity drift. With external op amp and using internal feedback resistor.

DIGITAL-TO-ANALOG CONVERTER DICE										
Description	Model	Resolution (Bits)	Linearity Error, max (% of FSR)	Gain Drift, max (ppm/°C)	Zero Drift, max (ppm FSR/°C)	Output Ranges	Settling Time max[1]	Temp Range[2]	Package	Page
High Resolution	● DAC7700KD	16	±0.003	±25	±12	0 to −2mA, ±1mA	1µsec	Com	Die	230
	● DAC7701KD	16	±0.003	±25	±12	0 to 10V, ±5V, ±10V	4µsec	Com	Die	235
12-Bit Micro-Processor Interface	● DAC811JD	12	±0.012	±30	±10	0 to 10V, ±5V, ±10V	4µsec	Com	Die	225

NOTES: (1) Settling to within ±0.003% of FSR. (2) Com = 0°C to +70°C.

PCM DIGITAL-TO-ANALOG CONVERTERS FOR AUDIO									
Description	Model	Resolution (Bits)	Total Harmonic Distortion (max)	Settling Time, FSR to ±1/2LSB, (typ)	Output Range	Temp Range (1)	Dynamic Range	Package	Page
PCM Audio D/A Converter	PCM52JG-V	16	0.002% at FS	3μsec	±5V	Com	96dB	24-pin DIP Ceramic	6-162
	PCM53JG-I	16	0.002% at FS	350nsec	±1mA	Com	96dB	24-pin DIP Ceramic	6-162
	PCM53JG-V	16	0.002% at FS	3μsec	710V	Com	96dB		6-162
	PCM53JP-I	16	0.004% at FS	350nsec	±1mA	Com	96dB	24-pin DIP Plastic	6-162
	PCM53KP-I	16	0.0025% at FS	350nsec	±1mA	Com	96dB		6-162
	PCM53JP-V	16	0.004% at FS	3μsec	±10V	Com	96dB		6-162
	PCM53KP-V	16	0.0025% at FS	3μsec	±10V	Com	96dB		6-162

NOTE: (1) Com = 0 to +70°C.

SELF-CALIBRATING, HIGH PRECISION D/A CONVERTER

This unique 16-bit D/A converter is actually an instrument. The heart is a highly accurate 16-bit D/A converter with a heated, temperature compensated precision reference. Wrapped around this D/A are microcomputer-controlled measurement and calibration circuits that automatically null out gain, offset and linearity errors caused by shifts with time and temperature when initiated by one negative-going TTL-pulse provided by the user.

SELF-CALIBRATING D/A CONVERTER							
Description	Model	Resolution	Total Error +15 to +45°C	Output Ranges	Calibration Time	Package	Page
Precision, High-Resolution	DAC74	16 bits	±0.0015%, max	0 to +10V ±10V	2.5sec, initiated by 15μsec negative TTL pulse	7" x 5" x 0.600" metal	6-62

VOLTAGE-TO-FREQUENCY CONVERTERS

VFC's provide a simple low cost way of converting analog signals into digital form. They produce a pulse train with a repetition rate proportional to the amplitude of the analog input. The combination of accuracy, linearity, and low temperature drift make these units some of the best available. Simple low cost isolation is obtained when a VFC is used together with a DC/DC converter and a single optical coupler.

V/F CONVERTERS								
Description	Model(1)	Frequency Range (kHz)	V_{IN} Range (V)	Linearity (% of FSR) max	Tempco (ppm of FSR/°C) max	Temp Range(2)	Package	Page
Low Cost, Monolithic	VFC32KP★	User-selected, 500kHz, max	User-selected	±0.01 at 10kHz	75 typ	Com	DIP	10-3
	VFC32BM, (Q)			±0.05 at 100kHz	±100	Ind	TO-100	10-3
	VFC32SM, (Q)			±0.2 at 500kHz	±150	MIL	TO-100	10-3
Military	VFC32/MIL Series	See Military Products, page xxi						
Low Cost Complete	VFC42BP	0 to 10	0 to +10	±0.01	±100	Ind	DIP	10-11
	VFC42SM	0 to 10	0 to +10	±0.01	±100	MIL	DIP	10-11
	VFC52BP	0 to 100	0 to +10	±0.05	±150	Ind	DIP	10-11
	VFC52SM	0 to 100	0 to +10	±0.05	±150	MIL	DIP	10-11
Precision Monolithic	VFC62BG	User-selected, 1MHz max	User-selected	±0.005 at 10kHz	±50	Ind	DIP	10-17
	VFC62BM			±0.005 at 10kHz	±50	Ind	TO-100	10-17
	VFC62SM			±0.005 at 10kHz	±50	MIL	TO100	10-17
	VFC62CG			±0.002 at 10kHz	±20	Ind	DIP	10-17
	VFC62CM			±0.002 at 10kHz	±20	Ind	TO-100	10-17
	VFC320BG	User-selected, 1MHz max	User-selected	±0.005 at 10kHz	±50	Ind	DIP	10-25
	VFC320BM			±0.005 at 10kHz	±50	Ind	TO-100	10-25
	VFC320SM			±0.005 at 10kHz	±50	MIL	TO-100	10-25
	VFC320CG			±0.002 at 10kHz	±20	Ind	DIP	10-25
	VFC320CM			±0.002 at 10kHz	±20	Ind	TO-100	10-25
Synchronized Monolithic	• VFC100AG	Clock Programmed, 2MHz max	0 to +10	0.025 at 100kHz	±100	Ind	DIP	199
	• VFC100BG		0 to +10	0.1 at 1MHz	±50	Ind	DIP	199
	• VFC100SG		0 to +10	0.025 at 100kHz	±100	MIL	DIP	199

★Die available. See page 223.
NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, page xxi. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

DATA ACQUISITION SYSTEMS

Designed for high performance general purpose applications, these systems provide a complete data acquisition function in one small package. You can devote your design efforts to other tasks because the totally self-contained system includes input multiplexer, instrumentation amplifier (in some models), sample-and-hold amplifier and 12-bit A/D converter. Timing and control logic, clock and reference are all internal. A host of features—even tri-state outputs for microprocessor buses—make this system practical, even in high volume buys.

DATA ACQUISITION SYSTEMS							
Description	Model	Channels	Resolution (Bits)	Throughput Accuracy (% of FSR)	Throughput Rate, min (kHz)	Package	Page
Modular	SDM853	16 single-ended, 8 differential	12	±0.025	30[1]	Module	8-59
Hybrid ±10V Input	SDM854AG SDM854BG	16 single-ended, 8 differential	12 12	±0.048 ±0.024	33 25	QIP[2] QIP	8-65 8-65
Hybrid	SDM856JG SDM856KG	16 single-ended, 8 differential	12 12	±0.048 ±0.024	33 25	QIP QIP	8-81 8-81
Hybrid Low Level	SDM857JG SDM857KG	16 single-ended, 8 differential	12 12	±0.048 ±0.024	22 18	QIP QIP	8-81 8-81

NOTES: (1) Can be increased if short-cycled to 8- or 10-bit resolution. (2) Quad in-line package.

MICROPROCESSOR INTERFACED ANALOG INPUT AND OUTPUT SYSTEMS

These data acquisition systems are complete—totally interfaced to the microprocessor bus with no external interfacing components required. They provide an instant solution by preserving your valuable engineering design resources. 16-channel analog input systems talk directly to popular buses under control of the microprocessor. They are truly design-in-and-forget solutions to analog interface problems.

MICROPROCESSOR INTERFACED ANALOG INPUT SYSTEMS							
Description	Model	Channels	Resolution (Bits)	Accuracy (% of FSR) max	Tempco (ppm/°C) max	Package	Page
8080-, SC/MP-Compatible	MP20	16 single-ended, 8 differential	8	±0.8, high ±0.4, low	±40	QIP[2]	8-11
Universal	MP22BG	16 single-ended, 8 differential	12	±0.4, high ±0.1, low	±25[1]	QIP	8-35
High-Accuracy	MP32BG MP32CG	16 single-ended, 8 differential	12 12	±0.05 ±0.025	±60 ±60	QIP QIP	8-43 8-43

NOTES: (1) Unipolar, excluding IA. (2) Quad in-line package.

SAMPLE/HOLD CIRCUITS

Proven technologies applied to these circuits achieve very high speed and accuracy for demanding applications. SHC298AM is a low cost monolithic. Designed to be performance compatible to Burr-Brown A/D and D/A converters, the application of all of these S/H circuits is quick and easy.

SAMPLE/HOLD CIRCUITS								
Description	Model[1]	Gain/Offset Error (%) (mV)	Charge Offset (mV)	Droop Rate (mV/msec)	Tempco (ppm of 20V/°C)	Acquisition Time (μsec)[2]	Package	Page
Low Cost, Complete	SHC80KP	±0.01, ±2 max	±2 max	0.5 max	3	10 max	DIP	7-3
High Speed, Complete	SHC85, (Q) SHC85ET, (Q)	±0.01, ±2 max ±0.01, ±2 max	±2 max ±2 max	0.5 max 0.5 max	3 3	4.5 max 4.5 max	DIP[3] DIP[3]	7-7 7-7
Low Cost, Monolithic	SHC298AM	±0.01, ±7 max	±25 max	10 max[4]	4	10 max	TO-99[3]	7-11
Low Cost, High Speed, Monolithic	• SHC5320KH • SHC5320SH	N/A[5], ±0.5[6] N/A[5], ±0.5[6]	1 typ 1 typ	0.5 max 0.5 max	N/A[5] N/A[5]	1.5 max 1.5 max	DIP[3] DIP[3]	176 176
Very-High Speed	SHM60	±0.01, ±1.5	±1.5	5	2	1 max	Module	7-23
Ultra-High Speed	SHC803BM SHC803CM SHC804BM SHC804CM	±0.1, ±5 max ±0.1, ±3 max ±0.1, ±5 max ±0.1, ±3 max	±10 max ±5 max ±10 max ±5 max	±5 max ±5 max ±5 max ±5 max	±10 max ±5 max ±10 max ±5 max	300nsec max 300nsec max 300nsec max 300nsec max	DIP DIP DIP DIP	7-17 7-17 7-17 7-17

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, page xxi. (2) 10V step to 0.01% of final value. (3) Hermetic. (4) With 1000pF external holding capacitor.

MULTIPLEXERS

Models MPC4, MPC8 and MPC16 offer over-voltage protected inputs that can withstand up to 20 volts greater than either supply—especially important when input signals are present and MUX power is off. Models MPC800 and MPC801 provide fast settling time for high throughput rate systems. All models have internal channel selection decoding and low leakage current to be compatible with higher accuracy systems.

MULTIPLEXERS								
Description	Model	Channels	Input Range (V)	On Resistance max	Crosstalk (% of OFF Channel Signal)	Settling Time (to 0.01%)	Package	Page
Protected Inputs	MPC8S	8 single	±15	1.8kΩ	0.005	5μsec	DIP	9-3
	MPC4D	4 differential	±15	1.8kΩ	0.005	5μsec	DIP	9-3
	MPC16S	16 single	±15	1.8kΩ	0.005	7μsec	DIP	9-10
	MPC8D	8 differential	±15	1.8kΩ	0.005	7μsec	DIP	9-10
High Speed	MPC800KG	16 single or	±15	750Ω	0.004	800nsec	DIP	9-17
	MPC800SG	8 differential	±15	750Ω	0.004	800nsec	DIP	9-17
	MPC801KG	8 single or	±15	750Ω	0.004	800nsec	DIP	9-24
	MPC801SG	4 differential	±15	750Ω	0.004	800nsec	DIP	9-24

HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

Your requirements for precise, accurate op amp performance in critical applications dictate our product design direction. We have applied our unequalled skills and experience in op amp design (we marketed the first solid state op amp in 1959) to solve your problems when you must have special performance: *very low bias current, low noise, low voltage drift vs temperature, wide bandwidth, high voltage or high current.* This broad selection—offering special performance characteristics—lets you select the right op amp without compromising your design.

Each of these differing amplifier functions requires very specific expertise—in design, assembly and testing. We have developed a unique set of skills in each area and our complete microelectronic facilities fully support the challenge of meeting your most demanding needs.

GENERAL PURPOSE

These moderately priced FET and bipolar op amps offer good performance over a wide range of parameters. These are good options when a special function op amp is not required. You can be confident that Burr-Brown's quality and reliability are inherent in their design.

Products in this *Supplement* are indicated by a ● next to model numbers; others are in the *Product Data Book.*

GENERAL PURPOSE												
		Offset Voltage		Bias	Open	Frequency Response		Rated Output				
		At 25°C	Temp Drift	Current (25°C)	Loop Gain		Slew					
Description	Model[1]	±mV max	±μV/°C max	nA max	dB min	GBW MHz	Rate V/μsec	±V min	±mA min	Temp Range[2]	Package	Page
Bipolar	3500A	5	20	±30	93	1.5	0.6	10	10	Ind	TO-99	1-96
	3500B	2	5	±20	93	1.5	0.8	10	10	Ind	TO-99	1-96
	3500C	1	3	±15	93	1.5	1.0	10	10	Ind	TO-99	1-96
	3500R, (Q)	5	20	±30	93	1.5	0.6	10	10	Ind	TO-99	1-96
	3500S, (Q)	2	10	±20	93	1.5	0.8	10	10	MIL	TO-99	1-96
	3500T, (Q)	1	5	±15	93	1.5	1.0	10	10	MIL	TO-99	1-96
	3501A, (Q)	5	20	±15	93	0.5	0.1	10	5	Ind	TO-99	1-105
	3501B, (Q)	2	10	±7	93	0.5	0.1	10	5	Ind	TO-99	1-105
	3501C, (Q)	2	5	±3	93	0.5	0.1	10	5	Ind	TO-99	1-105
	3501R	5	20	±15	93	0.5	0.1	10	5	MIL	TO-99	1-105
	3501S	2	10	±7	93	0.5	0.1	10	5	MIL	TO-99	1-105
Low Power	OPA21GZ[4]	0.5	5	50	114	0.3	0.2	13.6	1.3	Ind	DIP	1-13
	OPA21EZ[4]	0.1	1	25	120	0.3	0.2	13.7	1.4	Ind	DIP	1-13
Switchable Input	OPA201AG	0.5	5	50	114	0.5	0.1	13.5	5	Com	DIP	1-61
	OPA201BG	0.2	2	40	114	0.5	0.1	13.5	5	Com	DIP	1-61
	OPA201CG	0.1	1	25	120	0.5	0.1	13.5	5	Com	DIP	1-61
	OPA201SG	0.2	2	40	114	0.5	0.1	13.5	5	MIL	DIP	1-61
FET	OPA103AM	0.50	25	−0.002	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103BM	0.50	15	−0.001	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103CM	0.25	5	−0.001	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103DM	0.25	2	−0.001	106	1	1.3	10	5	Ind	TO-99	1-43
	3542J, (Q)	20	50	−0.025	88	1.0	0.5	10	10	Com	TO-99	1-143
	3542S, (Q)	20	50	−0.025	88	1.0	0.5	10	10	MIL	TO-99	1-143
Low Cost FET	●OPA121KP	3	10	±0.010	106	2	2	10	5	Com	DIP	89
	●OPA606KP	3	10[3]	±0.025	90	12	30	11	5	Com	DIP	111
Wide Temp Range	OPA11HT	5	5[3]	±25	94	12.0	7.0	10	15	−55°C to +175°C	TO-99	1-9
Military	3500/MIL Series	See Military Products, page xxi										

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, page xxi. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Typical. (4) Only E and G grades are available on this product.

LOW DRIFT

Low offset voltage drift vs temperature performance in both FET and bipolar input types is obtained by our sophisticated drift compensation techniques. First, the drift is measured and then special laser trim techniques are used to minimize the drift and the initial offset voltage at 25°C. Finally, "max drift" performance is retested for conformance with specifications.

LOW DRIFT (≤5µV/°C)

Description	Model[1]	Offset Voltage At 25°C ±mV max	Offset Voltage Temp Drift ±µV/°C max	Bias Current (25°C) nA max	Open Loop Gain dB min	Frequency Response GBW MHz	Frequency Response Slew Rate V/µsec	Rated Output ±V min	Rated Output ±mA min	Temp Range[2]	Package	Page
FET	OPA103CM	0.25	5	−0.001	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103DM	0.25	2	−0.001	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA111AM★	0.5	5	±0.002	114	2	2	10	5	Ind	TO-99	1-51
	OPA111BM	0.25	1	±0.001	120	2	2	10	5	Ind	TO-99	1-51
	OPA111SM	0.5	5	±0.002	114	2	2	10	5	MIL	TO-99	1-51
Wideband	•OPA156AM	2	5	0.05	94	6	14	10	5	MIL	TO-99	95
	•OPA356AM	2	5	0.05	94	6	14	10	5	Com	TO-99	95
	•OPA606LM	0.5	5	±0.010	100	13	35	12	5	Com	TO-99	111
Dual FET	•OPA2111BM	0.5	2.8	±0.004	114	2	2	10	5	Ind	TO-99	119
Bipolar	•OPA27A	0.025	0.6	±40	120	8	1.9	10	16.6	MIL		79
	•OPA37A	0.025	0.6	±40	120	63[4]	11.9	10	16.6	MIL		79
	•OPA27B	0.060	1.3	±55	120	8	1.9	10	16.6	MIL		79
	•OPA37B	0.060	1.3	±55	120	63[4]	11.9	10	16.6	MIL		79
	•OPA27C	0.100	1.8	±80	97	8	1.9	10	16.6	MIL		79
	•OPA37C	0.100	1.8	±80	97	63[4]	11.9	10	16.6	MIL	TO-99/	79
	•OPA27E	0.025	0.6	±40	120	8	1.9	10	16.6	Ind	DIP	79
	•OPA37E	0.025	0.6	±40	120	63[4]	11.9	10	16.6	Ind		79
	•OPA27F	0.060	1.3	±55	120	8	1.9	10	16.6	Ind		79
	•OPA37F	0.060	1.3	±55	120	63[4]	11.9	10	16.6	Ind		79
	•OPA27G★	0.100	1.8	±80	97	8	1.9	10	16.6	Ind/Com		79
	•OPA37G★	0.100	1.8	±80	97	63[4]	11.9	10	16.6	Ind/Com		79
	3510AM	0.15	2	±35	120	0.4	0.5	10	10	Ind	TO-99	1-117
	3510BM	0.12	1	±25	120	0.4	0.5	10	10	Ind	TO-99	1-117
	3510CM	0.06	0.5	±15	120	0.4	0.5	10	10	Ind	TO-99	1-117
	3500B	2	5	±20	93	1.5	0.8	10	10	Ind	TO-99	1-96
	3500C	1	3	±15	93	1.5	1.0	10	10	Ind	TO-99	1-96
	3500T, (Q)	1	3	±15	93	1.5	1.0	10	10	MIL	TO-99	1-96
	3500E	0.50	1	±50	100[6]	1.5	0.8	10	10	Ind	TO-99	1-96
	3500MP	0.20[5]	1[5]	±50	100[6]	1.5	0.8	10	10	Ind	TO-99	1-100
	3501C, (Q)	2	5	±3	93	0.5	0.1	10	5	Ind	TO-99	1-105
Low Power	OPA21EZ[7]	0.1	1	25	120	0.3	0.2	13.7	1.4	Ind	DIP	1-13
Military	3510VM/883B	See Military Products, page xxi										
Inverting Only[3]	3291/14	0.02	0.10	±0.05	140	3	6	10	5	Ind	Module	1-86
	3292/14	0.05	0.30	±0.05	140	3	6	10	5	Ind	Module	1-86
	3293/14	0.10	1	±0.10	140	3	6	10	5	Ind	Module	1-86
High Voltage	3271/25	0.05	1	±0.08	140	1	20	110	20	Ind	Module	1-83

★Die available. See page 223.

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, page xxi. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) Chopper-stabilized. (4) Gain ≥5. (5) These specifications apply to the match between two devices. The 3500MP is a matched pair of amplifiers. (6) Typical. (7) Only E and G grades are available on this product.

LOW BIAS CURRENT

Our many years of experience in designing, manufacturing and testing FET amplifiers gives us unique abilities in providing low and ultra low bias current op amps. These amplifiers offer bias currents as low as 75fA (75×10^{-15} amps) and low voltage drift as low as 1µV/°C. With offset voltage laser-trimmed to as low as 250µV, the need for expensive trim pot adjustments is eliminated.

LOW BIAS CURRENT (≤100pA)												
		Offset Voltage		Bias Current (25°C) pA max	Open Loop Gain dB min	Frequency Response		Rated Output				
Description	Model[1]	At 25°C ±mV max	Temp Drift ±µV/°C max			GBW MHz	Slew Rate V/µsec	±V min	±mA min	Temp Range[2]	Package	Page
Premium Performance	OPA111AM★	0.5	5	±2	114	2	2	10	5	Ind	TO-99	1-51
	OPA111BM	0.25	1	±1	120	2	2	10	5	Ind	TO-99	1-51
	OPA111SM	0.5	5	±2	114	2	2	10	5	MIL	TO-99	1-51
Low Bias Current	OPA103AM	0.50	25	−2	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103BM	0.50	15	−1	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103CM	0.25	5	−1	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103DM	0.25	2	−1	106	1	1.3	10	5	Ind	TO-99	1-43
Low Noise	OPA101AM	0.50	10	−15	94	10	6.5	12	12	Ind	TO-99	1-31
	OPA101BM	0.25	5	−10	94	10	6.5	12	12	Ind	TO-99	1-31
	OPA102AM	0.50	10	−15	94	40	14	12	12	Ind	TO-99	1-31
	OPA102BM	0.25	5	−10	94	40	14	12	12	Ind	TO-99	1-31
Ultra-Low Bias Current	OPA104AM	1.0	25	−0.300	106	1	2.2	10	5	Ind	TO-99	1-47
	OPA104BM	0.50	15	−0.150	106	1	2.2	10	5	Ind	TO-99	1-47
	OPA104CM	0.50	10	−0.075	106	1	2.2	10	5	Ind	TO-99	1-47
	3528AM, (Q)	0.50	15	−0.300	88	0.7	0.3	10	5	Ind	TO-99	1-137
	3528BM, (Q)	0.25	5	−0.150	92	0.7	0.3	10	5	Ind	TO-99	1-137
	3528CM, (Q)	0.50	10	−0.075	90	0.7	0.3	10	5	Ind	TO-99	1-137
	3523J, (Q)	1.0	50	−0.50	100	1	0.6	10	10	Com	TO-99	1-129
	3523K	0.50	25	−0.25	100	1	0.6	10	10	Com	TO-99	1-129
	3523L, (Q)	0.50	25	−0.10	100	1	0.6	10	10	Com	TO-99	1-129
Dual FET	•OPA2111AM★	0.75	6	±8	110	2	2	10	5	Ind	TO-99	119
	•OPA2111BM	0.5	2.8	±4	114	2	2	10	5	Ind	TO-99	119
	•OPA2111SM	0.75	6	±8	110	2	2	10	5	MIL	TO-99	119
Low Cost	•OPA121KM	2	10	±5	110	2	2	10	5	Com	TO-99	89
	•OPA121KP	3	10	±10	106	2	2	10	5	Com	DIP	89
	3542J	20	50	−25	88	1	0.5	10	10	Com	TO-99	1-143
	3542S	20	50	−25	88	1	0.5	10	10	MIL	TO-99	1-143
Chopper-Stabilized	3291/14	0.02	0.1	±50	140	3	6	10	5	Ind	Module	1-86
	3292/14	0.05	0.3	±50	140	3	6	10	5	Ind	Module	1-86
	3293/14	0.10	1	±100	140	3	6	10	5	Ind	Module	1-86
	3271/25	0.05	1	±80	140	1	20	110	20	Ind	Module	1-83
Wideband	3554AM, (Q)	2	50	−50	100	1000	1000	10	100	Ind	TO-3	1-159
	3554BM, (Q)	1	15	−50	100	1000	1000	10	100	Ind	TO-3	1-159
	3554SM, (Q)	1	25	−50	100	1000	1000	10	100	MIL	TO-3	1-159
	•OPA156AM	2	5	50	94	6	14	10	5	MIL	TO-99	95
	•OPA356AM	2	5	50	94	6	14	10	5	Com	TO-99	95
	•OPA606KM	1.5	5 T.	±15	95	12.5	33	11	5	Com	TO-99	111
	•OPA606LM	0.5	5	±10	100	13	35	12	5	Com	TO-99	111
	•OPA606SM	1.5	5 T.	±15	95	12.5	33	11	5	Mil	TO-99	111
	•OPA606KP	3	10 T.	±25	90	12	30	11	5	Com	DIP	111
High Current	3571AM, (Q)	2	40	−100	94	0.5	3	30	1A	Ind	TO-3	1-167
	3572AM	2	40	−100	94	0.5	3	30	2A	Ind	TO-3	1-167
High Voltage	3580J	10	30	−50	86	5	15	30	60	Com	TO-3	1-177
	3581J	3	25	−20	94	5	20	70	30	Com	TO-3	1-177
	3582J, (Q)	3	25	−20	100	5	20	145	15	Com	TO-3	1-177
	3583AM, (Q)	3	25	−20	105	5	30	140	75	Ind	TO-3	1-181
	3583JM	3	25	−20	94	5	30	140	75	Com	TO-3	1-181
	3584JM, (Q)	3	25	−20	100	20	150	145	15	Com	TO-3	1-185
General Purpose	3522J	1.0	50	−10	94	1	0.6	10	10	Com	TO-99	1-123
	3522K	0.50	10	−5	94	1	0.6	10	10	Com	TO-99	1-123
	3522L	0.50	25	−1	94	1	0.6	10	10	Com	TO-99	1-123
	3522S, (Q)	0.50	25	−5	94	1	0.6	10	10	MIL	TO-99	1-123
	3527AM, (Q)	0.50	10	−5	100	1	0.6	10	10	Ind	TO-99	1-133
	3527BM, (Q)	0.25	5	−2	100	1	0.6	10	10	Ind	TO-99	1-133
	3527CM, (Q)	0.25	2	−5	100	1	0.6	10	10	Ind	TO-99	1-133
	3521H	0.50	10	−20	94	1.5	0.6	10	10	Com	TO-99	1-123
	3521J, (Q)	0.25	5	−20	94	1.5	0.6	10	10	Com	TO-99	1-123
	3521K	0.25	2	−15	94	1.5	0.6	10	10	Com	TO-99	1-123
	3521L	0.25	1	−10	94	1.5	0.6	10	10	Com	TO-99	1-123
	3521R, (Q)	0.25	5	−20	94	1.5	0.6	10	10	MIL	TO-99	1-123

★Die available. See page 223.

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, page xxi. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

LOW NOISE

Now both FET and bipolar input op amps are offered with guaranteed low noise specifications. Until now the designer had to rely on "typical" specs for his demanding low noise designs. These fully characterized parts allow a truly complete error budget calculation.

LOW NOISE (Guaranteed e_n)

Description	Model	Noise Voltage $nV/\sqrt{Hz}$ at 10kHz max	Bias Current (25°C) pA max	Offset Voltage At 25°C ±mV max	Offset Voltage Temp Drift ±μV/°C max	Open Loop Gain dB min	Frequency Response GBW MHz	Frequency Response Slew Rate V/μsec min	Rated Output ±V min	Rated Output ±mA min	Temp Range (1)	Package	Page
Bipolar	•OPA27A	3.8	±40nA	0.025	0.6	120	8	1.7	10.0	16.6	MIL		79
	•OPA37A	3.8	±40nA	0.025	0.6	120	63	11	10.0	16.6	MIL		79
	•OPA27B	3.8	±55nA	0.060	1.3	120	8	1.7	10.0	16.6	MIL		79
	•OPA37B	3.8	±55nA	0.060	1.3	120	63	11	10.0	16.6	MIL		79
	•OPA27C	4.5	±80nA	0.100	1.8	97	8	1.7	10.0	16.6	MIL		79
	•OPA37C	4.5	±80nA	0.100	1.8	97	63	11	10.0	16.6	MIL	TO-99/	79
	•OPA27E	3.8	±40nA	0.025	0.6	120	8	11	10.0	16.6	Ind	DIP	79
	•OPA37E	3.8	±40nA	0.025	0.6	120	63	11	10.0	16.6	Ind		79
	•OPA27F	3.8	±55nA	0.060	1.3	120	8	1.7	10.0	16.6	Ind		79
	•OPA37F	3.8	±55nA	0.060	1.3	120	63	11	10.0	16.6	Ind		79
	•OPA27G★	4.5	±80nA	0.100	1.8	97	8	1.7	10.0	16.6	Ind		79
	•OPA37G★	4.5	±80nA	0.100	1.8	97	63	11	10.0	16.6	Ind		79
FET	OPA101AM	8	−15	0.5	10	94	20	5	12	12	Ind	TO-99	1-31
	OPA101BM	8	−10	0.25	5	94	20	5	12	12	Ind	TO-99	1-31
	OPA102AM	8	−15	0.5	10	94	40	10	12	12	Ind	TO-99	1-31
	OPA102BM	8	−10	0.25	5	94	40	10	12	12	Ind	TO-99	1-31
	OPA111AM★	8	±2	0.5	5	114	2	1	10	5	Ind	TO-99	1-51
	OPA111BM	8	±1	0.25	1	120	2	1	10	5	Ind	TO-99	1-51
	OPA111SM	8	±2	0.5	5	114	2	1	10	5	MIL	TO-99	1-51
	•OPA606LM	13	±10	0.5	5	100	13	25	12	5	Com	TO-99	111
Dual FET	•OPA2111AM★	8	±8	0.75	6	110	2	1	10	5	Ind	TO-99	119
	•OPA2111BM	8	±4	0.5	2.8	114	2	1	10	5	Ind	TO-99	119
	•OPA2111SM	8	±4	0.75	6	110	2	1	10	5	MIL	TO-99	119

★Die available. See page 223.
NOTES: (1) Ind = −25°C to +85°C; MIL = −55°C to +125°C.

UNITY-GAIN BUFFER (Power Booster)

These versatile amplifiers: boost the output current capability of another amplifier; buffer an impedance that might load a critical circuit; may be used inside the feedback loop of another op amp to form a current-boosted, composite amplifier. Currents as high as ±100mA are available with speeds of 2000V/μsec.

UNITY-GAIN BUFFER

Description	Model	Rated Output ±V min	Rated Output ±mA min	Frequency Response −3dB MHz	Frequency Response Full Power BW MHz	Frequency Response Slew Rate V/μsec	Gain V/V	Input Impedance Ω	Open Loop Gain dB	Temp Range(1)	Package	Page
Noninverting	3553AM	10	200	300	32	2000	≈1	10^{11}	NA	Ind	TO-3	1-155
	3329/03	10	100	5	1	—	≈1	10k	NA	Ind	DIP	1-92

NOTES: (1) Ind = −25°C to +85°C.

WIDE BANDWIDTH

Design expertise in wideband circuits combines with our fully developed technology to create cost effective wideband op amps. Burr-Brown high speed amplifiers also offer outstanding DC performance specifications.

WIDE BANDWIDTH (≥5MHz)

Description	Model(1)	Frequency Response GBW MHz	Frequency Response Slew Rate V/μsec min	t_s ±0.1% nsec	Compensation	Rated Output ±V min	Rated Output ±mA min	Offset Voltage At 25°C ±mV max	Offset Voltage Temp Drift ±μV/°C max	Open Loop Gain dB	Temp Range (2)	Package	Page
FET	3554AM, (Q)	1700,	1000	120	ext.	10	100	2	50	100	Ind	TO-3	1-159
	3554BM, (Q)	A=	1000	120	ext.	10	100	1	15	100	Ind	TO-3	1-159
	3554SM, (Q)	1000	1000	120	ext.	10	100	1	25	100	MIL	TO-3	1-159
	3551J	50, A=10	250	400	ext.	10	10	1	50(3)	100	Com	TO-99	1-151
	3551S, (Q)	50, A=10	250	400	ext.	10	10	1	50(3)	100	MIL	TO-99	1-151
	3550J	10, A=10	65	400	int.	10	10	1	50(3)	100	Com	TO-99	1-147
	3550K	20, A=1	100	400	int.	10	10	1	50(3)	100	Com	TO-99	1-147
	3550S, (Q)	10, A=1	65	400	int.	10	10	1	50(3)	100	MIL	TO-99	1-147

WIDE BANDWIDTH (≥5MHz) (continued)													
		Frequency Response				Rated Output		Offset Voltage					
Description	Model[1]	GBW MHz	Slew Rate V/μsec min	t_s ±0.1% nsec	Compensation	±V min	±mA min	At 25°C ±mV max	Temp Drift ±μV/°C max	Open Loop Gain dB	Temp Range [2]	Package	Page
Bipolar	3508J	100, A=100	20	—	ext.	10	10	5	30[3]	103	Com	TO-99	1-113
	3507J, (Q)	20, A=10	80	200	ext.	10	10	10	30[3]	83	Com	TO-99	1-109
FET	●OPA156AM	6, A = 1	10	1.5μsec	int.	10	5	2	5	94	MIL	TO-99	95
	●OPA356AM	6, A = 1	10	1.5μsec	int.	10	5	2	5	94	Com	TO-99	95
	OPA605H	200, A=1000	300[3]	300	ext.	10	30	1	25	96	Com	DIP	1-77
	OPA605A	200, A=1000	300[3]	300	ext.	10	30	1	25	96	Ind	DIP	1-77
	OPA605K	200, A=1000	300[3]	300	ext.	10	30	0.5	5	96	Com	DIP	1-77
	OPA605C	200, A=1000	300[3]	300	ext.	10	30	0.5	5	96	Ind	DIP	1-77
	●OPA606KM	12.5, A = 1	22	1μsec	int.	11	5	1.5	5[3]	95	Com	TO-99	111
	●OPA606LM	13, A = 1	25	1μsec	int.	12	5	0.5	5	100	Com	TO-99	111
	●OPA606SM	12.5, A = 1	22	1μsec	int.	11	5	1.5	5[3]	95	MIL	TO-99	111
	●OPA606KP	12, A = 1	20	1μsec	int.	11	5	3	10[3]	90	Com	DIP	111
Low Noise Bipolar	●OPA27A	8, A = 1	1.7	—	int.	10	16.6	0.025	0.6	120	MIL		79
	●OPA37A	63, A = 5	11	—	int.[4]	10	16.6	0.025	0.6	120	MIL		79
	●OPA27B	8, A = 1	1.7	—	int.	10	16.6	0.060	1.3	120	MIL		79
	●OPA37B	63, A = 5	11	—	int.[4]	10	16.6	0.060	1.3	120	MIL		79
	●OPA27C	8, A = 1	1.7	—	int.	10	16.6	0.100	1.8	97	MIL		79
	●OPA37C	63, A = 5	11	—	int.[4]	10	16.6	0.100	1.8	97	MIL	TO-99/	79
	●OPA27E	8, A = 1	1.7	—	int.	10	16.6	0.025	0.6	120	Ind	DIP	79
	●OPA37E	63, A = 5	11	—	int.[4]	10	16.6	0.025	0.6	120	Ind		79
	●OPA27F	8, A = 1	1.7	—	int.	10	16.6	0.060	1.3	120	Ind		79
	●OPA37F	63, A = 5	11	—	int.[4]	10	16.6	0.060	1.3	120	Ind		79
	●OPA27G★	8, A = 1	1.7	—	int.	10	16.6	0.100	1.8	97	Ind		79
	●OPA37G★	63, A = 5	11	—	int.[4]	10	16.6	0.100	1.8	97	Ind		79
Low Noise FET	OPA101AM	20, A=100	5	2.5μsec	int.	12	12	0.5	10	105	Ind	TO-99	1-31
	OPA101BM	20, A=100	5	2.5μsec	int.	12	12	0.25	5	105	Ind	TO-99	1-31
	OPA102AM	40, A=100	10	1.5μsec	int.	12	12	0.5	10	105	Ind	TO-99	1-31
	OPA102BM	40, A=100	10	1.5μsec	int.	12	12	0.25	5	105	Ind	TO-99	1-31
Fast Settling	OPA600UM	6000, A=1000	500	80	ext.	9	180	5	100	86	MIL	DIP	11-94
	OPA600VM	6000, A=1000	500	80	ext.	9	180	4	20	86	MIL	DIP	11-94
Unity-Gain Buffer	3553AM, (Q)	32	2000	—	—	10	200	50	300[3]	NA	Ind	TO-3	1-155
Wide Temp	OPA11HT	12, A=1	4	1.5μsec	ext.	10	15	5[3]	5	98	[5]	TO-99	1-9

★Die available. See page 223.

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, page xxi. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Typical. (4) G = 5 min for OPA37. (5) −55°C to +175°C.

HIGH VOLTAGE—HIGH CURRENT

These IC op amp designs set the pace for the industry and are a product of our extensive hybrid circuit technology. Output currents up to ±10A peak and voltages up to ±145V are available.

Output voltages > ±30V to ±145V.

HIGH VOLTAGE												
		Rated Output		Offset Voltage			Frequency Response					
Description	Model[1]	±V min	±mA min	At 25°C ±mV max	Temp Drift ±μV/°C max	Bias Current (25°C) pA max	Unity Gain MHz	Slew Rate V/μsec	Open Loop Gain dB	Temp Range [2]	Package	Page
FET	3584JM, (Q)	145	15	3	25	−20	20[3]	150	120	Com	TO-3	1-185
	3583AM, (Q)	140	75	3	25	−20	5	30	118	Ind	TO-3	1-181
	3583JM	140	75	3	25	−20	5	30	118	Com	TO-3	1-181
	3582J	145	15	3	25	−20	5	20	118	Com	TO-3	1-177
	3581J	70	30	3	25	−20	5	20	112	Com	TO-3	1-177
	3580J	30	60	10	30	−50	5	15	106	Com	TO-3	1-177
	3571AM, (Q)	30	1A[4]	2	40	−100	0.5	3	94	Ind	TO-3	1-167
	3572AM	30	2A[5]	2	40	−100	0.5	3	94	Ind	TO-3	1-167
Chopper-Stabilized	3271/25	110	20	0.05	1	±80	1	20	140	Ind	Module	1-83

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, page xxi. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Gain-bandwidth product. (4) 2A peak. (5) 5A peak.

Output currents > ±15mA to ±10A.

HIGH CURRENT												
		Rated Output		Offset Voltage		Bias Current	Frequency Response		Open Loop	Temp		
				At 25°C	Temp Drift	(25°C)	Unity	Slew	Gain	Range		
Description	Model[1]	±V min	±mA min	±mV max	±μV/°C max	pA max	Gain MHz	Rate V/μsec	dB	[2]	Package	Page
High Power	OPA501AM	20	10A	10	65	40nA	1	1.5	94	Ind	TO-3	1-69
	OPA501BM	26	10A	5	40	20nA	1	1.5	98	Ind	TO-3	1-69
	OPA501RM	20	10A	10	65	40nA	1	1.5	94	MIL	TO-3	1-69
	OPA501SM	26	10A	5	40	20nA	1	1.5	98	MIL	TO-3	1-69
	●OPA511AM	22	5A	10	65	40	1	1.0	91	Ind	TO-3	101
	●OPA512BM	39	10A	6	65	30	4	2.5	96	Ind	TO-3	106
	●OPA512SM	43	15A	3	40	20	4	2.5	96	MIL	TO-3	106
	3573AM	20	2A[5]	10	65	40nA	1	2.6	94	Ind	TO-3	1-173
	3572AM	30	2A[5]	2	40	−100	0.5	3	94	Ind	TO-3	1-167
	3571AM, (Q)	30	1A[4]	2	40	−100	0.5	3	94	Ind	TO-3	1-167
Wideband	3554AM, (Q)	10	100	2	50	−50	1700[3]	1200	100	Ind	TO-3	1-159
	3554BM, (Q)	10	100	1	15	−50	1700[3]	1200	100	Ind	TO-3	1-159
	3554SM, (Q)	10	100	1	25	−50	1700[3]	1200	100	MIL	TO-3	1-159
High Voltage	3584JM, (Q)	145	15	3	25	−20	20[3]	150	126	Com	TO-3	1-185
	3583AM	140	75	3	25	−20	5	30	118	Ind	TO-3	1-181
	3583JM	140	75	3	25	−20	5	30	118	Com	TO-3	1-181
	3582J	145	15	3	25	−20	5	20	118	Com	TO-3	1-177
	3581J	70	30	3	25	−20	5	20	112	Com	TO-3	1-177
	3580J	30	60	10	30	−50	5	15	106	Com	TO-3	1-177
Booster	3553AM, (Q)	10	200	50	300[6]	−200	300	2000	NA	Ind	TO-3	1-155
(Buffer)	3329/03	10	100	50	—	Bipolar	5	—	NA	Ind	DIP	1-92

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, page xxi. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Gain-bandwidth product. (4) 2A peak. (5) 5A peak. (6) Typical.

INSTRUMENTATION AMPLIFIERS AND PROGRAMMABLE GAIN AMPLIFIERS

INSTRUMENTATION AMPLIFIERS

Performance requirements for instrumentation amplifiers call on different talents—in design, manufacturing and testing—than those associated with producing simpler operational amplifiers. We have perfected our thin-film resistor technology, an essential factor in achieving excellent matching and tracking of the critical resistors in the amplifier's circuit. Laser-trimmed to produce the high accuracy demanded by you, these thin-film resistor networks provide excellent performance and stability at low cost.

What is an instrumentation amplifier? It's a closed-loop, differential input gain block. The primary function of this committed circuit is to accurately amplify the voltage applied to its inputs. An instrumentation amplifier responds only to the difference between the two input signals. It exhibits extremely high impedance between the two input terminals and from each terminal to ground. The output voltage produced is single-ended with respect to ground and is equal to the product of amplifier gain and the difference of the two input voltages.

Where are instrumentation amplifiers used? They are most often used in applications where low level differential signals riding on high common-mode voltages (±10V) must be extracted and accurately amplified. These applications require high input impedance, high CMRR, low input noise, low offset voltage drift and excellent gain linearity and stability.

VERY HIGH ACCURACY

A "breakthrough" in instrumentation amplifiers, the INA101 provides superior performance previously associated with expensive hybrids but now achieved at the low cost of a monolithic. A true three-op amp design allows gains of 1 to 1000V/V. The INA104 includes a fourth op-amp for increased versatility—additional gain, guard driver or offset. All circuits, including the thin-film resistors, are integrated on a single monolithic chip. The input stage uses Burr-Brown's ultra-low drift, low noise technology to provide exceptional input characteristics.

DIFFERENCE AMPLIFIER

Unity-Gain (3627): These amplifiers appear to be simple in design and assembly, but the requirement for matched components and precision adjustments makes the "build" rather than buy decision questionable. Because of our thin-film resistor technology and laser-trim skills these amplifiers offer a very cost effective solution to a common circuitry design problem.

PROGRAMMABLE GAIN AMPLIFIERS

Differential Input: 3606 is a true three-op amp instrumentation amplifier whose gain is controlled with a 4-bit digital word. Eleven differential gain steps of 1, 2, 4, 8, 16...1024V/V offer software gain control for applications where instrumentation amplifiers must operate with wide dynamic range signals while maintaining high system resolution.

Noninverting Amplifier with Multiplexed Inputs: PGA100 is a precision, digitally-programmable-gain multiplexed-input amplifier. The user can select any one of eight analog input channels simultaneously with any one of eight noninverting binarily weighted gain steps of 1, 2, 4, 8...128V/V. The digital gain and channel select are latchable for microprocessor-compatible interface.

Products in this *Supplement* are indicated by a ● next to model numbers; others are in the *Product Data Book*.

Description	Model	Gain Range	Gain Accuracy G = 100, 25°C max	Gain Drift G = 100 ppm/°C	Non-Linearity G = 100 max %	Input Parameters: CMR, DC to 60Hz, G = 10 1kΩ Unbal...min	Input Parameters: Offset Voltage vs Temp max (μV/°C)	Dynamic Response G = 100 ±3dB BW (kHz)	Temp Range [1]	Package	Page
INSTRUMENTATION AMPLIFIERS											
Very-High Accuracy	INA101AM	1-1000[2]	0.03	22[3]	±0.007	96dB	±(2 + 20/G)	25	Ind	TO-100	2-7
	INA101CM	1-1000[2]	0.03	22[3]	±0.004	96dB	±(0.25 + 10/G)	25	Ind	TO-100	2-7
	INA101SM	1-1000[2]	0.03	22[3]	±0.004	96dB	±(0.25 + 10/G)	25	MIL	TO-100	2-7
	INA101AG	1-1000[2]	0.03	22[5]	±0.007	96dB	±(2 + 20/G)	25	Ind	DIP	2-7
	INA101CG	1-1000[2]	0.03	22[5]	±0.003	96dB	±(0.25 + 10/G)	25	Ind	DIP	2-7
	INA101SG	1-1000[2]	0.03	22[5]	±0.003	96dB	±(0.25 + 10/G)	25	MIL	DIP	2-7
	INA101HP	1-1000[2]	0.3	22[5]	±0.007	90dB	±(2 + 20/G) typ	25	Com	DIP	2-7
	●INA102AG★	1-1000	0.25	20	±0.05	80dB	±(5 + 10/G)	3	Ind	DIP	54
	●INA102CG	1-1000	0.15	15	±0.02	90dB	±(2 + 5/G)	3	Ind	DIP	54
	INA104HP	1-1000[2]	0.15	22	±0.007	96dB	±(2 ± 20/G)	25	Com	DIP	2-15
	INA104JP	1-1000[2]	0.15	22	±0.003	96dB	±(0.25 ± 10/G)	25	Com	DIP	2-15
	INA104KP	1-1000[2]	0.15	22	±0.003	96dB	±(0.75 ± 10/G)	25	Com	DIP	2-15
	INA104AM	1-1000[2]	0.15	22[5]	±0.007	96dB	±(2 ± 20/G)	25	Ind	DIP	2-15
	INA104BM	1-1000[2]	0.15	22[5]	±0.003	96dB	±(0.75 ± 10/G)	25	Ind	DIP	2-15
	INA104CM	1-1000[2]	0.15	22[5]	±0.003	96dB	±(0.25 ± 10/G)	25	Ind	DIP	2-15
	INA104SM	1-1000[2]	0.15	22[5]	±0.003	96dB	±(0.75 ± 10/G)	25	MIL	DIP	2-15
	3630AM	1-1000[2]	0.1	125[3]	±0.007	96dB	±(2 + 20/G)	25	Ind	DIP	2-74
	3630BM	1-1000[2]	0.05	125[3]	±0.003	96dB	±(0.75 + 10/G)	25	Ind	DIP	2-74
	3630CM	1-1000[2]	0.05	125[3]	±0.003	96dB	±(0.25 + 10/G)	25	Ind	DIP	2-74
	3630SM	1-1000[2]	0.05	125	±0.003	96dB	±(0.75 + 10/G)	25	Ind	DIP	2-74
General Purpose	3626AP	5-1000[2]	0.5	35[3]	±0.05	74dB	±(6 + 10/G)	14	Ind	DIP	2-60
	3626BP	5-1000[2]	0.5	35[3]	±0.04	80dB	±(3 + 5/G)	14	Ind	DIP	2-60
	3626CP	5-1000[2]	0.5	35[3]	±0.04	80dB	±(1 + 5/G)	14	Ind	DIP	2-60
	3629AM	5-1000[2]	0.1	45[3]	±0.007	106dB[4]	±(3 + 10/G)	30	Ind	DIP	2-68
	3629AP	5-1000[2]	0.1	45[3]	±0.007	106dB[4]	±(3 + 10/G)	30	Ind	DIP	2-68
	3629BM	5-1000[2]	0.1	45[3]	±0.004	106dB[4]	±(1.5 + 7.5/G)	30	Ind	DIP	2-68
	3629BP	5-1000[2]	0.1	45[3]	±0.004	106dB[4]	±(1.5 + 7.5/G)	30	Ind	DIP	2-68
	3629CM	5-1000[2]	0.1	45[3]	±0.004	106dB[4]	±(0.75 + 5/G)	30	Ind	DIP	2-68
	3629CP	5-1000[2]	0.1	45[3]	±0.004	106dB[4]	±(0.75 + 5/G)	30	Ind	DIP	2-68
	3629SM	5-1000[2]	0.1	45[3]	±0.004	106dB[4]	±(1.5 + 7.5/G)	30	Ind	DIP	2-68
Buffer, Unity-Gain Differential	3627AM	1V/V, fixed	0.01	5	±0.001[5]	90dB	30	800[5]	Ind	TO-99	2-64
	3627BM	1V/V, fixed	0.01	5	±0.001[5]	100dB	20	800[5]	Ind	TO-99	2-64
PROGRAMMABLE GAIN AMPLIFIERS											
Noninverting Multiplexed Input	PGA100AG	Gain set with 4-bit word 1, 2, 4, 8,...128	0.05	10	±0.01	NA	6[6]	5MHz	Ind	DIP	2-26
	PGA100BG		0.02	10	±0.005	NA	6[6]	5MHz	Ind	DIP	2-26
	●PGA102AG	Gain set With 2-bit word 1, 10 100	0.02	7	0.01	N/A	3(G = 100)	250	Ind	DIP	156
	●PGA102BG		0.01	7	0.01	N/A	3(G = 100)	250	Ind	DIP	156
	●PGA102SG		0.01	7	0.01	N/A	3(G = 100)	250	MIL	DIP	156
Instrumentation Amplifier Input	PGA200AG	Gain set with 2-bit word 1, 10, 100, 1000	0.05	20	±0.007	96dB	2(G = 100)	30	Ind	DIP	2-34
	PGA200BG		0.02	10	±0.003	96dB	0.4(G = 100	30	Ind	DIP	2-34
Differential Input	3606AG	Gain set with 3-bit word 1, 2, 4 8...1024	0.05	10	0.004	90dB, G = 1	±(3 + 50/G)	40	Ind	DIP	2-52
	3606AM		0.05	10	0.004	90dB, G = 1	±(3 + 50/G)	40	Ind	DIP	2-52
	3606BG		0.02	10	0.004	90dB, G = 1	±(1 + 20/G)	40	Ind	DIP	2-52
	3606BM		0.02	10	0.004	90dB, G = 1	±(1 + 20/G)	40	Ind	DIP	2-52

PRECISION TRANSMITTERS

Description	Model	Span: Un-trimmed Error max	Span: Non-Linearity max	Span: Temp Drift ppm/°C	Input Parameters: Offset Voltage max	Input Parameters: Offset Voltage vs Temp max μV/°C	Input Parameters: CMR DC, min	Output Parameters: Current Range mA	Output Parameters: Offset Current Error μA, max	Output Parameters: FS Output Current Error μA, max	Temp Range [1]	Pack-age	Page
Two-Wire	XTR100AM	−3%	0.01%	±100	±50μV	±1	90dB	4-20	±4	±20	Ind	DIP	2-40
	XTR100AP	−3%	0.01%	±100	±50μV	±1	90dB	4-20	±4	±20	Ind	DIP	2-40
	XTR100BM	−3%	0.01%	±100	±25μV	±0.5	90dB	4-20	±4	±20	Ind	DIP	2-40
	XTR100BP	−3%	0.01%	±100	±25μV	±0.5	90dB	4-20	±4	±20	Ind	DIP	2-40
Three-Wire and Current Source	●XTR110AG★	0.6	0.025	50	—	—	—	4-20, 0-20, 5-25 [7]	±64	±96	Ind	DIP	214
	●XTR110BG	0.2	0.005	30	—	—	—		±16	±32	Ind	DIP	214

★ Die available. See page 223.

NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (2) Set with external resistor. (3) With zero TC external resistor. (4) DC only. (5) Unity- gain. (6) Typical. (7) Many more ranges with appropriate circuit.

ISOLATION PRODUCTS

Another facet of design, assembly and testing expertise is involved in developing and manufacturing our isolation products: amplifiers and power supplies.

Isolation amplifiers provide a signal path from the amplifier input to its output with no galvanic connection. Two techniques are used to cross the isolation barrier: transformer coupling and optical coupling.

Isolation amplifiers are useful in several ways: 1) to amplify low level signals in the presence of high common-mode voltages; 2) reduce noise by breaking ground loops; 3) protect sensitive instruments from damage by large common-mode input voltages; 4) protect patients from ground faults in patient monitoring equipment.

Our optically coupled amplifiers use a unique bifurcated optical design to greatly improve linearity and make the gain insensitive to the level of output of the LED light source used. The technique splits the LED light output—part is sent to the output amplifier (across the isolation barrier) and part is sent back to the input. This provides a stable closed loop negative feedback design and makes the gain independent of the LED output level.

ISO100 is a second generation, optically coupled ISO amp which uses a new monolithic FC designed especially for optically coupled isolation amplifiers.

The 3650 uses a differential current input stage. The 3652 uses FET inputs to provide high input impedance and allow the direct application of voltage sources.

Transformer coupled designs offer a wide range of input characteristics—uncommitted op amps of either low drift or FET input types and true three-wire instrumentation amplifier configurations. Some models provide isolated power at the input from self-contained DC-to-DC converters.

The most unique model, 3656, provides true three-port isolation (independent isolation of input, output and power supply) and provides both signal and power isolation with only one transformer.

DC-to-DC converters provide high voltage isolation from input to output and are available with dual voltage outputs of one, two or four channels per unit.

We 100% test the isolation barrier on all isolation products using a very conservative relationship of test voltage equal to two times continuous rated voltage plus 1000V.

TRANSFORMER COUPLED AMPLIFIERS

		Isolation Voltage (V)		Isolation Mode Rejection, min.		Leakage Current at Test Voltage	Isolation Impedance		Gain Nonlinearity		Voltage Drift	Bias Current	±3dB Freq.	External Isolation Power	Temp. Range		
Description	Model	Continuous, peak	Pulse/Test, peak	DC (dB)	60Hz (dB)	(μA)	Ω	pF	max (%)	typ. (%)	±μV/°C max	max	kHz	Required	[1]	Package	Page
Low Drift[2]	3450	±500	±2000	160	120	1	10^{12}	16	±0.005	±0.0015	100	50nA	1.5	No	Com	Module	3-19
Low Bias FET	3451	±500	±2000	160	120	1	10^{12}	16	±0.025	±0.005	100	25pA	2.5	No	Com	Module	3-19
	3452	±2000	±5000	160	120	1	10^{12}	16	±0.025	±0.005	100	10pA	2.5	No[4]	Com	Module	3-19
	3455	[3]	[3]	160	120	[3]	10^{12}	16	±0.025	±0.005	100	20pA	2.5	No[4]	Com	Module	3-19
True 3-wire Instrumentation Amplifier	3456A	±2000	±5000	160	130	25	10^{12}	14	±0.02	±0.01	2 + (150/G_1)	50nA	2.5	No	Com	Module	3-27
	3456B	±2000	±5000	160	130	25	10^{12}	14	±0.08	±0.03	1 + (75/G_1)	50nA	2.5	No	Com	Module	3-27
Highest Isolation Voltage	3656AG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	25 + (500/G_1)	100nA	30	No	Ind	DIP	3-41
	3656BG	±3500	±8000	160	125	0.5	10^{12}	6	±0.05	±0.03	5 + (1000/G_1)	100nA	30	No	Ind	DIP	3-41
	3656HG	±3500	±8000	160	125	0.5	10^{12}	6	±0.15	±0.03	200 + (1000/G_1)	100nA	30	No	Com	DIP	3-41
	3656JG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	50 + (750/G_1)	100nA	30	No	Com	DIP	3-41
	3656KG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	10 + (350/G_1)	100nA	30	No	Com	DIP	3-41
OPTICALLY COUPLED AMPLIFIERS																	
Balanced Current Input	3650HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	25	10nA	15	Yes[6]	Ind	DIP	3-30
	3650JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.03	10	10nA	15	Yes[6]	Ind	DIP	3-30
	3650KG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.05	±0.02	5	10nA	15	Yes[6]	Ind	DIP	3-30
	3650MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100	10nA	15	Yes[6]	Ind	DIP	3-30
Balanced FET Input	3652HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	50	50nA	15	Yes[6]	Ind	DIP	3-33
	3652JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.05	25	50nA	15	Yes[6]	Ind	DIP	3-33
	3652MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100	50nA	15	Yes[6]	Ind	DIP	3-33
Low Drift Wide Bandwidth	ISO100AP	750	2500	146[7]	108[7]	0.3	10^{12}	2.5	0.4	0.1	10[7]	10nA	60	Yes[6]	Ind	DIP	3-6
	ISO100BP	750	2500	146[7]	108[7]	0.3	10^{12}	2.5	0.1	0.01	4[7]	10nA	60	Yes[6]	Ind	DIP	3-6
	ISO100CP	750	2500	146[7]	108[7]	0.3	10^{12}	2.5	0.07	0.02	4[7]	10nA	60	Yes[6]	Ind	DIP	3-6

DC/DC CONVERTERS

Description	Model	Input	Output	Isolation	Leakage Current	Package	Page
Regulated	546	4.5VDC to 5.5VDC, 400mA	Single-Bipolar, ±15V, 120mA	300V	Not Specified	Module	12-3
Isolated	722	5VDC to 16VDC, 120mA	Two-Bipolar, ±15V, 64mA/160mA	3500V[7], 8000V[7]	1μA at 240V, 60Hz	DIP	12-17
	722BG	5VDC to 16VDC, 120mA		3500V[7], 8000V[8]	1μA at 240V, 60Hz	DIP	12-17
	724	5VDC to 16VDC, 125mA	Four-Bipolar, ±8V	100V[7], 3000V[8]	1μA at 240V, 60Hz	DIP	12-21

NOTES: (1) Com = 0°C to +70°C; Ind = −25°C to +85°C. (2) Bipolar. (3) Isolation voltage tested at 2500V, rms, 60Hz; leakage current tested for 2μA max at 240V, rms, 60Hz. (4) ±15V at ±15mA isolated power available to power external circuitry. (5) At 240V/60Hz. (6) Models 722 or 724. (7) R_{IN} = 10k, Gain = 100. (8) Continuous. (9) Test.

ANALOG CIRCUIT FUNCTIONS

These circuits offer a broad range of versatile, proven and ready-to-use analog computational functions designed to work in simple and complex instrumentation and control systems. Primarily they process and/or condition analog signals—usually for simulation of algebraic or trigonometric computations. Burr-Brown has the widest selection of such functions available in the industry. How you apply these circuits is limited only by your creative imagination!

MULTIPLIERS/DIVIDERS

You can select accuracy from 0.25% to 2% max from this complete line of integrated circuit multipliers. Most provide full four-quadrant multiplication. All are laser-trimmed for accuracy—no trim pots are needed to meet specified performance. These compact models bring the cost of high performance down to acceptable levels.

MULTIPLIERS/DIVIDERS

Model[1]	Transfer Function	Error max at 25°C %, max	Temperature Coefficient %/°C	Feed-through mV	Offset Voltage mV	1% Band-width kHz	Temp Range [2]	Package	Page
4203J	XY/10	2	0.04	50	20	40	Com	TO-100	4-89
4203K	*	1	0.04	50	20	40	Com	TO-100	4-89
4203S, (Q)	*	1	0.04	50	20	40	MIL	TO-100	4-89
4204J	XY/10	0.5	0.01	10	15	32	Ind	DIP	4-91
4204K	*	0.5	0.01	5	5	33	Ind	DIP	4-91
4204S, (Q)	*	0.25	0.02	5	5	33	MIL	DIP	4-91
4205J	$(X_1 - X_2)(Y_1 - Y_2)/10$	2	0.04	50	20	40	Com	TO-100	4-89
4205K	*	1	0.04	50	20	40	Com	TO-100	4-89
4205S, (Q)	*	1	0.04	50	20	40	MIL	TO-100	4-89
4206J	XY/10	0.5	0.01	10	15	33	Com	DIP	4-97
4206K	*	0.25	0.01	5	5	33	Com	DIP	4-97
4213AM, (Q)	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z$	1	0.008	30	10	70	Ind	TO-100	4-103
4213BM	*	0.5	0.008	30	7	70	Ind	TO-100	4-103
4213SM	*	0.5	0.008	30	7	70	MIL	TO-100	4-103
4213/MIL Series	See Military Products, page xxi								
MPY100A	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$	±2	0.017	100	50	70	Ind	TO-100	4-22
MPY100B	*	±1	0.008	30	10	70	Ind	TO-100	4-22
MPY100C	*	±0.5	0.008	30	7	70	Ind	TO-100	4-22
MPY100S	*	±0.5	0.025	30	7	70	MIL	TO-100	4-22
4214AP	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z$	1	0.02	30	10	70	Ind	DIP	4-110
4214BP	*	0.5	0.02	30	7	70	Ind	DIP	4-110
4214RM	*	1	0.02	30	10	70	Ind	DIP	4-110
4214SM	*	0.5	0.02	30	7	70	Ind	DIP	4-110

*Same as model above.

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, page xxi. (2) Com = 0°C to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

SPECIAL FUNCTIONS

This group of models offers many different functions that are the quick, easy way to solve a wide variety of analog computational problems. Most are in integrated circuit packages and are laser-trimmed for excellent accuracy.

SPECIAL FUNCTIONS

Function	Model	Description	Comments	Temp Range [1]	Package	Page
Multifunction Converter	4301 4302	$Y(Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	4301 is hermetically sealed and shielded in a metal package. 4302 is in a plastic package. Both units are pin-for-pin compatible.	Ind Ind	DIP DIP	4-114 4-116
	LOG100JP	K Log (I_1/I_2)	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity.	Com	DIP	4-114
Logarithmic Amplifier	4127JG 4127KP	K Log (I_1/I_{REF})	A more versatile part which contains an internal reference and a current inverter. 1% and 0.5% accuracy.	Com Com	DIP DIP	4-82 4-82
$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)dt}$	4340	True rms-to-DC conversion based on a log-antilog computational approach.	Laser-trimmed, requires no external trimming for rated accuracy. Hermetically sealed in a metal package.	Ind	DIP	4-122
	4341	True rms-to-DC conversion based on a log-antilog computational approach.	Some external trimming required. Lower cost in plastic package. Pin compatible with 4340.	Ind	DIP	4-126

SPECIAL FUNCTIONS (continued)						
Function	Model	Description	Comments	Temp Range (1)	Package	Page
Peak Detector	4085BM 4085KG 4085SM	These are analog memory circuits which hold and provide read-out of a DC voltage equal to peak value of a complex input waveform.	Digital mode control provides reset capability and allows selection of peaks within a desired time interval. May be used to make peak-to-peak detector.	Com Ind MIL	DIP DIP DIP	4-74 4-74 4-74
Window Comparator	4115/04	Provides a window or dual limit for comparison. Unit has 3 inputs: one for a voltage that sets upper limmit, one for a voltage that sets lower limit, and one for a signal input.	The 3 outputs are capable of sinking up to 200mA of current, indicating if the input voltage is above, below, or in the window.	Com	Module	4-80

NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

DIVIDERS

The use of a special log/antilog committed divider design overcomes the major problem encountered when trying to use a multiplier in a divider circuit. Outstanding accuracy is maintained even at very low denominator voltages.

DIVIDERS									
Model	Transfer Function	Input Range	Accuracy, max D = 250mV %	Temperature Coefficient %/°C	0.5% Bandwidth kHz	Rated Output, min	Temp Range(1)	Package	Page
DIV100HP	N/D 10	250mV	1.0	0.2	15	±10V, ±5mA	Ind	DIP	4-6
DIV100JP	N/D 10	to	0.5	0.2	15	±10V, ±5mA	Ind	DIP	4-6
DIV100KP	N/D 10	10V	0.25	0.2	15	±10V, ±5mA	Ind	DIP	4-6

NOTES: (1) Ind = −25°C to +85°C.

FREQUENCY PRODUCTS

This group of products consists of precision oscillators and active filters for both signal generation and attenuation. Both fixed frequency and user selected frequency units are available.

FREQUENCY PRODUCTS						
Function	Model	Description	Comments	Temp Range(1)	Package	Page
Oscillator	4023/25	Fixed-frequency (customer-specified, 10Hz to 20kHz) provides a low distortion, stable amplitude sine wave output.	Frequency stability vs temperature: 0.04%/°C max. Amplitude stability vs temperature: 0.02%/°C max.	Ind	Module	4-89
	4423	Very-low cost in plastic package. Provides resistor programmable quadrature outputs (sine and cosine wave outputs simultaneously available).	Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%.	Com	DIP	4-130
Universal Active Filter	UAF41 UAF31 UAF21 UAF11	These filters provide a complex pole pair. Based on state variable approach, low-pass, high-pass and bandpass outputs are available.	Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses.	Ind Ind Ind Ind	DIP DIP DIP DIP	4-60 4-52 4-44 4-44

NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C.

VOLTAGE REFERENCE

This product is a precision voltage reference which provides a +10V output. The output can be adjusted with minimal effect on drift or stability.

VOLTAGE REFERENCE								
				Power Supply				
Model	Output (V)	Minimum Output (mA)	Maximum Drift (ppm/°C)	(V)	(mA)	Temp Range(1)	Package	Page
REF10KM	+10.000 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	4-30
REF10JM	+10.000 ±0.005	10	2	+13.5/35	4.5	Com	TO-99	4-30
REF10SM	+10.000 ±0.005	10	3	+13.5/35	4.5	MIL	TO-99	4-30
REF10RM	+10.000 ±0.005	10	6	+13.5/35	4.5	MIL	TO-99	4-30
REF101KM	+10.000 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	4-36
REF101JM	+10.000 ±0.005	10	2	+13.5/35	4.5	Com	TO-99	4-36
REF101SM	+10.000 ±0.005	10	3	+13.5/35	4.5	MIL	TO-99	4-36
REF101RM	+10.000 ±0.005	10	6	+13.5/35	4.5	MIL	TO-99	4-36

NOTES: (1) Com = 0 to +70°C; MIL = −55°C to +125°C.

MODULAR POWER SUPPLIES

Products in this *Supplement* are indicated by a • next to model numbers; others are in the *Product Data Book*.

A broad line of compact, easily mounted encapsulated power supplies, AC/DC and DC/DC converters, are available from Burr-Brown. They are designed to power analog interface circuitry involving operational, instrumentation and isolation amplifiers, A/D and D/A converters and analog circuit functions in digital and analog systems. DC/DC converters offer high input-output isolation for those computer interface applications where analog circuitry must be floated independent of digital ground.

We provide a wide range of output voltages and current. International input voltage ratings are also available.

Burr-Brown offers one of the largest, most complete selections of high performance DC/DC converters in the industry. The new Power/Plus Series includes over 400 feature-packed, low cost converters to meet demanding power conversion requirements in such applications as process control, telecommunications, portable equipment, automatic test systems and medical, airborne and shipboard electronics systems.

Surface-Mounted Device (SMD) technology is used exclusively in the production of Power/Plus converters, providing higher levels of DC/DC circuit performance in compact, rugged packages—all at no additional cost. Standard features of the Power/Plus Series—normally costly options in other conventional designs—include: input and output filtering; six-sided shielding; input overvoltage and output short-circuit protection; nonconductive packages; and, full UL544, VDE750 and CSA C22.2 dielectric withstand test compliance.

Power Plus converters also offer the best isolation voltage performance available—1000V peak minimum isolation voltage and 25pF isolation capacitance—and every unit is tested at 240VAC for barrier capacitance and leakage current.

AC POWER SUPPLIES

Description	Model	Rated Output	Rated Input	Regulation No Load to Full Load	Regulation Overrated Line Voltage	Output(1) Ripple/ Noise	Package	Page
Dual ±15VDC Supply P.C.B. Mount	550	±15V, ±25mA	105VAC to 125VAC, 50Hz to 400Hz (2) (3) (4)	±0.1%	±0.05%	2mV	Module	12-3
	551	±15V, ±50mA		±0.05%	±0.05%	0.5mV	Module	12-3
	552	±15V, ±100mA		±0.05%	±0.05%	0.5mV	Module	12-3
	553	±15V, ±200mA		±0.05%	±0.05%	0.5mV	Module	12-3
	554	±15V, ±350mA		±0.02%	±0.02%	0.5mV	Module	12-3
Dual ±15VDC Supply Chassis Mount	556	±15V, ±200mA	105VAC to 125VAC, 50Hz to 400Hz (2) (3) (4)	±0.05%	±0.05%	1mV	Module	12-3
	558	±15V, ±500mA		±0.05%	±0.05%	1mV	Module	12-3
5VDC Supply P.C.B. Mount	560	5V(5), ±250mA	105VAC to 125VAC, 50Hz to 400Hz (2) (3) (4)	±0.1%	±0.05%	1mV	Module	12-3
	561	5V(5), ±500mA		±0.1%	±0.05%	1mV	Module	12-3
	562	5V(5), ±1000mA		±0.1%	±0.05%	1mV	Module	12-3

DC/DC CONVERTERS

Description	Model	Input	Output	Isolation	Leakage Current	Package	Page
Regulated	546	4.5VDC to 5.5VDC 400mA	Single-Bipolar ±15V, 120mA	300V	Not Specified	Module	12-3
Isolated	PWR70	10VDC to 18VDC	±15VDC, ±15mA	2000Vp	2μA, max	Module	12-9
	•PWR71	10VDC to 18VDC	±15VDC, ±25mA	1000VDC	3μA, max	Module	167
	•PWR74	10VDC to 20 VDC	±15VDC, ±25mA	1500V$_{pk}$	2μA, max	Module	169
	700	10VDC to 18VDC 89mA	±10VDC to ±18VDC (±1V tolerance) at 60mA total	1500Vp	1μA, max	Module	12-11
	700U(5)	10VDC to 18VDC 89mA	±10VDC to ±18VDC (±1V tolerance) at 60mA total	2000Vp	1μA, max	Module	12-11
	710(6)	10VDC to 18VDC 100mA	Four sets of outputs each set: ±10VDC to ±18VDC (±1V tolerance) at 76mA total all outputs	1000Vp	1μA, max	Module	12-13
	722 722BG	5VDC to 16VDC 120mA	Two-Bipolar ±15V, 64mA	3500V(5) 8000V(6)	1μA at 240V, 60Hz	DIP	12-17
	724	5VDC to 16VDC 125mA	Four-Bipolar ±8V	1000V(5) 3000V(6)	1μA at 240V, 60Hz	DIP	12-24

NOTES: (1) At full load, rms (max). (2) 205VAC, 50Hz to 400Hz option available. (3) 90VAC to 110VAC, 50Hz to 400Hz option available. (4) 220VAC to 260VAC, 50Hz to 400Hz option available. (5) Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields. Model 700M and 700UM are similar to Models 700/700U but, in addition, they are 100% screened to patient-connected circuit requirements for the leakage current (par. 27.5) and withstand voltage (par. 31.11) of UL544. Additional per unit charge for 700M or 700UM. See Product Data Sheet for complete specifications. (6) Model 710 provides 4 channels (sets) of isolated outputs. See Product Data Sheet for complete specifications.

POWER/PLUS SERIES									
Single or Dual Output									
Model	Input Voltage (VDC)	Output Voltage (VDC)	Output Current (mA) by Series Type PWR 1xx	PWR 2xx	PWR 3xx	PWR 4xx	PWR 5xx	PWR 6xx	PWR 7xx
PWR x00	5	5	90	300	200	600	200	400	1000
x01		12	38	125	84	250	84	167	417
x02		15	30	100	67	200	67	134	334
x03		±5	±45	±150	±100	±300	±100	±200	±500
x04		±12	±19	±63	±42	±125	±42	±84	±209
x05		±15	±15	±50	±34	±100	±34	±67	±167
PWR x06	12	5	90	300	200	600	200	400	1000
x07		12	38	125	84	250	84	167	417
x08		15	30	100	67	200	67	134	334
x09		±5	±45	±150	±100	±300	±100	±200	±500
x10		±12	±19	±63	±42	±125	±42	±84	±209
x11		±15	±15	±50	±34	±100	±34	±67	±167
PWR x12	15	5	90	300	200	600	200	400	1000
x13		12	38	125	84	250	84	167	417
x14		15	30	100	67	200	67	134	334
x15		±5	±45	±150	±100	±300	±100	±200	±500
x16		±12	±19	±63	±42	±125	±42	±84	±209
x17		±15	±15	±50	±34	±100	±34	±67	±167
PWR x18	24	5	90	300	200	600	200	400	1000
x19		12	38	125	84	250	84	167	417
x20		15	30	100	67	200	67	134	334
x21		±5	±45	±150	±100	±300	±100	±200	±500
x22		±12	±19	±63	±42	±125	±42	±84	±209
x23		±15	±15	±50	±34	±100	±34	±67	±167
PWR x24	28	5	90	300	200	600	200	400	1000
x25		12	38	125	84	250	84	167	417
x26		15	30	100	67	200	67	134	334
x27		±5	±45	±150	±100	±300	±100	±200	±500
x28		±12	±19	±63	±42	±125	±42	±84	±209
x29		±15	±15	±50	±34	±100	±34	±67	±167
PWR x30	48	5	90	300	200	600	200	400	1000
x31		12	38	125	84	250	84	167	417
x32		15	30	100	67	200	67	134	334
x33		±5	±45	±150	±100	±300	±100	±200	±500
x34		±12	±19	±63	±42	±125	±42	±84	±209
x35		±15	±15	±50	±34	±100	±34	±67	±167
		Page	166	166	166	166	166	166	166

Triple Output						
Model	Input Voltage (VDC)	Output Channel 1 Voltage (VDC)	Current (mA)	Output Channel 2 Voltage (VDC)	Current (mA)	Page
PWR 800 PWR 801	5	5	250	±12 ±15	±156 ±125	166
PWR 802 PWR 803	12	5	250	±12 ±15	±156 ±125	166
PWR 804 PWR 805	15	5	250	±12 ±15	±156 ±125	166
PWR 806 PWR 807	24	5	250	±12 ±15	±156 ±125	166
PWR 808 PWR 809	28	5	250	±12 ±15	±156 ±125	166
PWR 810 PWR 811	48	5	250	±12 ±15	±156 ±125	166

HIGH RELIABILITY SCREENING

Available from Burr-Brown as Standard Product

Burr-Brown Q and /QM Programs offer a number of screened versions of standard industrial products at reasonable cost.

The Q and /QM Programs consist of screening standard industrial products in accordance with applicable test methods of MIL-STD-883. The screening sequence is listed in individual data sheets or in the Burr-Brown Q Program brochure LI-217F.The /QM Program uses MIL-STD-883, Internal Visual Inspection Method 2010 (for single die monolithics) or Method 2017 (for hybrid circuits) and Method 2050 for external visual.

The Q Program uses Burr-Brown Internal Visual Inspection QC4118 (for complex hybrids) and Burr-Brown QC5150 for External Visual Inspection.

These products are identified in this selection guide by "Q" or "QM" following the model number.

SCREENING SEQUENCE

Screen	Procedure*	Requirement/ Performed
Internal Visual Inspection (precap)	See paragraph at left	100%
Electrical Test	Per appropriate Burr-Brown product data sheet	100%
Stabilization Bake	MIL-STD-883, Method 1008	100%
Temperature Cycling	MIL-STD-883, Method 1010	100%
Hermeticity, Fine Leak	MIL-STD-883, Method 1014	100%
Hermeticity, Gross Leak	MIL-STD-883, Method 1014	100%
Burn-In	MIL-STD-883, Method 1015	100%
Constant Acceleration (centrifuge)	MIL-STD-883, Method 2001	100%
Final Electrical Test	Per appropriate Burr-Brown product data sheet	100%
External Visual Inspection	See paragraph at left	100%

*See detailed Screening Procedures for each product.

MILITARY PRODUCTS

Burr-Brown's Military Products meet the demand for high quality products for high reliability applications. They feature exceptional electrical performance from −55°C to +125°C, Hi-Rel manufacture, MIL-STD-883 class B screening, and reasonable prices.

They are designed to conservative and stringent MIL-M-38510 requirements, and are produced on a separate manufacturing line, which exceeds Burr-Brown's standard lines' quality. MIL-M-38510 and MIL-STD-883 processes and controls are used throughout. Cleanliness is impeccable, and the particle count in the assembly area is reduced by filtered, laminar air flow. The internal visual inspection is per method 2010 or 2017 and is performed three times. A monometallic wirebond system is used and anti-static precautions (including ion grids) and atmospheric moisture are constantly observed.

Complete, 12- to 16-page detailed specifications (data sheets) are written in MIL-M-38510 format and contain the information necessary for non-standard parts approval by the procuring activity on government programs. They contain fully specified min and max parameters, tests performed, MIL-STD-883 class B screening and burn-in, qualification and quality conformance inspections, and life testing. Applications information and typical performance are included in most detailed specifications.

Applications for Burr-Brown's Military products range from critical applications, such as a missile or tactical weapon, to routine applications, such as signal processing or test equipment. Three electrical performance grades (U, V, and W) and two product assurance levels (standard and /883B) within each product series provide a performance/product assurance choice for each application.

/883B PROCESSING

Sequence	Method	Requirements*
Manufacture		Burr-Brown high reliability manufacture includes traceability, rework and rebonding provisions, product and process change controls, date coding, etc.
Screening (Class B)	MIL-STD-883 Method 5004	Class B, 100% • Internal visual (Method 2010/2017) • Stabilization bake • Temperature cycle • Hermeticity, fine leak • Hermeticity, gross leak • Interim electrical • Burn-in • Constant acceleration • Final electrical • External visual
Qualification Conformance Inspection	MIL-STD-883 Method 5005/5008	Groups A & B plus periodic groups C** & D** • Group A - electrical tests • Group B - mechanical tests • Group C - die-related tests • Group D - package related tests
Qualification	MIL-STD-883 Method 5005/5008	Groups A, B, C & D upon special request (Most recent data available)

*See the detailed product data sheet for each product.
**As required by MIL-STD-883.

Products in this *Supplement* are indicated by a ● next to model numbers; others are in the *Product Data Book*.

ANALOG-TO-DIGITAL CONVERTERS								
Model	Resolution Bits	Linearity ±LSB, max	Conversion Time μsec, max	Gain Drift ±ppm/°C, max	Input Range V	Operating Temperature Range[1]	Package	Page
ADC87/883B	12	1/2	8	15	±2.5, ±5, ±10, 0 to +5, 0 to +10	MIL	32-pin DIP	11-8
ADC87	12	1/2	8	15	±2.5, ±5, ±10, 0 to +5, 0 to +10	MIL	32-pin DIP	11-8
ADC87U/883B	12	1/2	10	15	±2.5, ±5, ±10, 0 to +5, 0 to +10	MIL	32-pin DIP	11-8
ADC87U	12	1/2	10	15	±2.5, ±5, ±10, 0 to +5, 0 to +10	MIL	32-pin DIP	11-8
ADC87V/883B	12	1/2	10	15	±2.5, ±5, ±10, 0 to +5, 0 to +10	MIL	32-pin DIP	11-8
ADC87V	12	1/2	10	15	±2.5, ±5, ±10, 0 to +5, 0 to +10	MIL	32-pin DIP	11-8

DIGITAL-TO-ANALOG CONVERTERS									
Model	Resolution Bits	Linearity ±LSB, max	Monotonicity	Gain Drift ±ppm/°C, max	Settling Time max	Output Ranges	Operating Temperature Range(1)	Package	Page
DAC87-CBI-V/B	12	1/2	−55°C/+125°C	20	7μsec	±2.5, ±5, ±10, +5, +10	MIL	24-pin DIP	11-24
DAC87-CBI-V	12	1/2	−55°C/+125°C	20	7μsec		MIL	24-pin DIP	11-24
DAC87U-CBI-V/B	12	1/2	−25°C/+85°C	20	7μsec		MIL	24-pin DIP	11-24
DAC87U-CBI-V	12	1/2	−25°C/+85°C	20	7μsec		MIL	24-pin DIP	11-24
DAC87-CBI-I/B	12	1/2	−55°C/+125°C	20	400nsec	0 to 2mA, ±1mA	MIL	24-pin DIP	11-36
DAC87-CBI-I	12	1/2	−55°C/+125°C	20	400nsec		MIL	24-pin DIP	11-36
DAC87U-CBI-I/B	12	1/2	−25°C/+85°C	20	400nsec		MIL	24-pin DIP	11-36
DAC87U-CBI-I	12	1/2	−25°C/+85°C	20	400nsec		MIL	24-pin DIP	11-36
DAC870V/883B	12	1/2	−55°C/+125°C	25	7μsec	±2.5, ±5, ±10, 0 to +5, 0 to +10	MIL	24-pin DIP ceramic	11-48
DAC870V	12	1/2	−55°C/+125°C	25	7μsec		MIL		11-48
DAC870U/883B	12	1/2	−25°C/+85°C	20	7μsec		MIL		11-48
DAC870U	12	1/2	−25°C/+85°C	20	7μsec		MIL		11-48
DAC870VL/883B	12	1/2	−55°C/+125°C	25	7μsec		MIL	28-term. leadless chip carrier	11-48
DAC870VL	12	1/2	−55°C/+125°C	25	7μsec		MIL		11-48
DAC870UL/883B	12	1/2	−25°C/+85°C	20	7μsec		MIL		11-48
DAC870UL	12	1/2	−25°C/+85°C	20	7μsec		MIL		11-48

VOLTAGE-TO-FREQUENCY CONVERTERS							
Model	V_{IN} Range V	F_{OUT} Range kHz, max	Linearity % FSR, max	Full Scale Drift ppm FSR/°C, max	Operating Temperature Range(1)	Package	Page
VFC32WM/883B	±10	200	±0.006 at 10kHz	±100 at 10kHz	MIL	TO-100	11-20
VFC32WM	±10	200	±0.006 at 10kHz	±100 at 10kHz	MIL	TO-100	11-20
VFC32VM/883B	±10	200	±0.01 at 10kHz	−400, +150 at 200kHz	MIL	TO-100	11-20
VFC32VM	±10	200	±0.01 at 10kHz	−400, +150 at 200kHz	MIL	TO-100	11-20
VFC32UM/883B	±10	200	±0.01 at 10kHz	±150 at 10kHz	MIL	TO-100	11-20
VFC32UM	±10	200	±0.01 at 10kHz	±150 at 10kHz	MIL	TO-100	11-20

MULTIPLIERS								
Model	Accuracy at 25°C ±%, max	Accuracy at 125°C ±%, max	Feedthrough ±mV, max	Output Offset ±mV, max	Output V, mA, min	Operating Temperature Range(1)	Package	Page
4213WM/883B	1/2	4	50	25	±10, ±5	MIL	TO-100	11-151
4213WM	1/2	4	50	25	±10, ±5	MIL	TO-100	11-151
4213VM/883B	1	4	100	30	±10, ±5	MIL	TO-100	11-151
4213VM	1	4	100	50	±10, ±5	MIL	TO-100	11-151
4213UM/883B	1	2(2)	100	50	±10, ±5	MIL	TO-100	11-151
4213UM	1	2(2)	100	50	±10, ±5	MIL	TO-100	11-151

NOTES: (1) U grade specified temperature range is −25°C to +85°C; all others specified over MIL temp range. (2) At +85°C.

OPERATIONAL AMPLIFIERS												
		Offset Voltage										
Description	Model	at 25°C ±mV, max	drift ±μV/°C max	Bias Current nA, max	Bandwidth Unity Gain MHz, min	Slew Rate V/μsec, min	ts ±0.01% nsec	Compen-sation	Output V, mA, min	Opera-ting Temp. Range(1)	Package	Page
Wideband	OPA600VM/883B	2	20	−100pA	5000, (3) A = 1000	400	125	external	±10, ±200	MIL	16-pin DIP	11-94
	OPA600VM	2	20	−100pA		400	125	external	±10, ±200	MIL		11-94
	OPA600UM/883B	5	80	−100pA		400	150	external	±10, ±200	MIL		11-94
	OPA600UM	5	80	−100pA		400	150	external	±10, ±200	MIL		11-94
General Purpose Bipolar	3500R/883B	5	20	±30	1	0.6	—	internal	±10, ±10	MIL	TO-99	11-132
	3500U/883B	5	20(2)	±30	1	0.6	—	internal	±10, ±10	MIL	TO-99	11-132
Precision Bipolar	3510VM/883B	0.12	2	±25	0.25	0.5	—	internal	±10, ±10	MIL	TO-99	11-143
Low Drift, Low Bias	OPA105WM/883B	.250	2	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105WM	.250	2	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105VM/883B	.250	5	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105VM	.250	5	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105UM/883B	.250	15(2)	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105UM	.250	15(2)	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74

OPERATIONAL AMPLIFIERS (continued)												
Description	Model	Offset Voltage at 25°C ±mV, max	Offset Voltage drift ±µV/°C max	Bias Current nA, max	Bandwidth Unity Gain MHz, min	Slew Rate V/µsec, min	ts ±0.01% nsec	Compensation	Output V, mA, min	Operating Temp. Range(1)	Package	Page
Ultra Low Bias Current	OPA106WM/883B	.250	5	−100fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106WM	.250	5	−100fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106VM/883B	.250	10	−150fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106VM	.250	10	−150fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106UM/883B	.250	20(2)	−300fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106UM	.250	20(2)	−300fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
Power	OPA8780VM/883B	10	30	−.05	5	15	—	internal	±30, ±60	MIL	TO-3	11-110
	OPA8780VM	10	30	−.05	5	15	—	internal	±30, ±60	MIL	TO-3	11-110
	OPA8780UM/883B	10	50	−.05	5	15	—	internal	±30, ±60	MIL	TO-3	11-110
	OPA8780UM	10	50	−.05	5	15	—	internal	±30, ±60	MIL	TO-3	11-110
High Power	●OPA8785UM	±10	±65	±40	1	1.5	—	internal	±20V, ±10A	MIL	TO-3	129
	●OPA8785UM/883B	±10	±65	±40	1	1.5	—	internal	±20V, ±10A	MIL	TO-3	129
	●OPA8785VM	±5	±40	±20	1	1.5	—	internal	±26V, ±10A	MIL	TO-3	129
	●OPA8785VM/883B	±5	±40	±20	1	1.5	—	internal	±26V, ±10A	MIL	TO-3	129

NOTES: (1) U grade specified temperature range is −25°C to +85°C; all others specified over MIL temp range. (2) −25°C to +85°C. (3) Gain-bandwidth product.

INSTRUMENTATION AMPLIFIERS											
						Input Parameters					
Description	Model	Gain Range(1)	Gain Accuracy G = 100, 25°C max	Gain Drift G = 100 ppm/°C, typ	Non-linearity G = 100 max	CMR, DC to 60Hz, G = 10 1kΩ Unbal...min	Offset Voltage vs Temp G = 100 max (µV/°C)	Dynamic Response G = 100 ±3dB BW (kHz)	Temp Range (2)	Package	Page
Very High Accuracy	INA258WG/883B	1-1000	0.10	22	0.007	96dB	0.5	25	MIL	DIP	11-61
	INA258WG	1-1000	0.10	22	0.007	96dB	0.5	25	MIL	DIP	11-61
	INA258VG/883B	1-1000	0.10	22	0.007	96dB	1.0	25	MIL	DIP	11-61
	INA258VG	1-1000	0.10	22	0.007	96dB	1.0	25	MIL	DIP	11-61
	INA258UG/883B	1-1000	0.10	22	0.007	96dB	3.0	25	MIL	DIP	11-61
	INA258UG	1-1000	0.10	22	0.007	96dB	3.0	25	MIL	DIP	11-61
	INA258WL/883B	1-1000	0.10	22	0.007	96dB	0.5	25	MIL		11-61
	INA258WL	1-1000	0.10	22	0.007	96dB	0.5	25	MIL	20-	11-61
	INA258VL/883B	1-1000	0.10	22	0.007	96dB	1.0	25	MIL	terminal	11-61
	INA258VL	1-1000	0.10	22	0.007	96dB	3.0	25	MIL	leadless	11-61
	INA258U./883B	1-1000	0.10	22	0.007	96dB	3.0	25	MIL	chip	11-61
	INA258UL	1-1000	0.10	22	0.007	96dB	3.0	25	MIL	carrier	11-61

NOTES: (1) Set with external resistor. (2) U grade specified temperature range is −25°C to +85°C; all others specified over MIL temperature range.

MICROCOMPUTER I/O SYSTEMS

Products in this *Supplement* are indicated by a ● next to model numbers; others are in the *Product Data Book.*

This full line of µC compatible I/O boards is available off-the-shelf. Design features let you put your microcomputer-based system together fast, using these analog and digital I/O's that offer: simple software requirements; memory-mapped designs; up to 64 input channels per board; analog inputs and outputs on the same board; 8- or 12-bit resolutions; software programmable gains; relay outputs; isolated digital I/O. Plug compatible with Intel, DEC, National, Motorola, Rockwell, Synertek, and others.

MULTIBUS™ ANALOG I/O									
			Inputs			Number Channels			
Model	Analog Input	Analog Output	High Level	Low Level	Analog Resolution (bits)	Input	Output	Features	Page
MP8305		●	●		12		4	Individual D/A converters	14-45
MP8316-V		●	●		12		16	Low cost per channel	14-49
MP8316-I		●			12		16	0 to 25mA inputs	14-49
MP8418	●		●	●	12	15 DIF/31 SE		Resistor programmable gain	14-51
MP8418-AO	●	●	●	●	12	15 DIF/31 SE	2	Resistor programmable gain	14-51
MP8418-PGA	●		●	●	12	15 DIF/31 SE		Software programmable gain	14-51
MP8418-PGA-AO	●	●	●	●	12	15 DIF/31 SE	2	Software programmable gain	14-51
MP8418-EXP	(1)		(1)	(1)	(1)	48 DIF/96 SE		Analog input expander	14-55
MP8430	●		●	●	12	16 DIF		RTD excitation	14-58
MP8450	●		●	●	12	16 DIF		900V transformer isolated	14-60
MP8616	●		●	●	8	16 SE		Low cost	14-69

NOTE: (1) Must be used with MP8418, MP8418-AO, MP8418-PGA or MP8418-PGA-AO which govern MP8418-EXP performance.

Multibus™ Intel Corp.

MULTIBUS™ DISCRETE I/O						
Model	Digital Input	Digital Output	Number Channels	Isolated	Features	Page
MP801		●	16	●	Relay output	14-8
MP802		●	32	●	Relay output	14-8
MP810	●		24	●	Contact closure input	14-10
MP810-NS	●		24	●	Voltage input	14-10
MP810-LV	●		24	●	Low voltage inputs	14-10
MP810-AC	●		24	●	AC sense inputs	14-10
MP810-DB	●		24	●	Debounce circuit	14-10
MP820-05	●		5	●	Count to 65,536	14-12
MP820-15	●		15	●	Count to 65,536	14-12
MP821-05	●		5	●	Time measurement	14-12
MP821-15	●		15	●	Time measurement	14-12
MP830-72	●	●	72		Output read back	14-13
MP830-72R	●	●	72		Input terminators	14-13
●MP840	●		24	●	Sequence of event detection	62

MULTIBUS™ BOARD			
Model	Function	Description	Page
●MP85188	CPU	Single-board computer with 80188-3, 16 JEDEC memory sockets, 8k RAM supplied, dual RS-232C ports, 24 parallel TTL I/O, 3 counters, watchdog timer, user-definable features.	64

NOTES: (1) Must be used with MP8418, MP8418-AO, MP8418-PGA or MP8418-PGA-AO which govern MP8418-EXP performance.

Multibus™ Intel Corp.

MOTOROLA MICROMODULES ANALOG I/O									
			Inputs		Analog Resolution (bits)	Number Channels			
Model	Analog Input	Analog Output	High Level	Low Level		Input	Output	Features	Page
MP7105		●			12		4	General purpose	14-33
MP7209	●		●	●	12	8 DIF		General purpose	14-37
MP7217	●		●	●	12	16 SE		General purpose	14-37
MP7218	●		●	●	12	16 SE		Low cost	14-37
MP7432	●		●	●	8	32 DIF/64 SE		Low cost	14-39
MP7432-AO	●	●	●	●	8	32 DIF/64 SE	2	Low cost	14-39
MP7504		●			8		4	Isolated-fused outputs	14-41
MP7608-I	●		●		12	8 DIF		Fused inputs	14-43

MOTOROLA MICROMODULES DIGITAL I/O						
Model	Digital Input	Digital Output	Number Channels	Isolated	Features	Page
MP702		●	32	●	Reed relays	14-4
MP710	●		24	●	Dry contact closures	14-6
MP710-NS	●		24	●	Wet contact closures	14-6

DEC Q-BUS ANALOG I/O									
			Inputs		Analog Resolution (bits)	Number Channels			
Model	Analog Input	Analog Output	High Level	Low Level		Input	Output	Features	Page
MP1104		●			12		4	Individual D/A converters	14-14
MP1216	●		●	●	12	32 SE/16DE		Resistor programmable gain	14-16
MP1216-PGA	●		●	●	12	32 SE/16DE		Software programmable gain	14-16

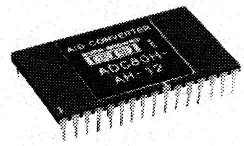
VMEBUS ANALOG I/O									
			Inputs		Analog Resolution (bits)	Number Channels			
Model	Analog Input	Analog Output	High Level	Low Level		Input	Output	Features	Page
MPV901	●		●	●	12	16DIF/32SE		Resistor programmable gain	14-72
MPV901A	●	●	●	●	12	16DIF/32SE	2	Resistor programmable gain	14-72
MPV901P	●	●	●	●	12	16DIF/32SE	2	Software programmable gain	14-72
MPV950S	●		●		12	16SE		High speed 3μsec throughput	14-84
MPV950D	●		●		12	8DIF/8SE		High speed 3μsec throughput	14-84
●MPV904		●			12		16	Voltage output	69
●MPV905		●			12		8	Current output selectable from 0-20-mA, 4-20mA, 5-25mA	71
●MPV960	●		●		12	4SE		4-channel analog input card with TMS320 DSP chip on-board	77

VMEBUS DIGITAL SIGNAL PROCESSING BOARD			
Model	Function	Description	Page
• SPV100	General Purpose DSP	DSP board based on TM5320 processor. Board incorporates two 4k × 16-bit swinging buffer data memories and two program memories (4k × 16-bit PROM and a 4k × 16-bit RAM). Applications include spectrum analysis, digital filtering, correlation, etc.	186

VMEBUS DISCRETE I/O						
Model	Digital Input	Digital Output	Number Channels	Isolated	Comments	Page
• MPV902		•	32	•	Relay output	67
• MPV910	•		32	•	Contact closure input	73
• MPV910-NS	•		32	•	Voltage input	73
• MPV910-LV	•		32	•	Low voltage input	73
• MPV930-48	•	•	48		TTL, output readback	75

BURR-BROWN®

ADC80H



General Purpose
ANALOG-TO-DIGITAL CONVERTER

FEATURES

- PIN-COMPATIBLE WITH INDUSTRY STANDARD ADC80
- <600mW POWER DISSIPATION
- 15μsec CONVERSION TIME WITH EXTERNAL CLOCK
- 25μSEC MAXIMUM CONVERSION TIME
- ±0.012% INTEGRAL LINEARITY
- 12-BIT RESOLUTION
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- NO MISSING CODES −25°C TO +85°C
- PARALLEL AND SERIAL OUTPUTS
- 32-PIN HERMETIC PACKAGE

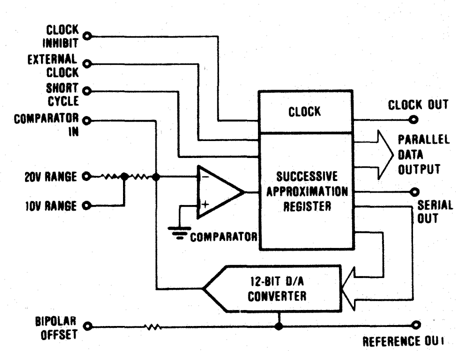
DESCRIPTION

The ADC80H is a 12-bit successive-approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom designed for freedom from latch-up and optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.012% (±1/2LSB). Like the industry standard ADC80, the ADC80H is completely specified for −25°C to +85°C operation.

The maximum conversion time of 25μsec makes the ADC80H ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, the ADC80H may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80H operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike other ADC80-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.



International Airport Industrial Park · P.O. Box 11400 · Tucson, Arizona 85734 · Tel. (602) 746-1111 · Twx: 910-952-1111 · Cable: BBRCORP · Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

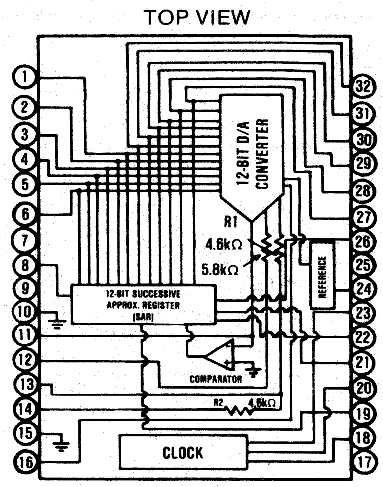
$T_A = +25°C$, $\pm V_{CC} = 12V$ or $15V$, $V_{DD} = +5V$ unless otherwise specified.

MODEL	ADC80H-AH-12			
	MIN	**TYP**	**MAX**	**UNITS**
RESOLUTION			12	Bits
INPUT				
ANALOG				
Voltage Ranges: Unipolar		0 to +5, 0 to +10		V
Bipolar		±2.5, ±5, ±10		V
Impedance: 0 to +5V, ±2.5V		2.3		kΩ
0 to +10V, +5V		4.6		kΩ
±10V		9.2		kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2.0		5.5	V
V_{IL} (Logic "0")	−0.3		+0.8	V
I_{IH} ($V_{IN} = +2.7V$)			−150	μA
I_{IL} ($V_{IN} = +0.4V$)			500	μA
Convert Command Pulse Width[1]	100		2000	nsec
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error[2]		±0.1	±0.3	% of FSR[3]
Offset Error[2]: Unipolar		±0.05	±0.2	% of FSR
Bipolar		±0.1	±0.3	% of FSR
Linearity Error			±0.012	% of FSR
Differential Linearity Error			±3/4	LSB
Inherent Quantization Error		1/2		LSB
POWER SUPPLY SENSITIVITY				
$+13.5V \leq +V_{CC} \leq +16.5V$ or $+11.4V \leq +V_{CC} \leq +12.6V$		±0.003	±0.009	% of FSR/%V_{CC}
$-16.5V \leq -V_{CC} \leq -13.5V$ or $-12.6V \leq -V_{CC} \leq -11.4V$		±0.003	±0.009	% of FSR/%V_{CC}
$+4.5V \leq V_{DD} \leq +5.5V$		±0.002	±0.005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar[4]		±10	±23	ppm/°C
Gain		±15	±30	ppm/°C
Offset: Unipolar		±3		ppm of FSR/°C
Bipolar		±7	±15	ppm of FSR/°C
Linearity Error Drift		±1	±3	ppm of FSR/°C
Differential Linearity over Temperature Range			±3/4	LSB
No Missing Code Temperature Range	−25		+85	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[5]	15	22	25	μsec
OUTPUT				
DIGITAL (Bits 1-12, Clock Out, Status, Serial Out)				
Output Codes[6]				
Parallel: Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ)[7]		CSB, COB		
Logic Levels: Logic 0 ($I_{sink} \leq 3.2mA$)			+0.4	V
Logic 1 ($I_{source} \leq 80\mu A$)	+2.4V			V
Internal Clock Frequency		545		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6.2	+6.3	+6.4	
Source Current Available for External Loads[8]	200			μA
Temperature Coefficient		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS				
Voltage, $\pm V_{CC}$	±11.4	±15	±16.5	V
V_{DD}	+4.5	+5.0	+5.5	V
Current, $+I_{CC}$		5	8.5	mA
$-I_{CC}$		21	26	mA
I_{DD}		11	15	mA
Power Dissipation ($\pm V_{CC} = 15V$)		450	595	mW
TEMPERATURE RANGE (Ambient)				
Specification	−25		+85	°C
Storage	−65		+150	°C

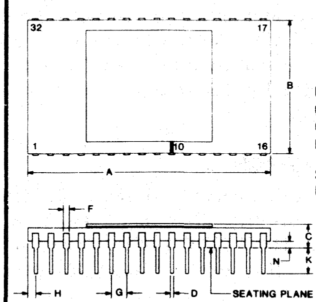
NOTES: (1) Accurate conversion will be obtained with any convert command pulse width of greater than 100nsec; however, it must be limited to 2μsec (max) to assure the specified conversion time. (2) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustments" section. (3) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (4) Includes drift due to linearity, gain, and offset drifts. (5) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time; see "Short Cycle Feature" section. (6) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table I for additional information. (7) NRZ means non-return-to-zero coding. (8) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specification.

CONNECTION DIAGRAM

Pin 1 - Bit 6	Pin 32 - Bit 7
Pin 2 - Bit 5	Pin 31 - Bit 8
Pin 3 - Bit 4	Pin 30 - Bit 9
Pin 4 - Bit 3	Pin 29 - Bit 10
Pin 5 - Bit 2	Pin 28 - Bit 11
Pin 6 - Bit 1 (MSB) with overbar	Pin 27 - Bit 12 (LSB)
Pin 7 - N/C	Pin 26 - Serial Out
Pin 8 - Bit 1 (MSB)	Pin 25 - $-V_{CC}$
Pin 9 - +5V Digital Supply	Pin 24 - Ref. Out (+6.3V)
Pin 10 - Digital Common	Pin 23 - Clock Out
Pin 11 - Comparator In	Pin 22 - Status
Pin 12 - Bipolar Offset	Pin 21 - Short Cycle
Pin 13 - R1 10V Range	Pin 20 - Clock Inhibit
Pin 14 - R2 20V Range	Pin 19 - External Clock
Pin 15 - Analog Common	Pin 18 - Convert Command
Pin 16 - Gain Adjust	Pin 17 - $+V_{CC}$



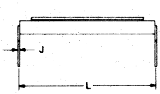
MECHANICAL



Leads in true position within .010" (.25MM) R at MMC at Seating Plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

S/R is connected to Pin 10.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

CASE: Ceramic, hermetic
MATING CONNECTOR: 2302MC
WEIGHT: 7.3gm (0.26oz)

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common .... 0 to +16.5V
$-V_{CC}$ to Analog Common .... 0 to −16.5V
V_{DD} to Digital Common .... 0 to +7V
Analog Common to Digital Common .... ±0.5V
Logic Inputs (Convert Command, Clock In)
to Digital Common .... −0.3V to V_{DD} +0.5V
Analog Inputs (Analog In, Bipolar Offset)
to Analog Common .... ±16.5V
Reference Output .... Indefinite Short to Common, Momentary Short to V_{CC}
Power Dissipation 1000mW
Lead Temperature, Soldering .... +300°C, 10sec
Thermal Resistance, θ_{JA} .... 60°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers.

The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1 which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

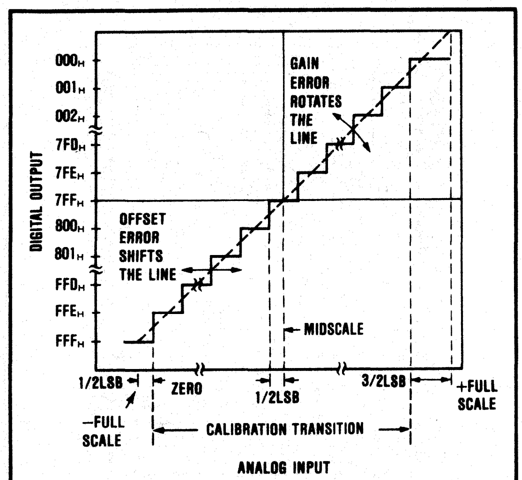


FIGURE 1. ADC80H Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC80H analog input signal range are described in Table I.

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88V. Refer to Table I for LSB values for other ADC80H input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is a definition of the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. ADC80H is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC80H connected for uniplolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC80H follows this convention. Thus, bipolar offset error for the ADC80H is

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB* or CTC**	COB or CTC	COB or CTC	CSB***	CSB
One Least Significant Bit (LSB)	$FSR/2^n$ n = 8 n = 10 n = 12	$20V/2^n$ 78.13mV 19.53mV 4.88mV	$10V/2^n$ 39.06mV 9.77mV 2.44mV	$5V/2^n$ 19.53mV 4.88mV 1.22mV	$10V/2^n$ 39.06mV 9.77mV 2.44mV	$5V/2^n$ 19.53mV 4.88mV 1.22mV
Transition Values MSB LSB 001_H to 000_H 800_H to $7FF_H$ FFF_H to FFE_H	 +Full Scale Mid Scale −Full Scale	 +10V − 3/2LSB 0 −10V + 1/2LSB	 +5V − 3/2LSB 0 −5V + 1/2LSB	 +2.5V − 3/2LSB 0 −2.5V + 1/2LSB	 + 10V − 3/2LSB +5V 0 + 1/2LSB	 +5V − 3/2LSB + 2.5V 0 + 1/2LSB

*COB = Complementary Offset Binary **CTC = Complementary Two's Complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.
***CSB = Complementary Straight Binary

defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the specification range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

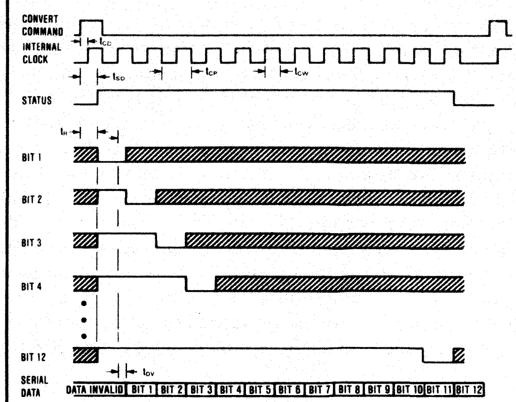
Electrical specifications for the ADC80H assume the application of the rated power supply voltages of+5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

TIMING CONSIDERATIONS

Timing relationships of the ADC80H are shown in Figure 2. It should be noted that although the convert command pulse width must be between 100nsec and 2μsec to obtain the specified conversion time with internal clock, the ADC80H will accept longer convert commands with no loss of accuracy, assuming that the analog input signal is stable.In this situation, the actual indicated conversion time (during which status is high) for 12-bit operation will be equal to approximately 1μsec less than the sum of the factory-set conversion time and the length of the convert command. The code returned by the converter at the end of the conversion will accurately represent the analog input to the converter at the time the convert command returns to the low state. In addition, although the initial state of the converter will be indeterminate when power is first applied, it is designed to time-out and be ready to accept a convert command within approximately 25μsec after power-up, provided that either an external clock source is present or the internal clock is not inhibited.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse "n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the rising edge of the 13th clock pulse, and with valid output data ready to be read at that time. A new conversion may not be initiated until 50nsec after the fall of the last clock pulse (pulse 13 for 12-bit operation).

Additional convert commands applied during conversion will be ignored.



Symbol	Parameter	Typ.	Units
t_{CD}	Clock delay from convert command	30	nsec
t_{CP}	Nominal clock period	1.65	μsec
t_{CW}	Nominal clock pulse width	0.65	μsec
t_{SD}	Status delay from convert command	130	nsec
t_R	All bits reset delay from convert command	65	nsec
t_{DV}	Data valid time from clock pulse high	−35	nsec

FIGURE 2. ADC80H Timing Diagram (nominal values at +25°C with internal clock).

DEFINITION OF DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC80H parallel output; all three are complementary codes, meaning that logic "0" is true. The available codes are complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) and complementary two's complement (CTC) for bipolar input signal ranges. CTC coding is obtained by complementing bit 1 (the MSB) relative to its normal state for CSB or COB coding; the complement of bit 1 is available on pin 8.

Serial Data

Two (complementary) straight binary codes are available on the serial output of the ADC80H; as in the parallel case, they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values of Table I also apply to the serial data output, except that the CTC code is not available. All clock pulses available from the ADC80H have equal pulse widths to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC80H, but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC80H as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC80H will be driving into a nominal DC input impedance of 2.3kΩ to 9.2kΩ depending upon the range selected. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC80H offers five standard input ranges: 0V to +5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. Use of external padding resistors to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range) will require matching of the external fixed resistor values to individual devices, due to the large tolerance of the internal input resistors. Alternatively, the gain range of the converter may easily be increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by the decreasing the value of the gain adjust series resistor in Figure 5.

TABLE II. ADC80H Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

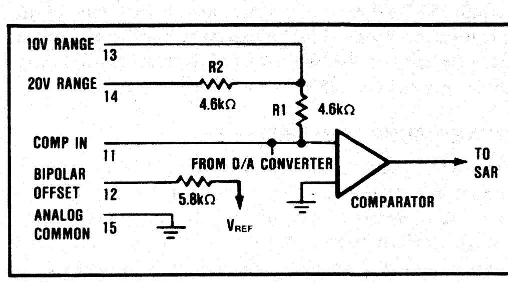


FIGURE 3. ADC80H Input Scaling Circuit.

CALIBRATION

Optional External Gain And Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC80H as shown in Figures 4 and 5 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These

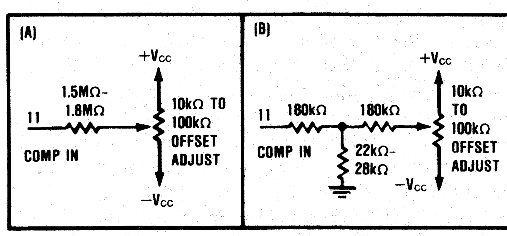


FIGURE 4. Two Methods of Connecting Optional Offset Adjust.

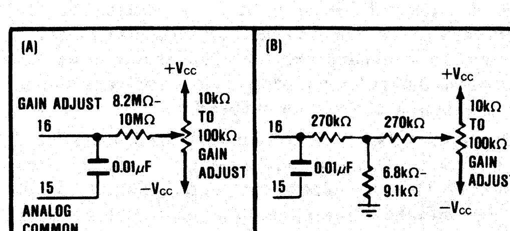


FIGURE 5. Two Methods of Connecting Optional Gain Adjust.

pots may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 16 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 4. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V +2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE_H and FFF_H with approximately 50% occurence of each of the two codes. In other words, the potentiometer is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 5. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V −7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transition to a precisely known value.

CLOCK OPTIONS

The ADC80H is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with inexpensive TTL logic as shown in Figures 6 through 9. When operating with an external clock, the conversion time may be as short as 15μsec (800kHz external clock frequency) with assured performance within specified limits. When operating with the internal clock, pin 19 (external clock input) and pin 20 (clock inhibit) may be left unconnected. No external pull-ups are required due to the inclusion of pull-up resistors in the ADC80H. Pin 20 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 19.

SHORT-CYCLE FEATURE

A short-cycle input (pin 21) permits the conversion to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applica-

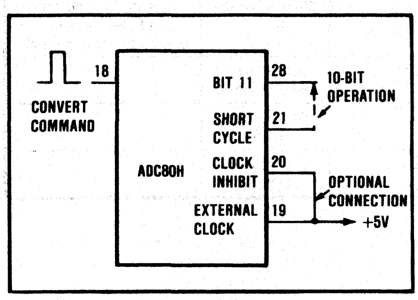


FIGURE 6. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

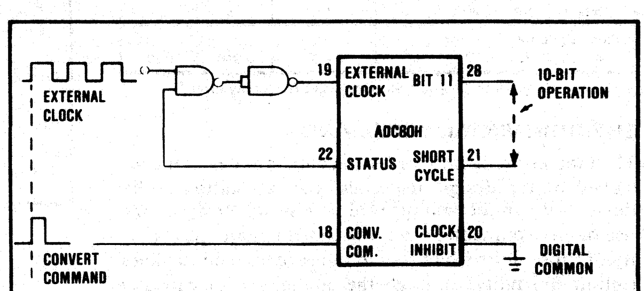


FIGURE 7. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

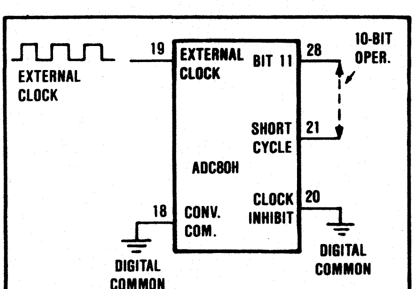


FIGURE 8. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

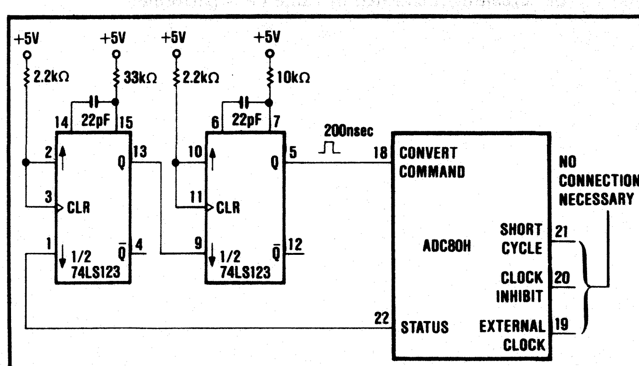


FIGURE 9. Continuous Conversion with 600nsec between Conversions. (Circuit insures that conversion will start when power is applied.)

tions not requiring full 12-bit resolution. In these situations, the short-cycle pin should be connected to the bit output pin of the next bit after the desired resolution. For example, when 10-bit resolution is desired, pin 21 is connected to pin 28 (bit 11). In this example, the conversion cycle terminates and status is reset after the bit 10 decision. Short-cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times (with internal clock) are shown in Table III. Also shown are recommended minimum conversion times (external clock) for these conversion lengths to obtain the stated accuracies. The ADC80H is not factory-tested for these external clock conversion speeds and the product is not guaranteed to achieve the stated accuracies under these operating conditions; the recommended values are offered as an aid to the user.

TABLE III. Short-Cycle Connections and Conversion Times for 8-, 10-, and 12-Bit Resolutions—ADC80H.

Resolution (Bits)	**12**	**10**	**8**
Connect pin 21 to	Pin 9 or NC	Pin 28	Pin 30
Maximum Conversion Time(1) Internal Clock (μsec)	25	22	18
Minimum Conversion Time(1) External Clock (μsec)	15	13	10
Maximum Linearity Error At +25°C (% of FSR)	0.012	0.048	0.20

NOTE: (1) Conversion time to maintain ±1/2LSB linearity error.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table IV is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE IV. Screening Flow for ADC80H-AH-12Q

Screen	**MIL-STD-883 Method, Condition**	**Screening Level**
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-in	1015, B	160 hour, +125°C, steady-state
Hermeticity: Fine Leak Gross Leak	1014, A1 or A2 1014, C	5×10^{-7} atm cc/sec bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	Burr-Brown QC5150	

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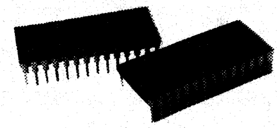
ADC574A



Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE**
- **IMPROVED PERFORMANCE SECOND SOURCE FOR 574A-TYPE A/D CONVERTERS**
  - **25μsec Maximum Conversion Time**
  - **150nsec Bus Access Time**
  - **A_0 Input: Bus Contention During Read Operation Eliminated**
- **FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES**
- **NO MISSING CODES OVER TEMPERATURE**
  - **0°C to +75°C: ADC574AJH, KH Grades**
  - **−55°C to +125°C: ADC574ASH, TH Grades**

DESCRIPTION

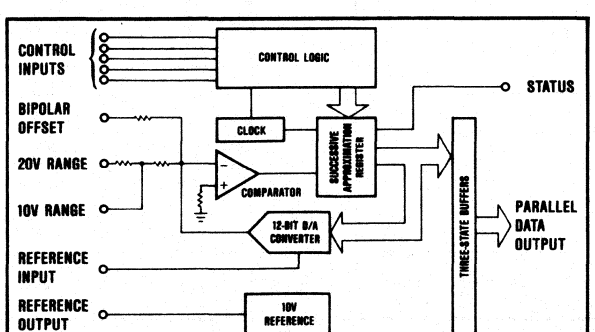
The ADC574A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally-trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 20μsec typical.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC574A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a hermetic 28-pin side-brazed ceramic DIP.



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SPECIFICATIONS

ELECTRICAL

$T_A = +25°C$, $V_{CC} = +12V$ or $+15V$, $V_{EE} = -12V$ or $-15V$, $V_{LOGIC} = +5V$ unless otherwise specified.

MODEL	ADC574AJH, ADC574ASH			ADC574AKH, ADC574ATH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			*	Bits
INPUT							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			*		V
Bipolar		±5, ±10			*		V
Impedance: 0 to +10V, ±5V	3.7	5	6.3	*	*	*	kΩ
±10V, 0V to +20V	7.5	10	12.5	*	*	*	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2.4[1]		+5.5	*		*	V
Logic 0	−0.5		+0.8	*		*	V
Current	−5	0.1	+5	*	*	*	μA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			*	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error[2] (adjustable to zero)			±0.3			*	% of FS[3]
No Missing Codes Resolution	11			12			Bits
Inherent Quantization Error		±1/2			*		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	% of FS
S, T Grades			±1			*	% of FS
Full-Scale Calibration Error							
Without Initial adjustment[2]: J, K Grades			±0.5			±0.4	% of FS
S, T Grades			±0.8			±0.6	% of FS
Adjusted to zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution	11			12			Bits
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
$+13.5V < V_{CC} < +16.5V$ or $+11.4V < V_{CC} < +12.6V$			±2			±1	LSB
$-16.5V < V_{EE} < -13.5V$ or $-12.6V < V_{EE} < -11.4V$			±2			±1	LSB
$+4.5V < V_{LOGIC} < +5.5V$			±1/2			*	LSB
CONVERSION TIME[4]							
8-Bit Cycle	10	13	17	*	*	*	μsec
12-Bit Cycle	15	20	25	*	*	*	μsec
DRIFT							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Change over Temperature Range, All Grades			±2			±1	LSB
Bipolar Offset, All Grades			±10			±5	ppm/°C
Change over Temperature Range: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Change over Temperature Range: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
OUTPUT							
DIGITAL ($DB_{11} - DB_0$, STATUS)							
Over Temperature Range							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 ($I_{sink} = 1.6mA$)			+0.4			*	V
Logic 1 ($I_{source} = 500\mu A$)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	*	*	*	μA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10.1	*	*	*	V
Source Current Available for External Loads[5]	2.0			*			mA

ELECTRICAL (CONT)

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC574AJH, ADC574ASH			ADC574AKH, ADC574ATH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	−11.4		−16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		11	15		*	*	mA
I_{EE}		21	28		*	*	mA
I_{LOGIC}		7	15		*	*	mA
Power Dissipation (±15V Supplies)		515	720		*	*	mW
TEMPERATURE RANGE (Ambient)							
Specification: J, K Grades	0		+75	*		*	°C
S, T Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

*Same specification as grade to the immediate left.

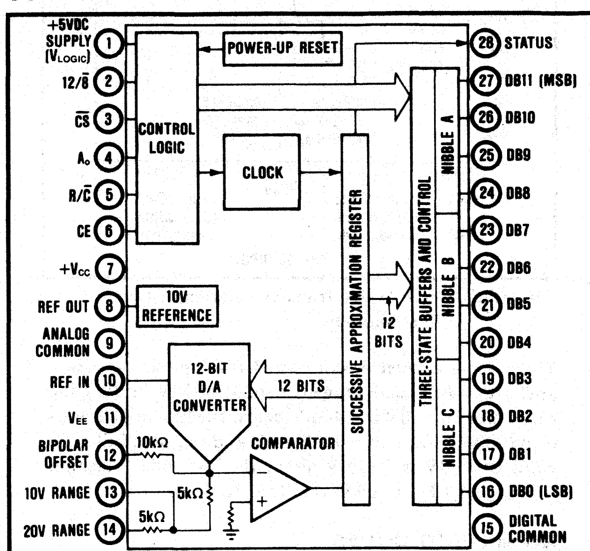
NOTES: (1) Although this guaranteed threshold is higher than the standard TTL guaranteed level (+2.0V), bus loading is much less. Typical input current is only 0.25% of a standard TTL load. (2) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C (see "Optional External Full Scale and Offset Adjustments" section). (3) FS in this specification table means Full-Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. Use of the term Full Scale for these specifications instead of Full-Scale Range is consistent with other vendors' 574 and 574A specification tables. (4) See "Controlling the ADC574A" section for detailed information concerning digital timing. (5) External loading must be constant during conversion. When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the reference output.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common .... 0 to +16.5V
V_{EE} to Digital Common .... 0 to −16.5V
V_{LOGIC} to Digital Common .... 0 to +7V
Analog Common to Digital Common .... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)
to Digital Common .... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$)
to Analog Common .... ±16.5V
$20V_{IN}$ to Analog Common .... ±24V
REF OUT .... Indefinite Short to Common, Momentary Short to V_{CC}
Chip Temperature: J, K, L Grades .... +100°C
S, T, U Grades .... +150°C
Power Dissipation 1000mW
Lead Temperature, Soldering .... +300°C, 10sec
Thermal Resistance, θ_{JA} .... 48°C/W

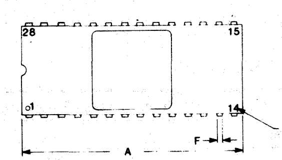
CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

CONNECTION DIAGRAM



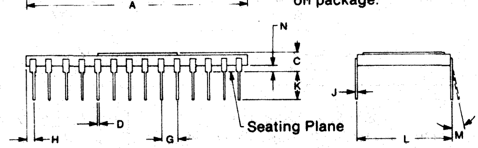
MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.386	1.414	35.20	35.92
C	.108	.166	2.74	4.22
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	– –	10°	– –	10°
N	.025	.060	0.64	1.52



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



CASE: Ceramic, hermetic
MATING CONNECTOR: 2803MC
WEIGHT: 4.8 grams (0.17oz.)

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).

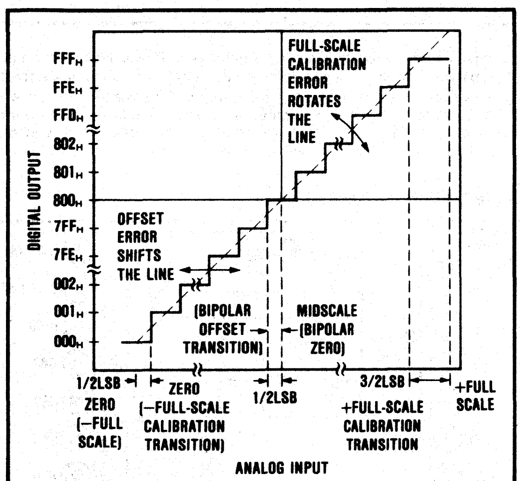


FIGURE 1. ADC574A Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of −10V is 2.44mV below the first code transition (000_H to 001_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table I).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur.

ADC57A KH and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An ADC574A connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC574A specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC574A is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC574A assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply

TABLE I. Input Voltages, Transition Values, and LSB Values.

Binary (BIN) Output	Input Voltage Range and LSB Values				
Analog Input Voltage Range	Defined As:	±10V	±5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$ n = 8 n = 12	$\frac{20V}{2^n}$ 78.13mV 4.88mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{20V}{2^n}$ 78.13mV 4.88mV
Output Transition Values FFE_H to FFF_H $7FFF_H$ to 800_H 000_H to 001_H	+ Full-Scale Calibration Midscale Calibration (Bipolar Offset) Zero Calibration (− Full-Scale Calibration)	+10V − 3/2LSB 0 − 1/2LSB −10V + 1/2LSB	+5V − 3/2LSB 0 − 1/2LSB −5V + 1/2LSB	+10V − 3/2LSB +5V − 1/2LSB 0 + 1/2LSB	+20V − 3/2LSB +10V −1/2LSB 0 + 1/2LSB

voltage deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given otuput code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC574A, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. This single common path will typically carry about 1.5mA of current out of the converter. Code-dependent currents do not flow in analog (pin 9) or digital (pin 15) commons. DC currents that flow are typically +7mA in pin 9 and −5.5mA in pin 15.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC574A as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC574A will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 200Ω potentiometer in series with pin 13 for the 10.24V range, or a 500Ω potentiometer in series with pin 14 for the 20.48V range. Use a fixed 50Ω, 1% resistor for R_2 (Figures 2 and 3). Offset adjustment is still performed as described below. Full-scale adjustment is performed as described below but with adjustment performed using the input potentiometer instead of R_2.

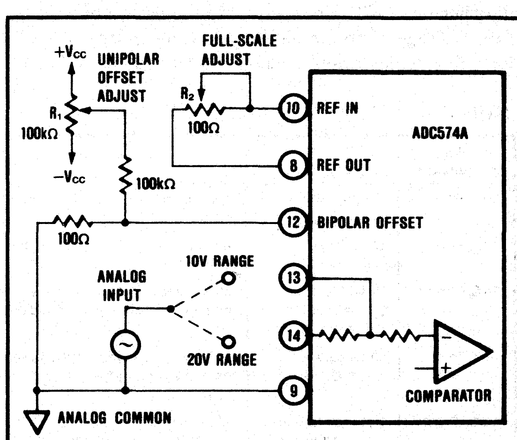


FIGURE 2. Unipolar Configuration.

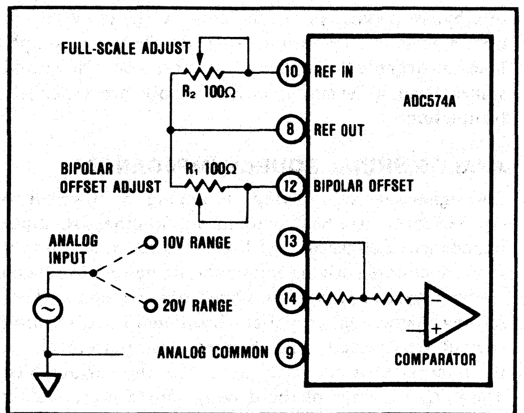


FIGURE 3. Bipolar Configuration.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC574A as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE— UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (high). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1–DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (−4.9988V for the ±5V range, −9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

CONTROLLING THE ADC574A

The Burr-Brown ADC574A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the $R/\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/8, $\overline{CS}$, A_0, $R/\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to $R/\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and $12/\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The

TABLE II. ADC574A Control Line Functions.

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
$R/\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
$12/\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, $12/\overline{8}$ = "1" enables all 12 output bits simultaneously. $12/\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

TABLE III. Control Input Truth Table.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_o	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50nsec.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the ouptut data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Table IV lists timing specifications for stand-alone operation.

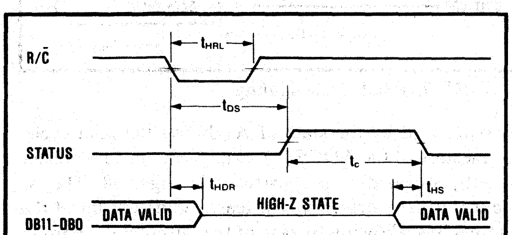


FIGURE 4. R/$\overline{C}$ Pulse Low — Outputs Enabled After Conversion.

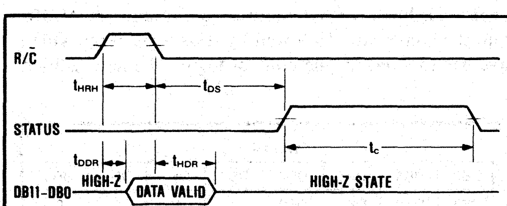


FIGURE 5. R/$\overline{C}$ Pulse High — Outputs Enabled Only While R/$\overline{C}$ Is High.

TABLE IV. Stand-Alone Mode Timing.

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			nsec
t_{DS}	STS Delay from R/$\overline{C}$			200	nsec
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			nsec
t_{HS}	STS Delay After Data Valid	300	500	1000	nsec
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			nsec
t_{DDR}	Data Access Time			150	nsec

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_o input, which is latched upon receipt of a conversion start transition (described below). If A_o is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_o is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0–DB2) will be low (logic 0) and DB3 will be high (logic 1). A_o is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50nsec prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

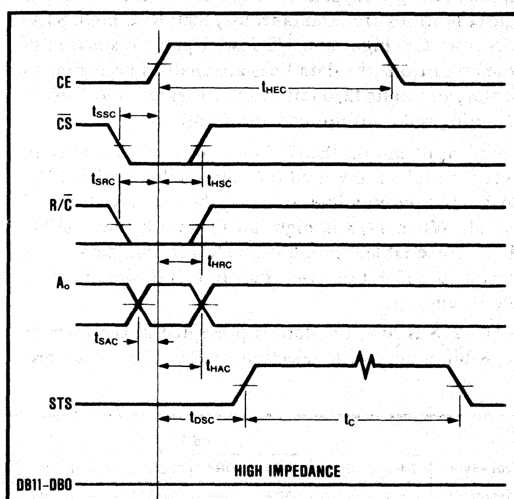


FIGURE 6. Conversion Cycle Timing.

TABLE V. Timing Specifications.

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS delay from CE		100	200	nsec
t_{HEC}	CE Pulse width	50	30		nsec
t_{SSC}	$\overline{CS}$ to CE setup	50	20		nsec
t_{HSC}	$\overline{CS}$ low during CE high	50	20		nsec
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		nsec
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		nsec
t_{SAC}	A_0 to CE setup	0	0		nsec
t_{HAC}	A_0 valid during CE high	50	20		nsec
t_c	Conversion time, 12 bit cycle	15	20	25	μsec
	8 bit cycle	10	13	17	μsec
Read Mode					
t_{DD}	Access time from CE		75	150	nsec
t_{HD}	Data valid after CE low	25	35		nsec
t_{HL}	Output float delay		100	150	nsec
t_{SSR}	$\overline{CS}$ to CE setup	50	0		nsec
t_{SRR}	R/$\overline{C}$ to CE setup	0	0		nsec
t_{SAR}	A_0 to CE setup	50	25		nsec
t_{HSR}	$\overline{CS}$ valid after CE low	0	0		nsec
t_{HRR}	R/$\overline{C}$ high after CE low	0	0		nsec
t_{HAR}	A_0 valid after CE low	50	25		nsec
t_{HS}	STS delay after data valid	300	500	1000	nsec

NOTE: Specifications are at +25°C and measured at 50% level of transitions.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0–DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest

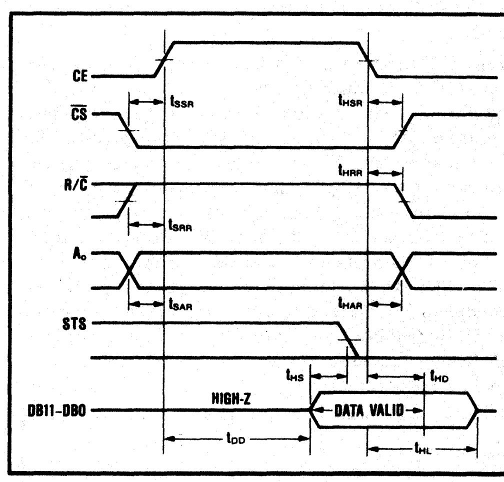


FIGURE 7. Read Cycle Timing.

accomplished by the state of A_0 during the read cycle. Connection of the ADC574A to an 8-bit bus for transfer of left-justified data is illustrated in Figure 8. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC574A guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as 1.15μsec (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Figure 7 for these timing relationships.

ORDERING INFORMATION

Model	Temperature Range	Linearity Error, max (T_{MIN} to T_{MAX})	Resolution, No Missing Codes (T_{MIN} to T_{MAX})	Full-Scale TC, max (ppm/°C)
ADC574AJH	0°C to +75°C	±1LSB	11 Bits	±45
ADC574AKH	0°C to +75°C	±1/2LSB	12 Bits	±25
ADC574ASH	−55°C to +125°C	±1LSB	11 Bits	±50
ADC574ATH	−55°C to +125°C	±1LSB	12 Bits	±25

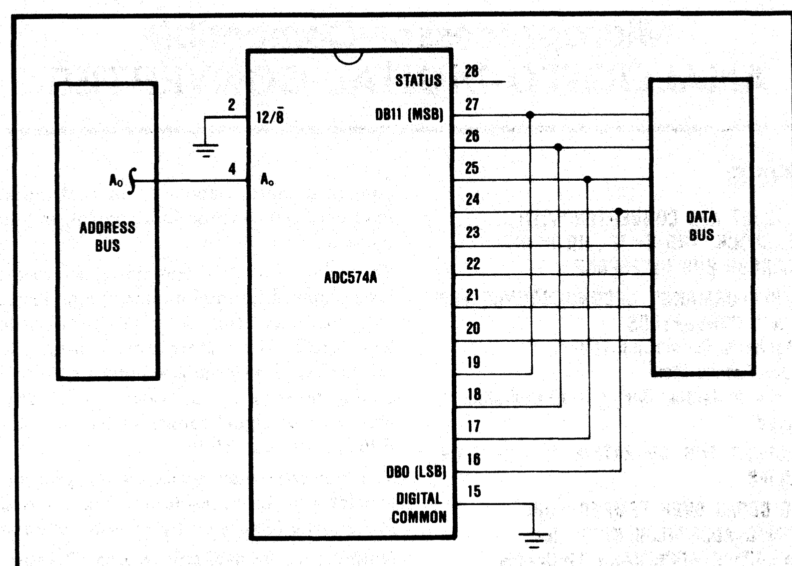
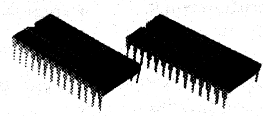


FIGURE 9. Connection to an 8-bit Bus.

BURR-BROWN®

ADC674A



Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE
- IMPROVED PERFORMANCE SECOND SOURCE FOR 574A-TYPE A/D CONVERTERS
  - 15μsec Maximum Conversion Time
  - 150nsec Bus Access Time
  - A_0 Input: Bus Contention During Read Operation Eliminated
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- NO MISSING CODES OVER TEMPERATURE
  - 0°C to +75°C: ADC674AJH, KH Grades
  - −55°C to +125°C: ADC674ASH, TH Grades

DESCRIPTION

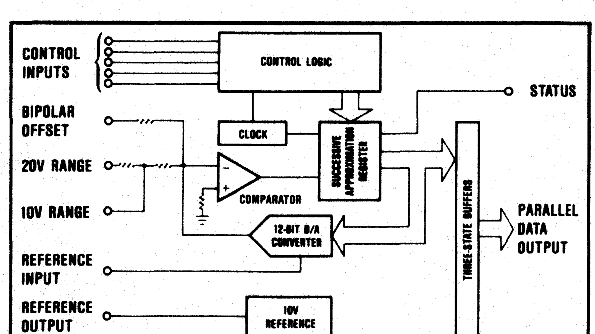
The ADC674A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally-trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 15μsec maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC574A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a hermetic 28-pin side-brazed ceramic DIP.



International Airport Industrial Park · P.O. Box 11400 · Tucson, Arizona 85734 · Tel. (602) 746-1111 · Twx: 910-952-1111 · Cable: BBRCORP · Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

$T_A = +25°C$, $V_{CC} = +12V$ or $+15V$, $V_{EE} = -12V$ or $-15V$, $V_{LOGIC} = +5V$ unless otherwise specified.

MODEL	ADC674AJH, ADC674ASH			ADC674AKH, ADC674ATH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			•	Bits
INPUT							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			•		V
Bipolar		±5, ±10			•		V
Impedance: 0 to +10V, ±5V	3.7	5	6.3	•	•	•	kΩ
±10V, 0V to +20V	7.5	10	12.5	•	•	•	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2.4[1]		+5.5	•		•	V
Logic 0	−0.5		+0.8	•		•	V
Current	−5	0.1	+5	•	•	•	μA
Capacitance		5			•		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			•	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error[2] (adjustable to zero)			±0.3			•	% of FS[3]
No Missing Codes Resolution	11			12			Bits
Inherent Quantization Error		±1/2			•		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			•	LSB
Full-Scale Calibration Error							
Without Initial adjustment[2]: J, K Grades			±0.5			±0.4	% of FS
S, T Grades			±0.8			±0.6	% of FS
Adjusted to zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution	11			12			Bits
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
$+13.5V < V_{CC} < +16.5V$ or $+11.4V < V_{CC} < +12.6V$			±2			±1	LSB
$-16.5V < V_{EE} < -13.5V$ or $-12.6V < V_{EE} < -11.4V$			±2			±1	LSB
$+4.5V < V_{LOGIC} < +5.5V$			±1/2			•	LSB
CONVERSION TIME[4]							
8-Bit Cycle	6	8	10	•	•	•	μsec
12-Bit Cycle	9	12	15	•	•	•	μsec
DRIFT							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Change over Temperature Range, All Grades			±2			±1	LSB
Bipolar Offset, All Grades			±10			±5	ppm/°C
Change over Temperature Range: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Change over Temperature Range: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
OUTPUT							
DIGITAL ($DB_{11} - DB_0$ STATUS)							
Over Temperature Range							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 ($I_{sink} = 1.6mA$)			+0.4			•	V
Logic 1 ($I_{source} = 500\mu A$)	+2.4			•			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	•	•	•	μA
Capacitance		5			•		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10.1	•	•	•	V
Source Current Available for External Loads[5]	2.0			•			mA

ELECTRICAL (CONT)

$T_A = +25°C$, $V_{CC} = +12V$ or $+15V$, $V_{EE} = -12V$ or $-15V$, $V_{LOGIC} = +5V$ unless otherwise specified.

MODEL	ADC674AJH, ADC674ASH			ADC674AKH, ADC674ATH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	−11.4		−16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		11	15		*	*	mA
I_{EE}		21	28		*	*	mA
I_{LOGIC}		7	15		*	*	mA
Power Dissipation (±15V Supplies)		515	720		*	*	mW
TEMPERATURE RANGE (Ambient)							
Specification: J, K Grades	0		+75	*		*	°C
S, T Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

*Same specification as grade to the immediate left.

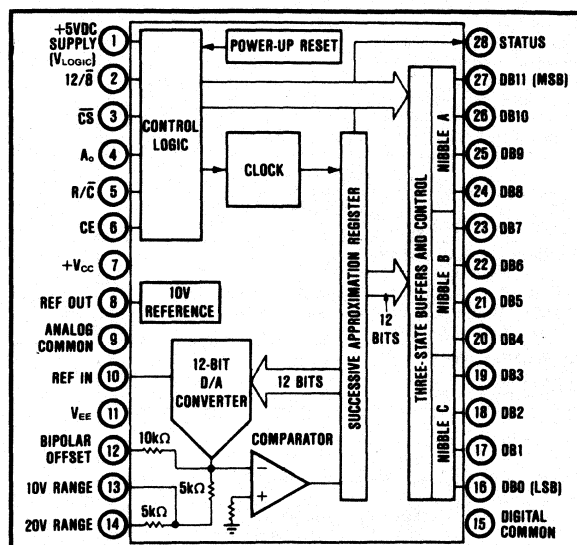
NOTES: (1) Although this guaranteed threshold is higher than the standard TTL guaranteed level (+2.0V), bus loading is much less. Typical input current is only 0.25% of a standard TTL load. (2) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C (see "Optional External Full Scale and Offset Adjustments" section). (3) FS in this specification table means Full-Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. Use of the term Full Scale for these specifications instead of Full-Scale Range is consistent with other vendors' 574 and 574A type specification tables. (4) See "Controlling the ADC674A" section for detailed information concerning digital timing. (5) External loading must be constant during conversion. When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the reference output.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common .... 0 to +16.5V
V_{EE} to Digital Common .... 0 to −16.5V
V_{LOGIC} to Digital Common .... 0 to +7V
Analog Common to Digital Common .... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)
to Digital Common .... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$)
to Analog Common .... ±16.5V•
$20V_{IN}$ to Analog Common .... ±24V
REF OUT .... Indefinite Short to Common, Momentary Short to V_{CC}
Chip Temperature: J, K Grades .... +100°C
S, T Grades .... +150°C
Power Dissipation 1000mW
Lead Temperature, Soldering .... +300°C, 10sec
Thermal Resistance, θ_{JA} .... 48°C/W

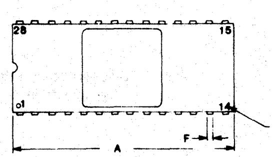
CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

CONNECTION DIAGRAM



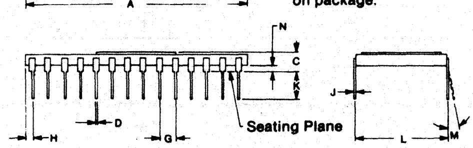
MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.386	1.414	35.20	35.92
C	.108	.166	2.74	4.22
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	- -	10°	- -	10°
N	.025	.060	0.64	1.52



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



CASE: Ceramic, hermetic
MATING CONNECTOR: 2803MC
WEIGHT: 4.8 grams (0.17oz.)

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).

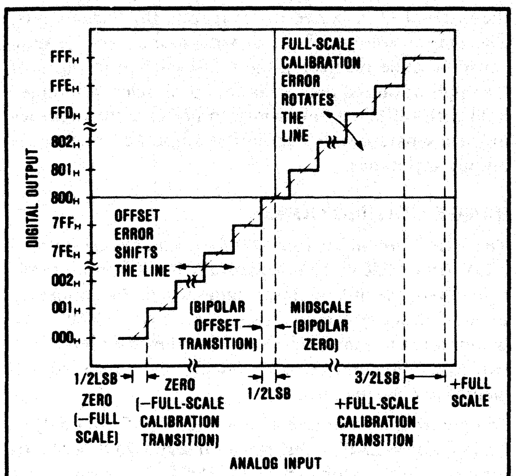


FIGURE 1. ADC674A Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of −10V is 2.44mV below the first code transition (000_H to 001_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table I).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur.

ADC674A KH and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An ADC674A connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC674A specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC674A is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC674A assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply

TABLE I. Input Voltages, Transition Values, and LSB Values.

Binary (BIN) Output	Input Voltage Range and LSB Values				
Analog Input Voltage Range	Defined As:	±10V	±5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$ n = 8 n = 12	$\frac{20V}{2^n}$ 78.13mV 4.88mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{20V}{2^n}$ 78.13mV 4.88mV
Output Transition Values FFE_H to FFF_H $7FFF_H$ to 800_H 000_H to 001_H	+ Full-Scale Calibration Midscale Calibration (Bipolar Offset) Zero Calibration (− Full-Scale Calibration)	+10V − 3/2LSB 0 − 1/2LSB −10V + 1/2LSB	+5V − 3/2LSB 0 − 1/2LSB −5V + 1/2LSB	+10V − 3/2LSB +5V − 1/2LSB 0 + 1/2LSB	+20V − 3/2LSB ±10V − 1/2LSB 0 + 1/2LSB

voltage deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC674A, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. This single common path will typically carry about 3mA of current out of the converter. Code-dependent currents do not flow in analog (pin 9) or digital (pin 15) commons. DC currents that flow are typically 6mA in pin 9 and −3mA in pin 15.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC674A as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC674A will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC674A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 200Ω potentiometer in series with pin 13 for the 10.24V range, or a 500Ω potentiometer in series with pin 14 for the 20.48V range. Use a fixed 50Ω, 1% resistor for R_2 (Figures 2 and 3). Offset adjustment is still performed as described below. Full-scale adjustment is performed as described below but with adjustment performed using the input potentiometer instead of R_2.

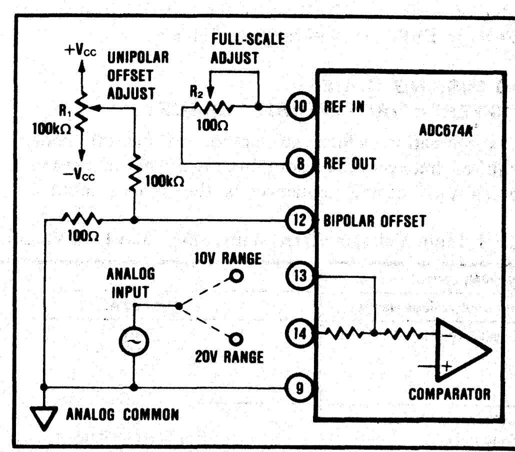


FIGURE 2. Unipolar Configuration.

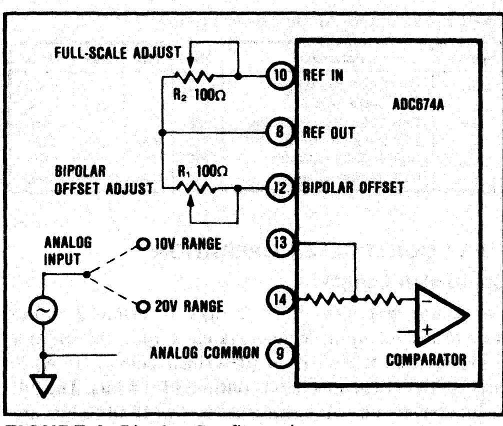


FIGURE 3. Bipolar Configuration.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC674A as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE—UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (high). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1–DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (−4.9988V for the ±5V range, −9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

CONTROLLING THE ADC674A

The Burr-Brown ADC674A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the $R/\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs ($12/\overline{8}$, $\overline{CS}$, A_0, $R/\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to $R/\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and $12/\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The

TABLE II. ADC674A Control Line Functions.

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
$R/\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
$12/\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, $12/\overline{8}$ = "1" enables all 12 output bits simultaneously. $12/\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

TABLE III. Control Input Truth Table.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50nsec.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/C. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

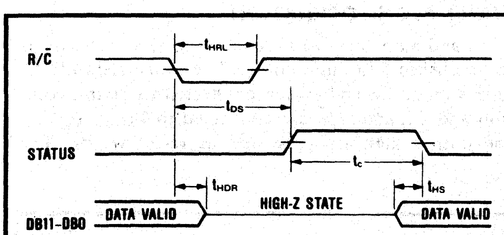


FIGURE 4. R/$\overline{C}$ Pulse Low — Outputs Enabled After Conversion.

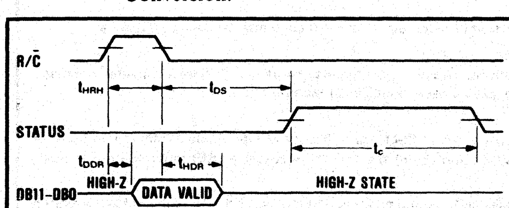


FIGURE 5. R/$\overline{C}$ Pulse High — Outputs Enabled Only While R/$\overline{C}$ Is High.

TABLE IV. Stand-Alone Mode Timing.

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			nsec
t_{DS}	STS Delay from R/$\overline{C}$			200	nsec
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			nsec
t_{HS}	STS Delay After Data Valid	100	300	600	nsec
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			nsec
t_{DDR}	Data Access Time			150	nsec

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0–DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50nsec prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

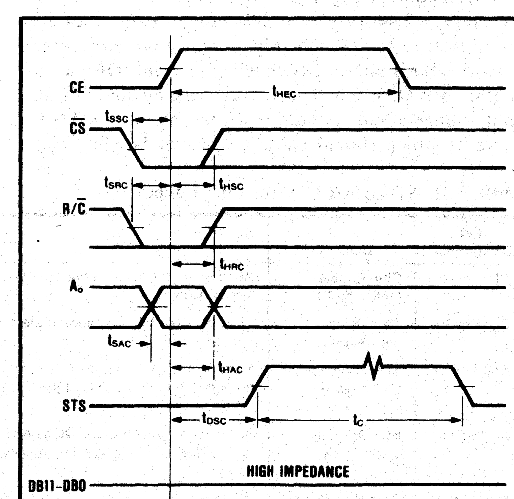


FIGURE 6. Conversion Cycle Timing.

TABLE V. Timing Specifications.

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS delay from CE		100	200	nsec
t_{HEC}	CE Pulse width	50	30		nsec
t_{SSC}	$\overline{CS}$ to CE setup	50	20		nsec
t_{HSC}	$\overline{CS}$ low during CE high	50	20		nsec
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		nsec
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		nsec
t_{SAC}	A_0 to CE setup	0	0		nsec
t_{HAC}	A_0 valid during CE high	50	20		nsec
t_c	Conversion time, 12 bit cycle	9	12	15	µsec
	8 bit cycle	6	8	10	µsec
Read Mode					
t_{DD}	Access time from CE		75	150	nsec
t_{HD}	Data valid after CE low	25	35		nsec
t_{HL}	Output float delay		100	150	nsec
t_{SSR}	$\overline{CS}$ to CE setup	50	0		nsec
t_{SRR}	R/$\overline{C}$ to CE setup	0	0		nsec
t_{SAR}	A_0 to CE setup	50	25		nsec
t_{HSR}	$\overline{CS}$ valid after CE low	0	0		nsec
t_{HRR}	R/$\overline{C}$ high after CE low	0	0		nsec
t_{HAR}	A_0 valid after CE low	50	25		nsec
t_{HS}	STS delay after data valid	100	300	600	nsec

NOTE: Specifications are at +25°C and measured at 50% level of transitions.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0–DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. Connection of the ADC674A to an 8-bit bus for transfer of left-justified data is illustrated in Figure 9. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

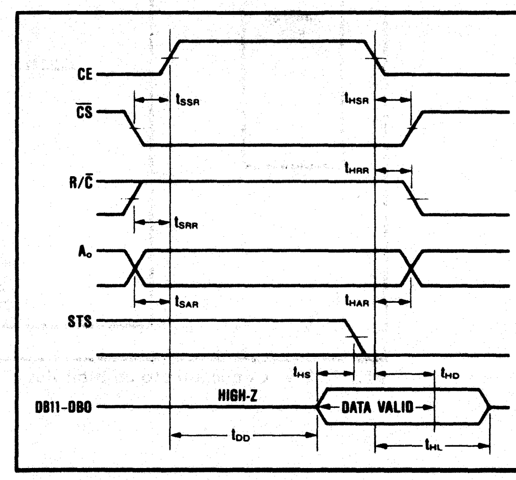


FIGURE 7. Read Cycle Timing.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC674A guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as 950nsec (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Figure 7 for these timing relationships.

ORDERING INFORMATION

Model	Temperature Range	Linearity Error, max (T_{MIN} to T_{MAX})	Resolution, No Missing Codes (T_{MIN} to T_{MAX})	Full-Scale TC, max (ppm/°C)
ADC674AJH	0°C to +75°C	±1LSB	11 Bits	±45
ADC674AKH	0°C to +75°C	±1/2LSB	12 Bits	±25
ADC674ASH	−55°C to +125°C	±1LSB	11 Bits	±50
ADC674ATH	−55°C to +125°C	±1LSB	12 Bits	±25

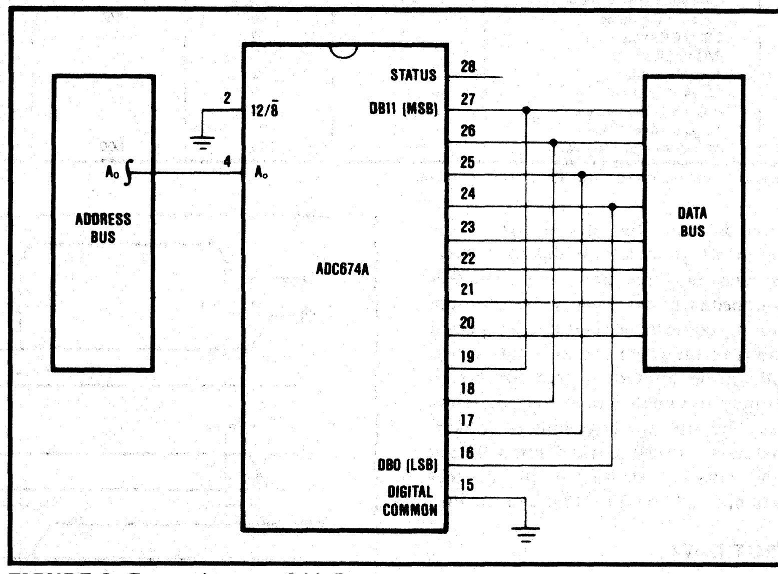


FIGURE 9. Connection to an 8-bit Bus.

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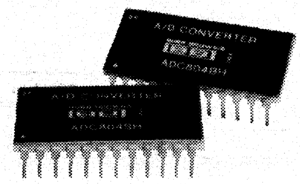


ADC804

Serial Output ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 17μsec CONVERSION TIME
- SERIAL OUTPUT—Ideal for applications requiring isolation or long-distance data transmission
- <500mW POWER DISSIPATION
- 24-PIN DUAL-WIDE HERMETIC PACKAGE
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- ±0.012% INTEGRAL LINEARITY
- 12-BIT RESOLUTION
- TWO TEMPERATURE RANGES AVAILABLE: ADC804BH for −25°C to +85°C Operation ADC804SH for −55°C to +125°C Operation
- NO MISSING CODES −25°C TO +85°C

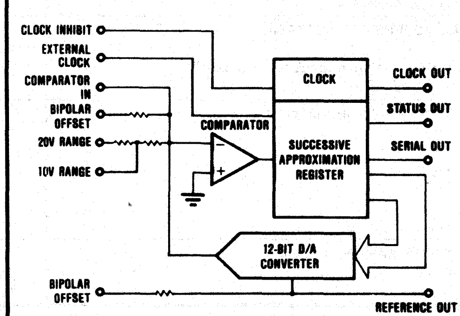
DESCRIPTION

The ADC804 is a 12-bit successive approximation analog-to-digital converter, custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic funtions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.012% (±1/2LSB). The ADC804 has two grades, one completely specified for −25°C to +85°C operation (ADC804BH), and the other for −55°C to +125°C operation (ADC804SH).

The maximum conversion time of 17μsec makes the ADC804 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 59kHz. In addition, an external clock may be used to synchronize the converter to the system clock or to obtain faster operation. As an added benefit for ADC80 users employing the serial output capability, the ADC804 is designed to replace or provide an alternate source to ADC80 with a minimum of circuit board changes and it provides a 40% reduction in conversion time.

Data is available in serial form with corresponding clock and status signals. Elimination of the parallel output capability enables the ADC804 to be the smallest fully self-contained 12-bit ADC available today. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC804 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic supply. It is packaged in a hermetic 24-pin side-brazed ceramic dual-in-line package.



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SPECIFICATIONS

ELECTRICAL

$T_A = +25°C$, $\pm V_{CC} = 12V$ or 15V, $V_{DD} = +5V$ unless otherwise specified.

MODEL	ADC804BH			ADC804SH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			*	Bits
INPUT							
ANALOG							
Voltage Ranges: Unipolar		0 to +5, 0 to +10			*		V
Bipolar		±2.5, ±5, ±10			*		V
Impedance: 0 to +5V, ±2.5V		2.3			*		kΩ
0 to +10V, +5V		4.6			*		kΩ
±10V		9.2			*		kΩ
DIGITAL							
Logic Characteristics (over specification temperature range)							
V_{IH} (logic "1")	2.0		5.5	*		*	V
V_{IL} (logic "0")	−0.3		+0.8	*		*	V
I_{IH} ($V_{IN} = +2.7V$)			−150			*	μA
I_{IL} ($V_{IN} = +0.4V$)			500			*	μA
Convert Command Pulse Width	100		1200	*		*	nsec
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(1)		±0.1	±0.3		*	*	% of FSR(2)
Offset Error(1): Unipolar		±0.05	±0.2		*	*	% of FSR
Bipolar		±0.1	±0.3		*	*	% of FSR
Linearity Error			±0.012			*	% of FSR
Differential Linearity Error			±1			*	LSB
Inherent Quantization Error		1/2			*		LSB
POWER SUPPLY SENSITIVITY							
$+13.5V \leq +V_{CC} \leq +16.5V$ or $+11.4V \leq +V_{CC} \leq +12.6V$		±0.003	±0.009		*	*	% of FSR/%V_{CC}
$-16.5V \leq -V_{CC} \leq -13.5V$ or $-12.6V \leq -V_{CC} \leq -11.4V$		±0.003	±0.009		*	*	% of FSR/%V_{CC}
$+4.5V \leq V_{DD} \leq +5.5V$		±0.002	±0.005		*	*	% of FSR/%V_{DD}
DRIFT							
Total Accuracy, Bipolar(3)		±10	±23		*	*	ppm/°C
Gain		±15	±30		*	*	ppm/°C
Offset: Unipolar		±3			*		ppm of FSR/°C
Bipolar		±7	±15		*	*	ppm of FSR/°C
Linearity Error Drift		±1	±3		*		ppm of FSR/°C
Differential Linearity over Temperature Range			+1, −3/4			*	LSB
No Missing Code Temperature Range	−25		+85	−55		+125	°C
Monotonicity Over Temperature Range		Guaranteed			Guaranteed		
CONVERSION TIME(4)		15	17		*	*	μsec
OUTPUTS							
DIGITAL(Clock Out, Status, Serial Out)							
Output Codes, Serial (NRZ)(5)		CSB,COB			*		
Logic Levels: Logic 0 ($I_{sink} \leq 3.2mA$)			+0.4			*	V
Logic 1 ($I_{source} \leq 80\mu A$)	+2.4			*			V
Internal Clock Frequency		92.3			*		kHz
INTERNAL REFERENCE VOLTAGE							
Voltage	+6.2	+6.3	+6.4	*	*	*	V
Source Current Available for External Loads(6)	200			*			μA
Temperature Coefficient		±10	±30		*	*	ppm/°C
POWER SUPPLY REQUIREMENTS							
Voltage, $\pm V_{CC}$	±11.4	±15	±16.5	*	*	*	V
V_{DD}	+4.5	+5.0	+5.5	*	*	*	V
Current, $+I_{CC}$		5	8.5		*	*	mA
$-I_{CC}$		21	26		*	*	mA
I_{DD}		11	15		*	*	mA
Power Dissipation ($\pm V_{CC} = 15V$)		450	595		*	*	mW
TEMPERATURE RANGE (Ambient)							
Specification	−25		+85	−55		+125	°C
Storage	−65		+150	*		*	°C

*Same as specification for ADC804BH.

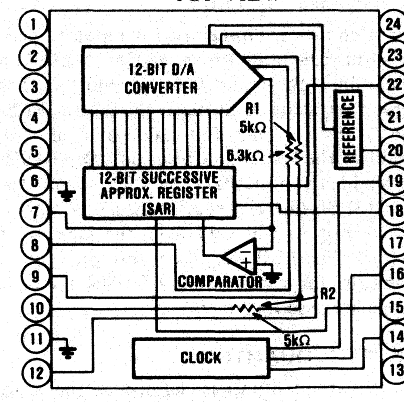
NOTES: (1) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustments" section. (2) FSR means full-scale range and is 20V for ±10V Range, 10V for ±5V and 0 to +10V ranges, etc. (3) Includes drift due to linearity, gain, and offset drifts. (4) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. (5) CSB means Complementary Straight Binary, and COB means Complementary Offset Binary, NRZ means non-return-to-zero coding. See Table I for additional information. (6) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specifications.

CONNECTION DIAGRAM

Pin 1 - N/C
Pin 2 - N/C
Pin 3 - N/C
Pin 4 - N/C
Pin 5 - V_{DD}
Pin 6 - Digital Common
Pin 7 - Comparator In
Pin 8 - Bipolar Offset
Pin 9 - R1 10V Range
Pin 10 - R2 20V Range
Pin 11 - Analog Common
Pin 12 - Gain Adjust

Pin 24 - N/C
Pin 23 - N/C
Pin 22 - Serial Out
Pin 21 - $-V_{CC}$
Pin 20 - Reference Out (+6.3V)
Pin 19 - Clock Out
Pin 18 - Status
Pin 17 - N/C
Pin 16 - Clock Inhibit
Pin 15 - External Clock
Pin 14 - Convert Command
Pin 13 - $+V_{CC}$

TOP VIEW



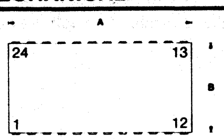
ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common .... 0 to +16.5V
$-V_{CC}$ to Analog Common .... 0 to −16.5V
V_{DD} to Digital Common .... 0 to +7V
Analog Common to Digital Common .... ±0.5V
Logic Inputs (Convert Command, Clock In)
 to Digital Common .... −0.3V to V_{DD} +0.5V
Analog Inputs (Analog In, Bipolar Offset)
 to Analog Common .... ±16.5V
Reference Output .... Indefinite Short to Common, Momentary Short to V_{CC}
Power Dissipation 1000mW
Lead Temperature, Soldering .... +300°C, 10sec
Thermal Resistance, θ_{JA} .... 60°C/W

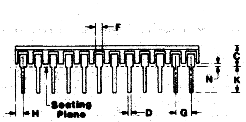
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

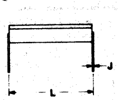
CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

MECHANICAL



NOTES:
1. Leads in true position within .010" (.25MM) R at MMC at Seating Plane.
2. Pin numbers shown for reference only. may not be marked on package.





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.190	1.210	30.23	30.73
B	.580	.600	14.73	15.24
C	.112	[illegible]	2.84	[illegible]
D	.015	.019	0.38	0.48
F	.040	.060	1.02	1.52
G	.100	BASIC	2.54	BASIC
H	.030	.070	0.76	1.78
J	.009	.012	0.23	0.30
K	.136	.176	3.45	4.46
L	.590	.610	14.99	15.49
N	.010	.030	0.25	0.76

CASE: Ceramic, hermetic

MATING CONNECTOR: 0245MC

WEIGHT: 4.4gm (0.16oz)

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers. The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1, which illustrates these relationships. A linearity specification which guarantees

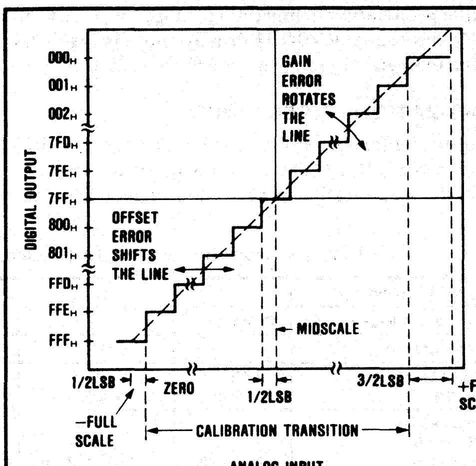


FIGURE 1. ADC804 Transfer Characteristic Terminology.

±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC804 analog input signal range are described in Table I.

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC804 input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is a definition of the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. The ADC804BH is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range of −25°C to +85°C, and the ADC804SH displays no missing codes over the temperature range of −55°C to +125°C.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC804 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC804 follows this convention. Thus, bipolar offset error for the ADC804 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the specification range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC804 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

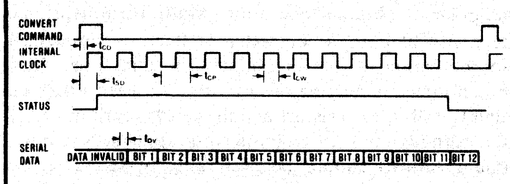
TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB*	COB*	COB*	CSB**	CSB**
One Least Significant Bit (LSB)	$FSR/2^n$ n = 12	$20V/2^n$ 4.88mV	$10V/2^n$ 2.44mV	$5V/2^n$ 1.22mV	$10V/2^n$ 2.44mV	$5V/2^n$ 1.22mV
Transition Values MSB LSB 001_H to 000_H 800_H to $7FF_H$ FFF_H to FFE_H	+Full Scale Mid Scale −Full Scale	+10V − 3/2LSB 0 −10V + 1/2LSB	+5V − 3/2LSB 0 −5V + 1/2LSB	+2.5V − 3/2LSB 0 −2.5V + 1/2LSB	+ 10V − 3/2LSB +5V 0 + 1/2LSB	+5V − 3/2LSB + 2.5V 0 + 1/2LSB

*COB = Complementary Offset Binary **CSB = Complementary Straight Binary

TIMING CONSIDERATIONS

Timing relationships of the ADC804 are shown in Figure 2. It should be noted that although the convert command pulse width must be between 100nsec and 1.2μsec to obtain the specified conversion time with internal clock, the ADC804 will accept longer convert commands with no loss of accuracy, assuming that the



Symbol	Parameter	Typ	Units
t_{CD}	Clock delay from convert command	30	nsec
t_{CP}	Nominal clock period	1.1	μsec
t_{CW}	Nominal clock pulse width	0.55	μsec
t_{SD}	Status delay from convert command	130	nsec
t_{DV}	Data valid time from clock pulse high	−35	nsec

FIGURE 2. ADC804 Timing Diagram (normal values at +25°C with internal clock).

analog input signal is stable. In this situation, the actual indicated conversion time (during which status is high) for 12-bit operation will be equal to approximately 600nsec less than the sum of the factory-set conversion time and the length of the convert command. The code returned by the converter at the end of the conversion will accurately represent the analog input to the converter at the time the convert command returns to the low state. In addition, although the initial state of the converter will be indeterminate when power is first applied, it is designed to time-out and be ready to accept a convert command within approximately 15μsec after power-up, provided that either an external clock source is present or the internal clock is not inhibited.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse " n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the rising edge of the thirteenth clock pulse. A new conversion may not be initiated until 50nsec after the fall of the thirteenth clock pulse. Additional convert commands applied during conversion will be ignored.

DEFINITION OF DIGITAL CODES

Two binary codes are available on the serial output of the ADC804, complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) for bipolar input ranges. Both are complementary codes, meaning that logic "0" is true. Serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. All clock pulses available from the ADC804 have a nominal pulse width of 550nsec to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC804 but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use a wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC804 as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC804 will be driving into a nominal DC input impedance of 2.5kΩ to 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC804 offers five standard input ranges: 0V to+5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. Use of external padding resistors to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range) will require matching of the external fixed resistor values to individual devices, due to the large tolerance of the internal input resistors. Alternatively, the gain range of the converter may be easily increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by decreasing the value of the gain adjust series resistor in Figure 6.

TABLE II. ADC804 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 8 To Pin	Connect Pin 10 To	Connect Input Signal To
±10V	COB	7	Input Signal	10
±5V	COB	7	Open	9
±2.5V	COB	7	Pin 7	9
0 to +5V	CSB	11	Pin 7	9
0 to +10V	CSB	11	Open	9

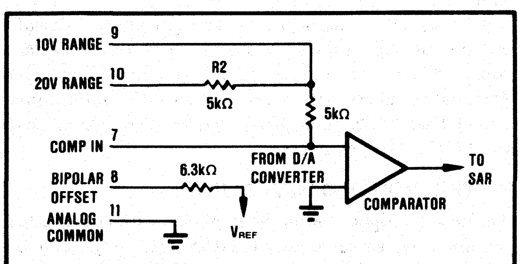


FIGURE 3. ACD804 Input Scaling Circuit.

REPLACEMENT OF ADC80

As illustrated in Figure 4, a circuit board configured for use of the ADC80 serial output capability may be very easily adapted to also use the ADC804, or to achieve space savings due to the smaller package of the ADC804. The pin assignments of the ADC804 have been chosen to allow it to fit neatly into one corner of the ADC80 layout. When replacing ADC80 with ADC804, a board space improvement of approximately 1.25 square inches (8.06cm^2) is obtained.

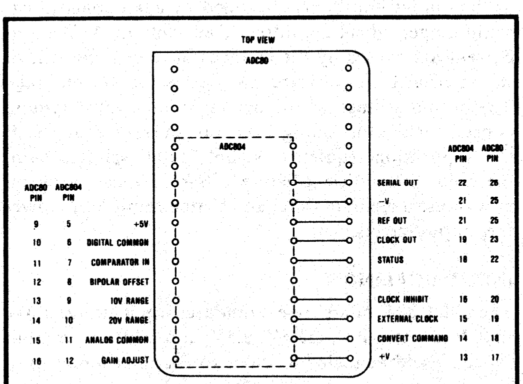


FIGURE 4. Adapting an ADC80 Layout for ADC804.

CALIBRATION

Optional External Gain and Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC804 as shown in Figures 5 and 6 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These potentiometers may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 12 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

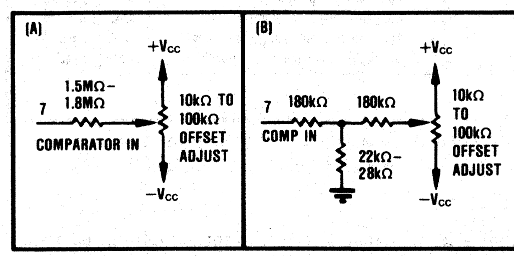


FIGURE 5. Two Methods of Connecting Optional Offset Adjust.

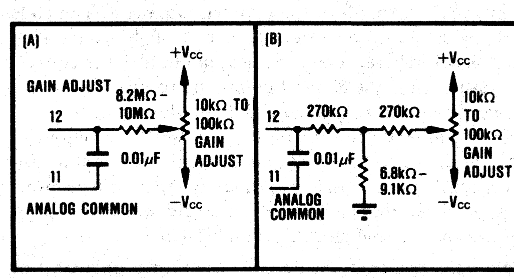


FIGURE 6. Two Methods of Connecting Optional Gain Adjust.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 5. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V + 2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE$_H$ and FFF$_H$ with approximately 50% occurrence of each of the two codes. In other words, the potentiomter is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 6. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V − 7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transition to a precisely known value.

CLOCK OPTIONS

The ADC804 is extremely versatile in that it can be operated with either internal or external clock. Thus, use of an available system clock enables synchronization of the converter to the rest of the system to optimize performance in a noisy environment.

When operating with the internal clock, pin 15 (external clock input) and pin 16 (clock inhibit) may be left unconnected. No external pull-ups are required due to the inclusion of pull-up resistors in the ADC804. Pin 16 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 15.

See Figures 7 through 10 for diagrams to implement the various clock options.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models

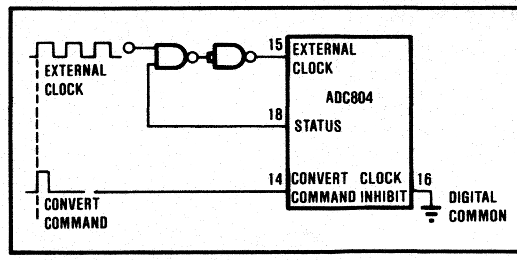


FIGURE 8. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

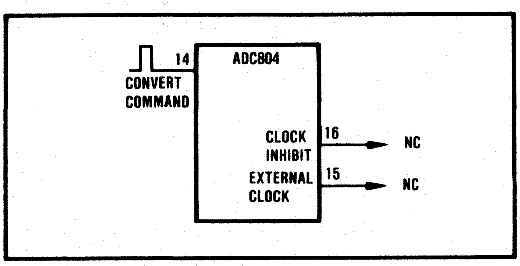


FIGURE 7. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

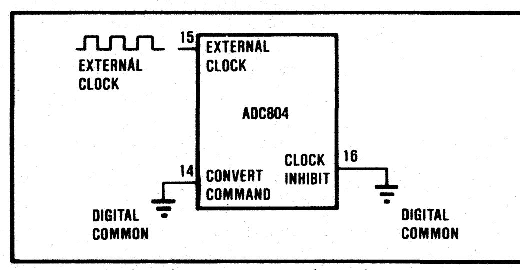


FIGURE 9. Continuous Conversion with external Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

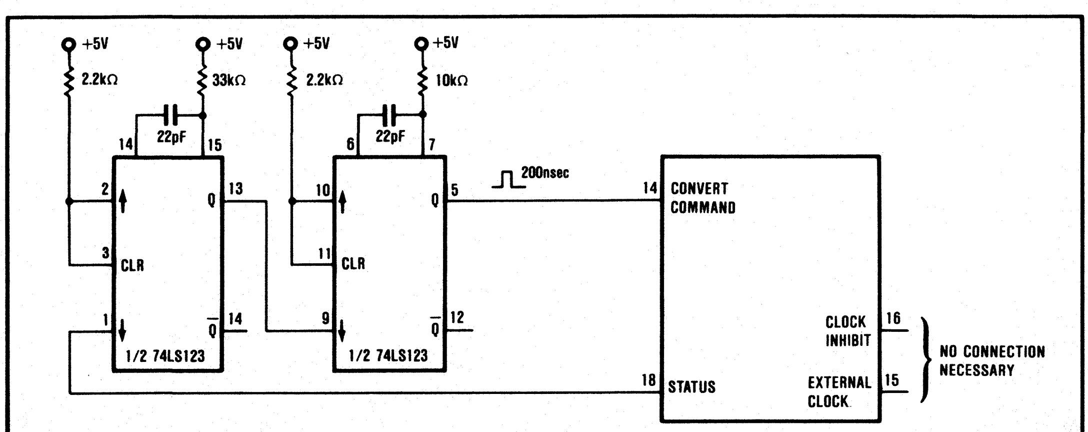


FIGURE 10. Continuous Conversion with 200nsec between Conversions Using Internal Clock. (Circuit insures that the conversion process will start when power is applied.)

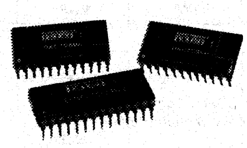
are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table III is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE III. Screening Flow for ADC804xHQ

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-in	1015, B	160 hour, +125°C, steady-state
Hermeticity: Fine Leak Gross Leak	 1014, A1 or A2 1014, C	 5×10^{-7} atm cc/sec bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	Burr-Brown QC4118	

BURR-BROWN®

DAC705/706/707 DAC708/709



Microprocessor-Compatible 16-BIT DIGITAL-TO-ANALOG CONVERTERS

FEATURES

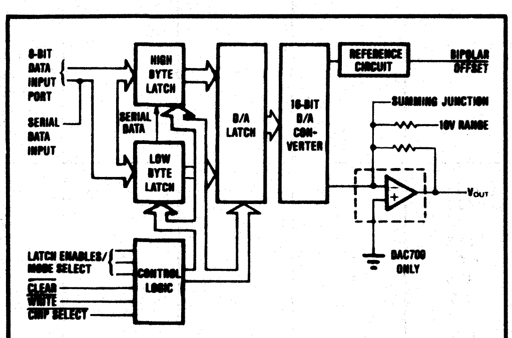
- **TWO-CHIP CONSTRUCTION**
- **HIGH-SPEED 16-BIT PARALLEL, 8-BIT (BYTE) PARALLEL, AND SERIAL INPUT MODES**
- **DOUBLE-BUFFERED INPUT REGISTER CONFIGURATION**
- **V_{OUT} AND I_{OUT} MODELS**
- **HIGH ACCURACY:**
  Linearity Error ±0.003% of FSR max
  Differential Linearity Error ±0.006% of FSR max
- **MONOTONIC (TO 14 BITS) OVER SPECIFIED TEMPERATURE RANGE**
- **HERMETICALLY SEALED**

DESCRIPTION

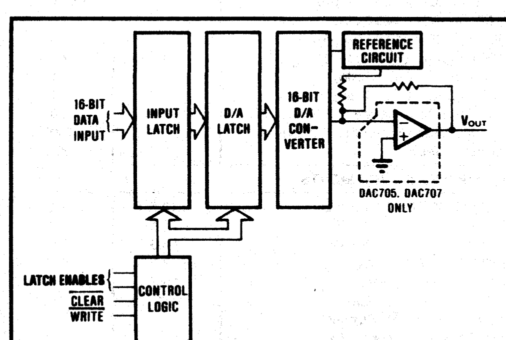
The DAC708 and DAC709 are 16-bit converters designed to interface to an 8-bit microprocessor bus. 16-bit data is loaded in two successive 8-bit bytes into parallel 8-bit latches before being transferred into the D/A latch. The DAC708 and DAC709 are current and voltage output models respectively and are in 24-pin hermetic DIPs. Input coding is Binary Two's Complement (bipolar) or Unipolar Straight Binary (unipolar, when an external logic inverter is used to invert the MSB). In addition, the DAC708/709 can be loaded serially (MSB first). They are packaged in a 24-pin hermetic DIP.

The DAC705, DAC706, and DAC707 are designed to interface to a 16-bit bus. Data is written into a 16-bit latch and subsequently the D/A latch. The DAC705 and DAC707 are voltage output models. DAC706 is a current output model. Outputs are bipolar only (current or voltage) and input coding is Binary Two's Complement (BTC).

All models have Write and Clear control lines as well as input latch enable lines. In addition, DAC708 and DAC709 have Chip Select control lines. In the bipolar mode, the Clear input sets the D/A latch to give zero voltage or current output. They are all 14-bit accurate and are complete with reference, and, for the DAC705, DAC707, and DAC709, a voltage output amplifier.



DAC708/709 Block Diagram



DAC705/706/707 Block Diagram

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10 minute warm-up unless otherwise noted.

MODEL	DAC705/706/707/708/709KH			DAC705/706/707/708/709BH, SH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution			16			*	Bits
Bipolar Input Code (All models)		Binary Two's Complement			*		
Unipolar Input Code[1] (DAC708/709 only)		Unipolar Straight Binary			*		
Logic Levels[2]: V_{IH}	+2.0		+5.5	*		*	V
V_{IL}	−1.0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			1			*	µA
I_{IL} (V_I = +0.4V)			1			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY[3]							
Linearity Error		±0.0015	±0.003		*	*	% of FSR[4]
Differential Linearity Error[5]		±0.003	±0.006		*	*	% of FSR
at Bipolar Zero[5,6]		±0.003	±0.006		±0.0015	±0.003	% of FSR
Gain Error[7]		±0.07	±0.15		±0.05	±0.10	%
Zero Error[7]		±0.05	±0.1		*	*	% of FSR
Monotonicity Over Spec Temp Range	14			*			Bits
Power Supply Sensitivity: $+V_{CC}$		±0.0015	±0.006		*	±0.003	% of FSR/%V_{CC}
$-V_{CC}$		±0.0015	±0.006		*	±0.003	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*	% of FSR/%V_{DD}
DRIFT (over specification temperature range[3])							
Gain Drift		±10	±25		±7	±15	ppm/°C
Zero Drift: Unipolar (DAC708/709 only)		±2.5	±5		±1.5	±3	ppm of FSR/°C
Bipolar (all models)		±5	±12		±4	±10	ppm of FSR/°C
Differential Linearity Over Temp[5]			+0.009, −0.006			*	% of FSR
Linearity Error Over Temp[5]			±0.006			*	% of FSR
SETTLING TIME (to ±0.003% of FSR)[8]							
Voltage Output Models							
Full Scale Step (2kΩ load)		4	8		*	*	µsec
1LSB Step at Worst Case Code[9]		2.5	4		*	*	µsec
Slew Rate		10			*		V/µsec
Current Output Models							
Full Scale Step (2mA)							
10 to 100Ω load		350			*		nsec
1kΩ load		1			*		µsec
OUTPUT							
VOLTAGE OUTPUT MODELS							
Output Voltage Range							
DAC709 Unipolar (USB Code)		0 to +10			*		V
Bipolar (BTC Code)		±5, ±10			*		V
DAC707 Bipolar (BTC Code)		±10			*		V
DAC705 Bipolar (BTC Code)		±5			*		V
Output Current	±5			*			mA
Output Impedance		0.15			*		Ω
Short Circuit to Common Duration		Indefinite			*		
CURRENT OUTPUT MODELS							
Output Current Range (±30% typ)							
DAC708 Unipolar (USB Code)		0 to −2			*		mA
Bipolar (BTC Code)		±1			*		mA
DAC706 Bipolar (BTC Code)		±1					mA
Unipolar Output Impedance (±30% typ)		4.0			*		kΩ
Bipolar Output Impedance (±30% typ)		2.45			*		kΩ
Compliance Voltage		±2.5			*		V
POWER SUPPLY REQUIREMENTS							
Voltage, DAC705/706/707: $+V_{CC}$	+13.5	+15	+16.5	*	*	*	V
$-V_{CC}$	−13.5	−15	−16.5	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	V
Voltage, DAC708/709: $+V_{CC}$	+13.5	+15	+16.5	*	*	*	V
$-V_{CC}$	−13.5	−15	−16.5	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	V
Current (No load, +15V supplies)							
Current Output Models: $+V_{CC}$		+10	+25		*	*	mA
$-V_{CC}$		−13	−25		*	*	mA
V_{DD}		+5	+10		*	*	mA
Voltage Output Models: $+V_{CC}$		+16	+30		*	*	mA
$-V_{CC}$		−18	−30		*	*	mA
V_{DD}		+5	+10		*	*	mA

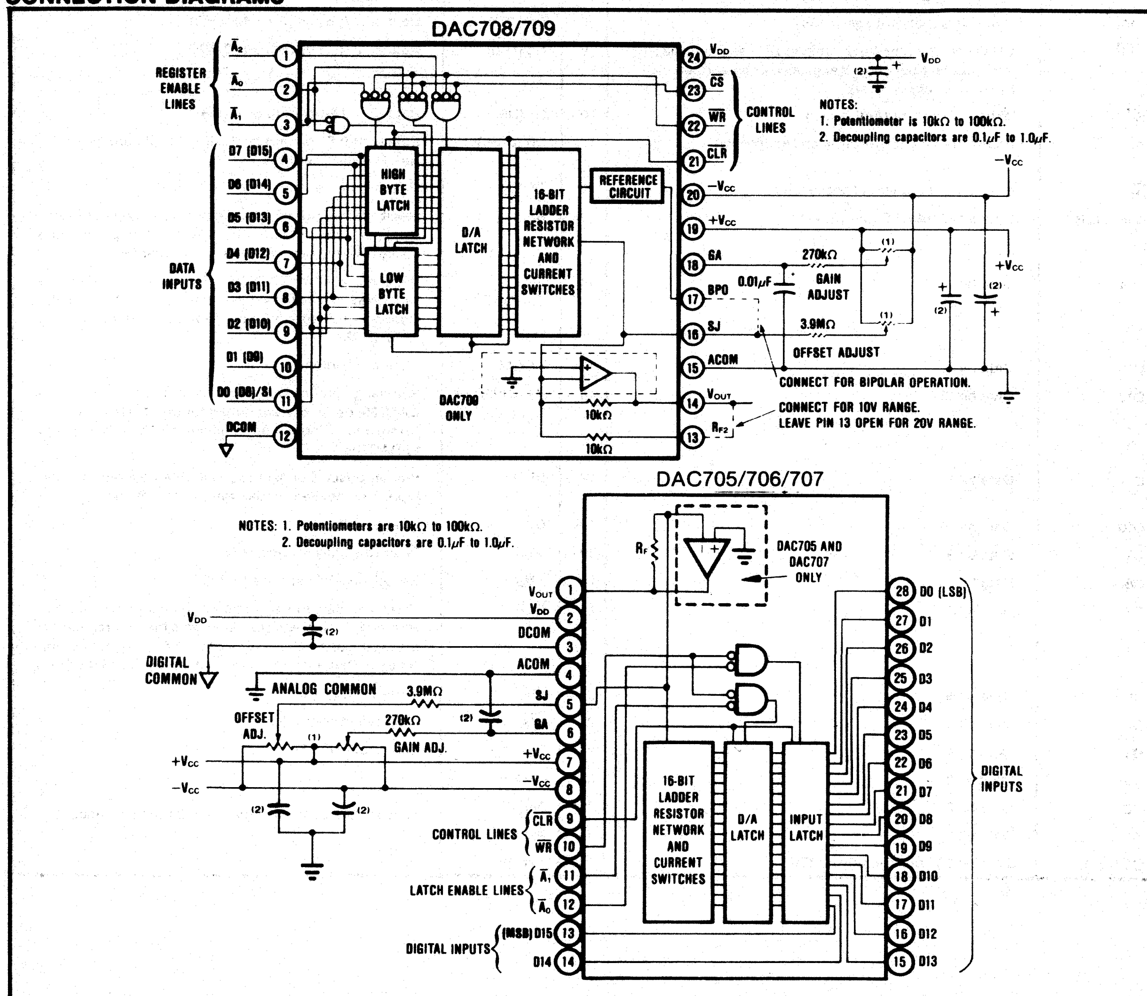
ELECTRICAL (CONT)

MODEL	DAC705/706/707/708/709KH			DAC705/706/707/708/709BH, SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS (CONT)							
Power Dissipation (±15V supplies)							
Current Output Models		370	800		*	*	mW
Voltage Output Models		535	950		*	*	mW
TEMPERATURE RANGE							
Specification: BH grades				−25		+85	°C
KH grades	0		+70				°C
SH grades				−55		+125	°C
Storage	−65		+150	*		*	°C

*Specification same as for DAC706/707/708/709KH.

NOTES: (1) MSB must be inverted externally prior to DAC708/709 input. (2) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the specified temperature range. (3) DAC706 and DAC708 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all tests. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) ±0.0015% of Full Scale Range is equal to 1 LSB in 16-bit resolution. ±0.003% of Full Scale Range is equal to 1 LSB in 15-bit resolution. ±0.006% of Full Scale Range is equal to 1 LSB in 14-bit resolution. (6) Error at input code 0000_H. (For unipolar connection on DAC708/709 the MSB must be inverted externally prior to D/A input.) (7) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) The bipolar worst-case code change is $FFFF_H$ to 0000_H and 0000_H to $FFFF_H$. For unipolar (DAC708/709 only) it is $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$.

CONNECTION DIAGRAMS

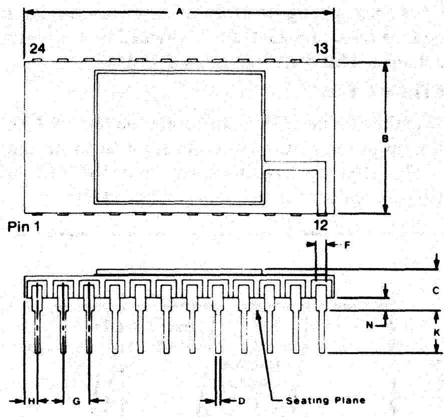


DESCRIPTION OF PIN FUNCTIONS

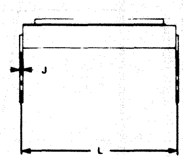
DAC705/706/707		Pin	DAC708/709	
Designator	Description	#	Designator	Description
V_{OUT} (DAC707 and DAC705) R_F (DAC706)	Voltage output for DAC707 (±10V) and DAC705 (±5V) or an internal feedback resistor for use with an external output op amp for the DAC706.	1	$\overline{A_2}$	Latch enable for D/A latch (Active low)
V_{DD}	Logic supply (+5V)	2	$\overline{A_0}$	Latch enable for "low byte" input (Active low). When both $\overline{A_0}$ and $\overline{A_1}$ are logic "0", the serial input mode is selected and the serial input is enabled.
DCOM	Digital Common	3	$\overline{A_1}$	Latch enable for "high byte" input (Active low). When both $\overline{A_0}$ and $\overline{A_1}$ are logic "0", the serial input mode is selected and the serial input is enabled.
ACOM	Analog Common	4	D7 (D15)	Input for data bit 7 if enabling low byte (LB) latch or data bit 15 if enabling the high byte (HB) latch.
SJ (DAC705 and DAC707) I_{OUT} (DAC706)	Summing Junction of the internal output op amp for the DAC705 and DAC707, or the current output for the DAC706. Offset adjust circuit is connected to the summing junction of the output amplifier. Refer to Block Diagram.	5	D6 (D14)	Input for data bit 6 if enabling LB latch or data bit 14 if enabling the HB latch.
GA	Gain Adjust pin. Refer to Connection Diagram for gain adjust circuit.	6	D5 (D13)	Data bit 5 (LB) or data bit 13 (HB)
$+V_{CC}$	Positive supply voltage (+15V)	7	D4 (D12)	Data bit 4 (LB) or data bit 12 (HB)
$-V_{CC}$	Negative supply voltage (−15V)	8	D3 (D11)	Data bit 3 (LB) or data bit 11 (HB)
$\overline{CLR}$	Clear line. Sets the input latch to zero and sets the D/A latch to the input code that gives bipolar zero on the D/A output (Active low)	9	D2 (D10)	Data bit 2 (LB) or data bit 10 (HB)
$\overline{WR}$	Write control line (Active low)	10	D1 (D9)	Data bit 1 (LB) or data bit 9 (HB)
$\overline{A_1}$	Enable for D/A converter latch (Active low)	11	D0 (D8)/SI	Data bit 0 (LB) or data bit 8 (HB). Serial input when serial mode is selected.
$\overline{A_0}$	Enable for input latch (Active low)	12	DCOM	Digital Common
D15 (MSB)	Data bit 15 (Most Significant Bit)	13	R_{F2}	Feedback resistor for internal or external operational amplifier. Connect to pin 14 when a 10V output range is desired. Leave open for a 20V output range.
D14	Data bit 14	14	V_{OUT} R_{F1} (DAC708)	Voltage output for DAC709 or feedback resistor for use with an external output op amp for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D13	Data bit 13	15	ACOM	Analog common
D12	Data bit 12	16	SJ (DAC709) I_{OUT} (DAC708)	Summing junction of the internal output op amp for the DAC709, or the current output for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D11	Data bit 11	17	BPO	Bipolar offset. Connect to pin 16 when operating in the bipolar mode. Leave open for unipolar mode.
D10	Data bit 10	18	GA	Gain Adjust pin
D9	Data bit 9	19	$+V_{CC}$	Positive supply voltage (+15V)
D8	Data bit 8	20	$-V_{CC}$	Negative supply voltage (−15V)
D7	Data bit 7	21	$\overline{CLR}$	Clear line. Sets the high and low byte input registers to zero and, for bipolar operation, sets the D/A register to the input code that gives bipolar zero on the D/A output. (In the unipolar mode, invert the MSB prior to the D/A.)
D6	Data bit 6	22	$\overline{WR}$	Write control line
D5	Data bit 5	23	$\overline{CS}$	Chip select control line
D4	Data bit 4	24	V_{DD}	Logic supply (+5V)
D3	Data bit 3	25	No pin	
D2	Data bit 2	26	No pin	(The DAC708 and DAC709 are in 24-pin packages)
D1	Data bit 1	27	No pin	
D0 (LSB)	Data bit 0 (Least Significant Bit)	28	No pin	

MECHANICAL

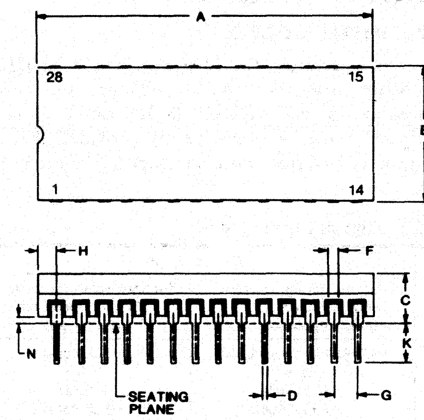
DAC708/709

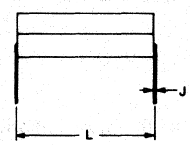


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.190	1.210	30.23	30.73
B	.580	.600	14.73	15.24
C	.140	.185	3.56	4.70
D	.016	.020	0.41	0.51
F	.030	.050	0.76	1.27
G	.100 BASIC		2.54 BASIC	
H	.035	.065	0.89	1.65
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52



DAC705/706/707





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.465	35.20	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	.38	.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.035	.095	.89	2.41
J	.009	.012	.23	.30
K	.155	.195	3.94	4.05
L	.600 BASIC		15.42 BASIC	
N	.020	.060	.51	1.52

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON .... 0V, +15V
$+V_{CC}$ to COMMON .... 0V, +18V
$-V_{CC}$ to COMMON .... 0V, −18V
Digital Data Inputs to COMMON .... −0.5V, V_{DD} +0.5
DC Current any Input .... ±10mA
Reference Out to COMMON .... Indefinite Short to COMMON
External Voltage Applied to R_F
(pin 1, DAC706; pin 13 or 14, DAC708) .... ±18V

External Voltage Applied to D/A Output
(pin 1, DAC707; pin 14, DAC709) .... ±5V
V_{OUT} (DAC707, DAC709) .... Indefinite Short to COMMON
Power Dissipation 1000mW
Storage Temperature .... −60°C to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Model	Temperature Range	Input Configuration	Output Configuration
DAC705KH	0 to +70°C	16-bit port	±5V output
DAC705BH	−25 to +85°C	16-bit port	±5V output
DAC705BH/QM	−25 to +85°C	16-bit port	±5V output
DAC705SH	−55 to +125°C	16-bit port	±5V output
DAC705SH/QM	−55 to +125°C	16-bit port	±5V output
DAC706KH	0 to +70°C	16-bit port	±1mA output
DAC706BH	−25 to +85°C	16-bit port	±1mA output
DAC706BH/QM	−25 to +85°C	16-bit port	±1mA output
DAC706SH	−55 to +125°C	16-bit port	±1mA output
DAC706SH/QM	−55 to +125°C	16-bit port	±1mA output
DAC707KH	0 to +70°C	16-bit port	±10V output
DAC707BH	−25 to +85°C	16-bit port	±10V output
DAC707BH/QM	−25 to +85°C	16-bit port	±10V output
DAC707SH	−55 to +125°C	16-bit port	±10V output
DAC707SH/QM	−55 to +125°C	16-bit port	±10V output
DAC708KH	0 to +70°C	8-bit port	±1mA output
DAC708BH	−25 to +85°C	8-bit port	±1mA output
DAC708BH/QM	−25 to +85°C	8-bit port	±1mA output
DAC708SH	−55 to +125°C	8-bit port	±1mA output
DAC708SH/QM	−55 to +125°C	8-bit port	±1mA output
DAC709KH	0 to +70°C	8-bit port	±10V output
DAC709BH	−25 to +85°C	8-bit port	±10V output
DAC709BH/QM	−25 to +85°C	8-bit port	±10V output
DAC709SH	−55 to +125°C	8-bit port	±10V output
DAC709SH/QM	−55 to +125°C	8-bit port	±10V output

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

For bipolar operation, the DAC705/706/707/708/709 accept positive-true binary two's complement input code. For unipolar operation (DAC708/709 only) the input code is positive-true straight-binary provided that the MSB input is inverted with an external inverter. See Table I.

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output	
	Unipolar Straight Binary[1] (DAC708/709 only; connected for Unipolar operation)	Binary Two's Complement (Bipolar operation; all models)
$7FFF_H$	+1/2 Full Scale −1 LSB[2]	+Full Scale
0000_H	Zero	Zero
$FFFF_H$	+Full Scale	−1LSB
8000_H	+1/2 Full Scale	−Full Scale

(1) MSB must be inverted externally. (2) Assumes MSB is inverted externally.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (−Full Scale point and +Full Scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of −1LSB maximum (−0.0006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC705/706/707/708/709 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences at t_{min}, +25°C and t_{max}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with 0000_H applied to the D/A converter inputs over the specified temperature range. (For the DAC708/709 in unipolar mode, the MSB must be inverted.) This code corresponds to zero volts (DAC705/707 and DAC709) or zero milliamps (DAC706 and DAC708) at the analog output. The maximum change in offset at t_{min} or t_{max} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

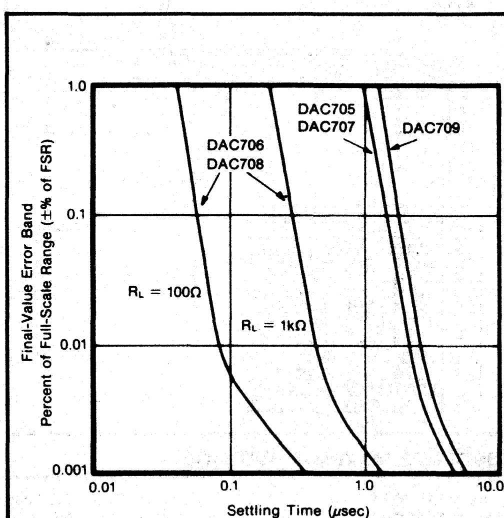


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2 LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V) or 10V (±5V or 0 to 10V) and a 1LSB change at the "major carry", the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

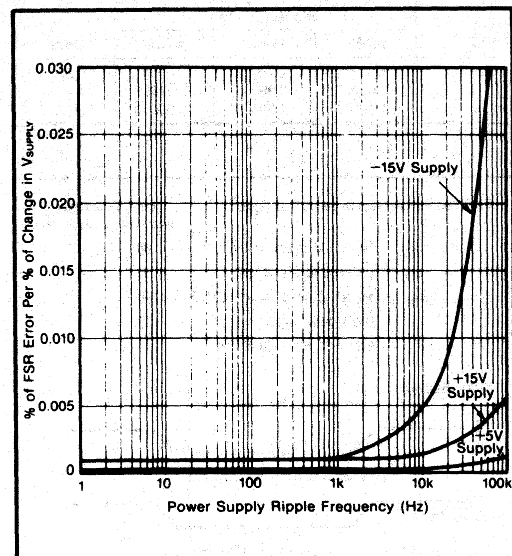


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001μF to 0.01μF ceramic capacitor should be connected from GAIN ADJUST to ANALOG COMMON to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar D/A converters.

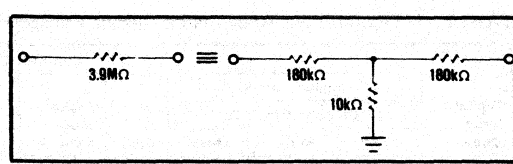


FIGURE 3. Equivalent Resistances.

Zero Adjustment

For unipolar (USB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (BTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and connection diagrams for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

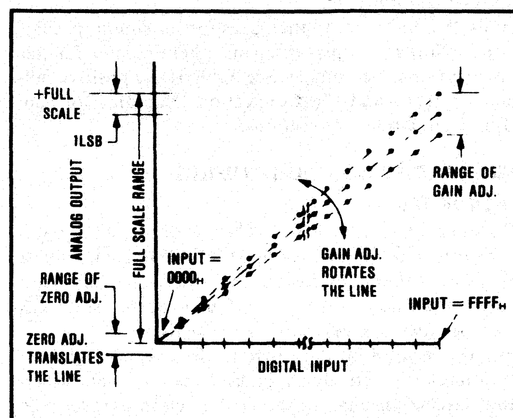


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC708 and DAC709.

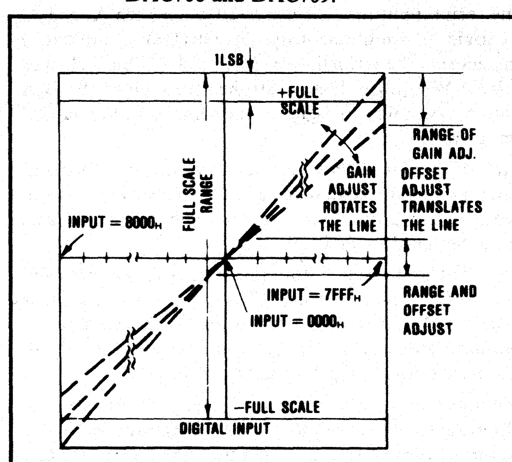


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC705/706/707 and DAC708/709.

TABLE II. Digital Input And Analog Output Voltage/Current Relationships.

VOLTAGE OUTPUT MODELS

Digital Input Code	Analog Output *Unipolar, 0 to +10V			Units	Digital Input Code	Analog Output Bipolar, ±10V			Analog Output Bipolar, ±5V			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	16-Bit	15-Bit	14-Bit	
One LSB	153	305	610	μV	One LSB	305	610	1224	153	305	610	μV
$FFFF_H$	+9.99985	+9.99969	+9.99939	V	$7FFF_H$	+9.99960	+9.99939	+9.99878	+4.99980	+4.99970	+4.99939	V
0000_H	0	0	0	V	8000_H	−10.0000	−10.0000	−10.0000	−5.0000	−5.0000	−5.0000	V

CURRENT OUTPUT MODELS

Digital Input Code	Analog Output *Unipolar, 0 to −2mA			Units	Digital Input Code	Analog Output Bipolar, ±1mA			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	
One LSB	0.031	0.061	0.122	μA	One LSB	0.031	0.061	0.122	μA
$FFFF_H$	−1.99997	−1.99994	−1.99988	mA	$7FFF_H$	−0.99997	−0.99994	−0.99988	mA
0000_H	0	0	0	mA	8000_H	+1.00000	+1.00000	+1.00000	mA

*MSB assumed to be inverted externally.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and the Connection Diagrams for gain adjustment circuit connections.

INTERFACE LOGIC AND TIMING

DAC708/709

The signals CHIP SELECT ($\overline{CS}$), WRITE ($\overline{WR}$), register enables ($\overline{A_0}$, $\overline{A_1}$, and $\overline{A_2}$) and CLEAR ($\overline{CLR}$), provide the control functions for the microprocessor interface. They are all active in the "low" or logic "0" state. $\overline{CS}$ must be low to access any of the registers. $\overline{A_0}$ and $\overline{A_1}$ steer the input 8-bit data byte to the low- or high-byte input latch respectively. $\overline{A_2}$ gates the contents of the two input latches through to the D/A latch in parallel. The contents are then applied to the input of the D/A converter. When $\overline{WR}$ goes low, data is strobed into the latch or latches which have been enabled.

The serial input mode is activated when both $\overline{A_0}$ and $\overline{A_1}$ are logic "0" simultaneously. The D0 (D8)/SI input data line accepts the serial data MSB first. Each bit is clocked in by a $\overline{WR}$ pulse. Data is strobed through to the D/A latch by $\overline{A_2}$ going to logic "0" the same as in the parallel input mode.

Each of the latches can be made "transparent" by maintaining its enable signal at logic "0". However, as stated above, when both $\overline{A_0}$ and $\overline{A_1}$ are logic "0" at the same time, the serial mode is selected.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the D/A latch to 8000_H. This is the binary code that gives a null, or zero, at the output of the D/A in the bipolar mode. In the unipolar mode, activating $\overline{CLR}$ will cause the output to go to one-half of full scale.

The maximum clock rate of the latches is 10MHz. The minimum time between write (WR) pulses for successive enables is 20nsec. In the serial input mode (DAC708 and DAC709), the maximum rate at which data can be clocked into the input shift register is 10MHz.

The timing of the control signals is given in Figure 6.

LOGIC TIMING - Parallel or Serial Data Input

		Over Temperature nsec, min.	nsec, max.
t_{DW}	Data valid to end of $\overline{WR}$	80	
t_{CW}	$\overline{CS}$ valid to end of $\overline{WR}$	80	
t_{AW}	$\overline{A0}$, $\overline{A1}$, $\overline{A2}$ valid to end of $\overline{WR}$	80	
t_{WP}	Write pulse width	80	
t_{DH}	Data held after end of $\overline{WR}$		0

TIMING DIAGRAM

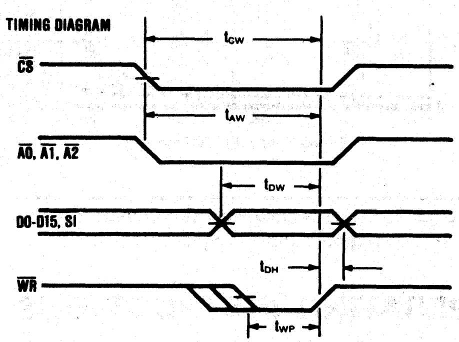


FIGURE 6. Logic Timing Diagram.

DAC706/707

The DAC705/706/707 interface timing is the same as that described above except instead of two 8-bit separately-enabled input latches, it has a single 16-bit input latch enabled by $\overline{A_0}$. The D/A latch is enabled by $\overline{A_1}$. Also, there is no serial-input mode and no CHIP SELECT ($\overline{CS}$) line.

INSTALLATION CONSIDERATIONS

Due to the extremely-high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of typical 1 ounce copper-clad printed circuit board material is approximately 1/2mΩ per square. In the example above, a 10 milliinch-wide conductor 60 milliinches long would cause a 1LSB error.

In Figures 7 and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error

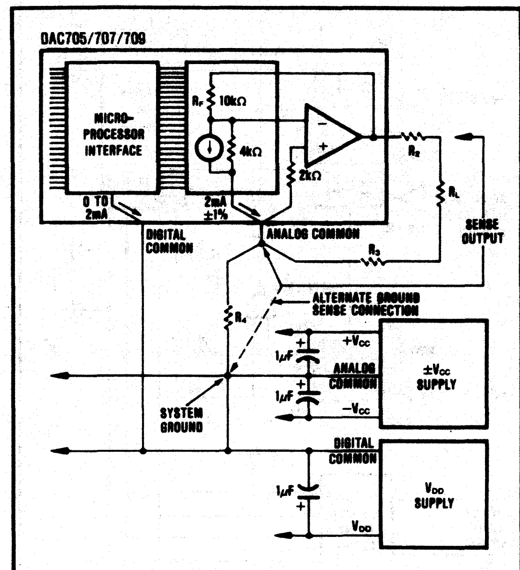


FIGURE 7. DAC705/707/709 Bipolar Output Circuit (Voltage Out).

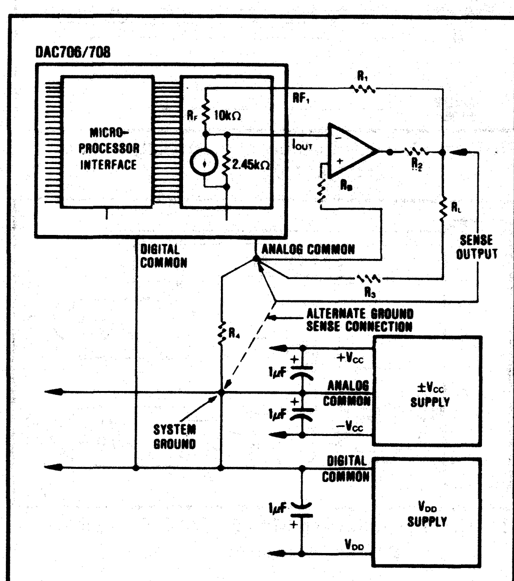


FIGURE 8. DAC706/708 Bipolar Output Circuit (with External Op Amp).

and can be removed with gain calibration. R_3 is part of R_L if the output voltage is sensed at ANALOG COMMON.

Figures 8 and 9 show two methods of connecting the currrent output model with an external precision output op amp. By sensing the output voltage at the load resistor (connecting R_F to the output of the amplifier at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

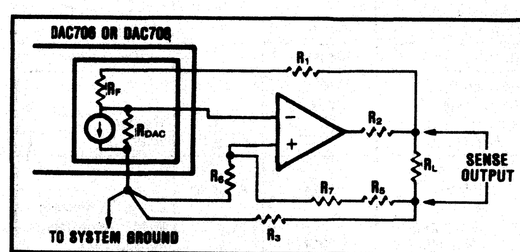


FIGURE 9. Alternate Connection for Ground Sensing at the Load (Current Output Models).

In many applications it is impractical to sense the output voltage at ANNALOG COMMON. Sensing the output voltage at the system ground point is permissible because these converters have separate analog and digital common lines and the analog return current is a near-constant 2mA and varies by only 10μA to 20μA over the entire input code range. R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 is constant and appears as a zero error that can be nulled with the zero calibration adjustment.

Another approach senses the output at the load as shown in Figure 9. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection across R_L. The effect of R_4 is negligible as explained previously.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small flux-capture cross section for any external field.

ENVIRONMENTAL SCREENING

/QM Screening

All BH and SH models are available with Burr-Brown's /QM environmental screening for enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

SCREENING FLOW FOR /QM MODELS

Screen	MIL-STD-883 Method	Condition	Comments
Internal Visual	2017	B	
High Temperature Storage (Stabilization Bake)	1008	C	+150°C, 24hrs
Temperature Cycling	1010	C	−65 to +150°C, 10 cycles
Burn-in	1015	B	+125°C, 160hrs
Constant Acceleration 28-pin pkg. 24-pin pkg.	2001	 B E	 10,000G 30,000G
Hermeticity Fine Leak 28-pin pkg. 24-pin pkg. Gross Leak	 1014 1014	 A1 or A2 C	 2×10^{-7} atmcc/sec 5×10^{-8} atmcc/sec 60psig, 2hr
External Visual	2009		

APPLICATIONS

LOADING THE DAC709 SERIALLY ACROSS AN ISOLATION BARRIER

A very useful application of the DAC709 is in achieving low-cost isolation that preserves high accuracy. Using the serial input feature of the input register pair, only three signal lines need to be isolated. The data is applied to pin 11 in a serial bit stream, MSB first. The WR input is used as a data strobe, clocking in each data bit. A RESET signal is provided for system startup and reset. These three signals are each optically isolated. Once the 16 bits of serial data have been strobed into the input register pair, the data is strobed through to the D/A register by the "carry" signal out of a 4-bit binary synchronous counter that has counted the 16 WR pulses used to clock in the data. The circuit diagram is given in Figure 10.

CONNECTING MULTIPLE DAC707s TO A 16-BIT MICROPROCESSOR BUS

Figure 11 illustrates the method of connecting multiple DAC707s to a 16-bit microprocessor bus. The circuit shown has two DAC707s and uses only one address line to select either the input register or the D/A register. An external address decoder selects the desired converter.

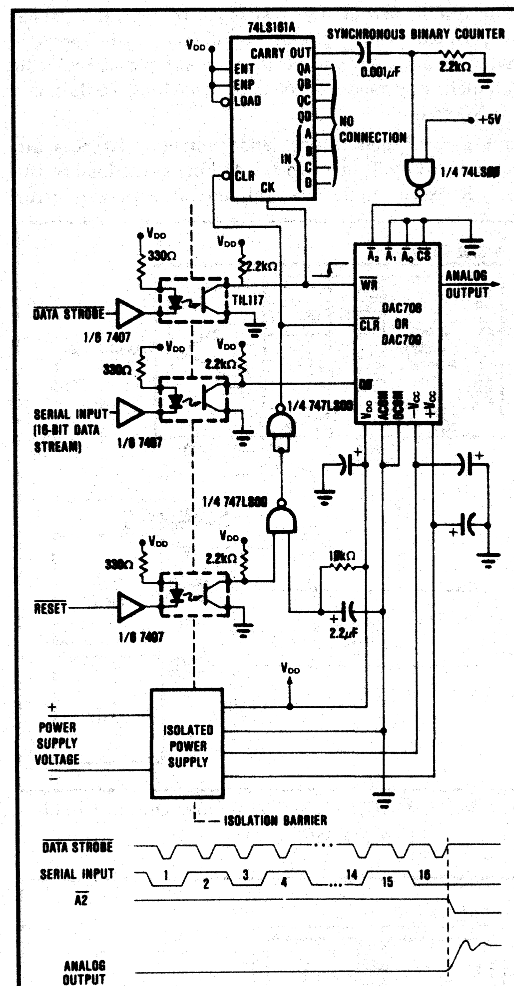


FIGURE 10. Serial Loading of Electrically Isolated DAC708/709.

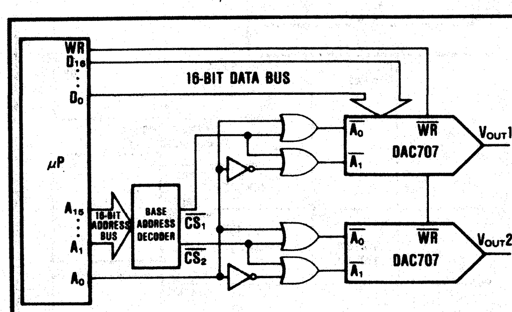
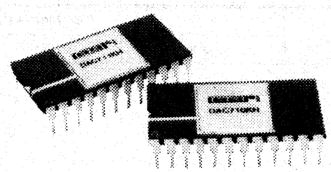


FIGURE 11. Connecting Multiple DAC707s to a 16-Bit Microprocessor.

BURR-BROWN®

DAC710
DAC711



Monolithic 16-Bit
ROBOTICS DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- **DESIGNED SPECIFICALLY FOR CLOSED-LOOP SERVO-CONTROL APPLICATIONS**
- **MONOTONIC TO 15 BITS OVER TEMPERATURE**
- **MONOLITHIC CONSTRUCTION**
- **V_{OUT} AND I_{OUT} MODELS**
- **PIN-COMPATIBLE WITH DAC702, DAC703**
- **VERY-LOW COST FOR MULTIPLE-CHANNEL APPLICATIONS**

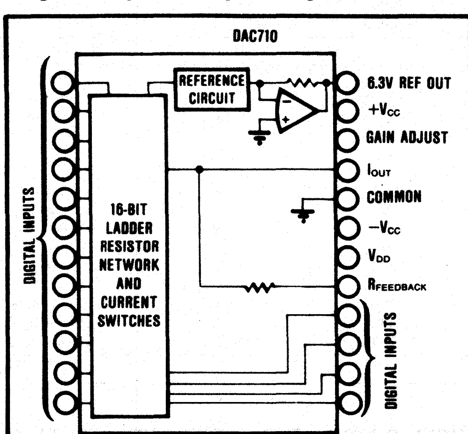
DESCRIPTION

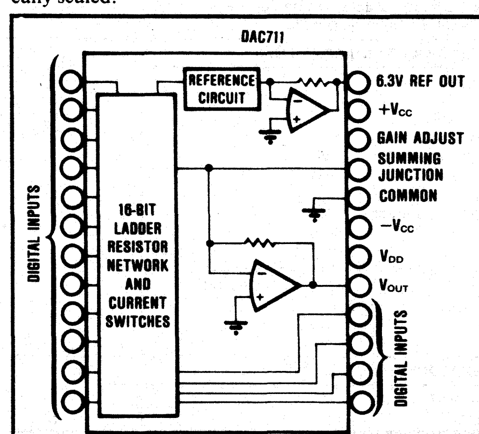
Robotics, numerical controllers, and other applications that involve the driving of servomotors require D/A converters that have very-good differential linearity around the zero output point. The DAC710KH (current output) and DAC711KH (voltage output) have been optimized for this characteristic.

DAC710 and DAC711 are complete 16-bit D/A converters on one chip. They include a precision buried-zener voltage reference, a fast settling operational amplifier (DAC711 only) as well as the D/A converter circuits. A combination of current switch design techniques accomplishes a guaranteed monotonicity of 15 bits around Bipolar Zero over the entire specification temperature range, 0°C to +70°C.

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C-, and 54/74HC-compatible over the entire temperature range. Outputs are ±10V for the DAC711KH and ±1mA for the DAC710KH.

This D/A family is pin-compatible with the voltage and current output DAC703 and DAC702 model families. These D/A converters are packaged in 24-pin ceramic side-brazed packages that are hermetically sealed.





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SPECIFICATIONS

ELECTRICAL

At $T_A = +25°C$ and rated power supplies and after 10 minutes of warm-up time unless otherwise noted.

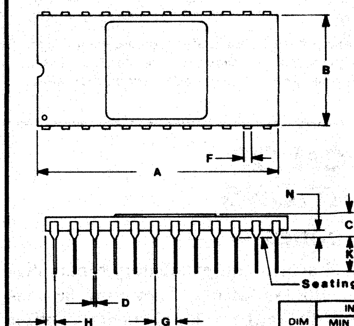
MODEL	DAC710KH/DAC711KH			UNITS
	MIN	TYP	MAX	
INPUT				
DIGITAL INPUT				
Resolution			16	Bits
Digital Inputs[1]: V_{IH}	+2.4		$+V_{CC}$	V
V_{IL}	−1.0		+0.8	V
I_{IH}, $V_I = +2.7V$			+40	μA
I_{IL}, $V_I = +0.4V$		−0.35	−0.5	mA
TRANSFER CHARACTERISTICS				
ACCURACY[2]				
Differential Linearity Error (near bipolar zero)[4][5]			+0.006, −0.003	% of FSR[3]
Monotonicity (near bipolar zero)[4]	15			Bits
Linearity Error			±0.0045	% of FSR
Gain Error[6]		±0.15	±0.30	%
Bipolar Zero Error[6][7]		±0.05	±0.1	% of FSR
DRIFT (over specification temperature range)				
Differential Linearity Error (near bipolar zero) over Temperature[4][5]			+0.009, −0.003	% of FSR
Monotonicity (near bipolar zero) over Temperature[4]	15			Bits
Linearity Error over Temperature			±0.009	% of FSR
Gain Drift		±25	±50	ppm/°C
Bipolar Zero Drift		±5	±12	ppm of FSR/°C
SETTLING TIME (to ±0.003% of FSR)[8]				
DAC711 (V_{OUT} Models)				
Full Scale Step (2kΩ load)		4	8	μsec
For 1LSB Step Change at Worst-Case Code[9]		2.5	4	μsec
Slew Rate		10		V/μsec
DAC710 (I_{OUT} Models)				
Full Scale Step (2mA): 10Ω to 100Ω load		350		nsec
1kΩ load		1		μsec
OUTPUT				
VOLTAGE OUTPUT				
DAC711		±10		V
Output Current	±5			mA
Output Impedance		0.15		Ω
Short Circuit to Common Duration		Indefinite		
CURRENT OUTPUT				
DAC710				
Output Range (±30% typ)		±1		mA
Output Impedance (±30% typ)		4.0		kΩ
Compliance	−2.5		+2.5	V
REFERENCE VOLTAGE				
Voltage		+6.3		V
Source Current Available for External Loads		+2.5		mA
Short Circuit to Common Duration		Indefinite		
POWER SUPPLY REQUIREMENTS				
Voltage: $+V_{CC}$	+13.5	+15	+16.5	V
$-V_{CC}$	−13.5	−15	−16.5	V
V_{DD}	+4.5	+5	+16.5	V
Current: (No Load)				
DAC711 (V_{OUT} Model): $+V_{CC}$		+16	+30	mA
$-V_{CC}$		−18	−30	mA
V_{DD}		+4	+8	mA
DAC710 (I_{OUT} Model): $+V_{CC}$		+10	+25	mA
$-V_{CC}$		−13	−25	mA
V_{DD}		+4	+8	mA
Power Dissipation ($V_{DD} = +5.0V$)[10]: DAC711		530	940	mW
DAC710		365	790	mW
Power Supply Rejection: $+V_{CC}$		±0.003	±0.006	% of FSR/%V_{CC}
$-V_{CC}$		±0.003	±0.006	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001	% of FSR/%V_{DD}
TEMPERATURE RANGE				
Specification	0		+70	°C
Storage	−60		+150	°C

NOTES: (1) Digital inputs are TTL-, LSTTL-, 54/74C-, 54/74HC-, and 54/74HTC-compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. As logic "0" and logic "1" inputs vary over 0V to +0.8V and +2.4V to +10V, respectively, the change in the D/A converter output voltage will not exceed ±0.006% of FSR. (2) DAC710KH is specified and tested with an external output operational amplifier using the internal feedback resistor in all parameters except settling time. (3) FSR means Full Scale Range and is 20V for the DAC711KH and 2mA for the DAC710KH. (4) This specification is for ±2048 consecutive codes around the bipolar zero code; that is, from $77FF_H$ to $87FF_H$. (5) ±0.003% of FSR is 1LSB for 15-bit resolution. (6) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (7) Error at input code $7FFF_H$, bipolar zero. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$. (10) Power dissipation is an additional 40mW when V_{DD} is operated at +15V.

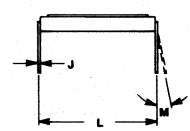
PIN ASSIGNMENTS

Pin No.	Function: DAC710	Function: DAC711
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	$R_{FEEDBACK}$	V_{OUT}
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	I_{OUT}	Summing Junction (Zero Adjust)
22	Gain Adjust	Gain Adjust
23	$+V_{CC}$	$+V_{CC}$
24	+6.3V Ref. Out.	+6.3V Ref. Out.

MECHANICAL

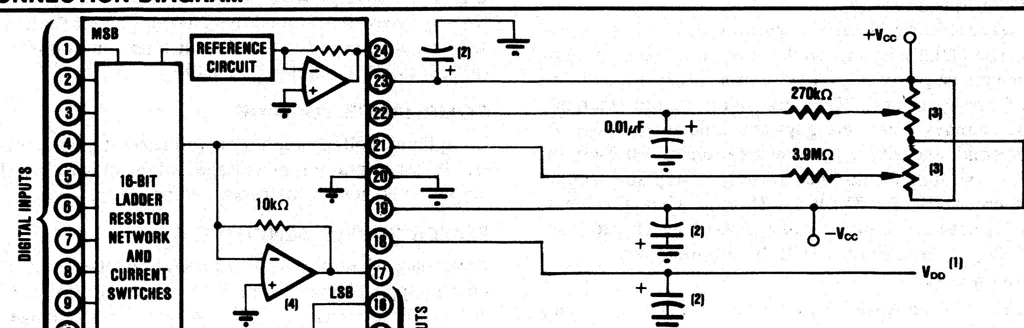


NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.185	1.215	30.10	30.86
B	.600	.620	15.24	15.75
C	.125	.171	3.18	4.34
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

CONNECTION DIAGRAM



NOTES:
1. CAN BE TIED TO $+V_{CC}$ INSTEAD OF HAVING SEPARATE V_{DD} SUPPLY.
2. DECOUPLING CAPACITORS ARE 0.1μF TO 1.0μF, TANTALUM.
3. POTENTIOMETERS ARE 10kΩ TO 100kΩ.
4. AMPLIFIER IN DAC711 ONLY.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON	0V to +18V
$+V_{CC}$ to COMMON	0V to +18V
$-V_{CC}$ to COMMON	0V to −18V
Digital Data Inputs (pins 1-16) to COMMON	−1V to +18V
Reference out (pin 24) to COMMON	Indefinite Short to COMMON
External Voltage Applied to R_F (pin 21, DAC710KH)	±18V
External Voltage Applied to D/A Output (pin 17, DAC711KH)	−5V to +5V
V_{OUT} (pin 17, DAC711)	Indefinite Short to COMMON
Power Dissipation	1000mW
Storage Temperature	−60°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC710/711KH accept complementary binary digital input codes in bipolar format. They may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

ACCURACY

Linearity

Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity

For servomotor control applications, differential linearity error (DLE) is one of the most important performance measures of a D/A converter. DLE is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of +0.006% of FSR maximum means that an output step size can be between 1LSB and 3LSB (at 15 bits) when the input changes between adjacent codes. A DLE specification of −0.003% maximum ensures 15-bit monotonicity.

Monotonicity

When a D/A converter is monotonic, the analog output increases or remains the same for an increasing input digital code. For ±2048 consecutive codes around bipolar zero, the DAC710KH and DAC711KH are monotonic to 15 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts-per-million per degree centigrade (ppm/°C). Gain drift is established by (1) testing the end point difference for each D/A at t_{min}, +25°C and t_{max} (2) calculating the gain error with respect to the +25°C value, and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with $7FFF_H$ (bipolar zero) applied to the digital inputs. This code corresponds to 0V (DAC711KH) or 0mA (DAC710KH) at the analog output. The maximum change in offset at t_{min} or t_{max} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in parts-per-million of full-scale range per degree centigrade (ppm of FSR/°C).

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output	
	Complementary Offset Binary (COB)	*Complementary Two's Complement (CTC)
0000_H	+ Full Scale	−1LSB
$7FFF_H$	Bipolar Zero	− Full Scale
8000_H	−1LSB	+ Full Scale
$FFFF_H$	− Full Scale	Bipolar Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

SETTLING TIME

Settling time of the D/A is the total time required for the output to settle within an error band around its final value after a change in input. Refer to Figure 1 for typical values.

Voltage Output, DAC711KH

Settling times are specified to ±0.003% of FSR for two input conditions: a full-scale range change of 20V and a ±0.006% of FSR (±1LSB in 14 bits) change at the major carry, the point at which the worst-case setting time occurs.

Current Output, DAC710KH

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output while maintaining specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2).

REFERENCE SUPPLY

All models have an internal +6.3V reference voltage derived from an on-chip buried-zener diode. This reference voltage, available at pin 24, has a tolerance of ±5%. A minimum of 1.5mA is available for external loads. Gain and Zero adjustments should be made under constant load conditions.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the bipolar offset (connected internally to the reference) from load variations.

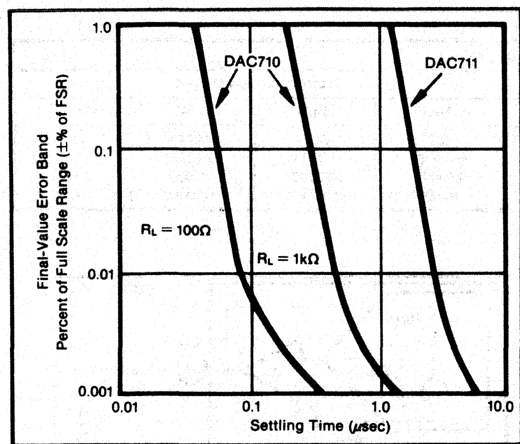


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

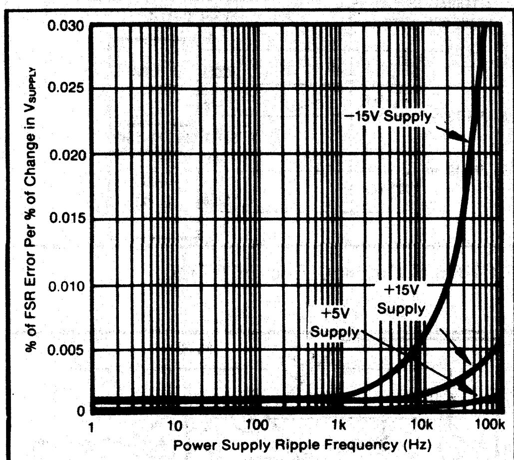


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. The 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor should be connected (even if GAIN ADJUST is not used) from GAIN ADJUST (pin 22) to COMMON to prevent noise pickup. Refer to Figure 4 for the relationship of zero and gain adjustments.

Zero Adjustment

Apply the digital input code ($7FFF_H$) that produces zero output voltage or current. See Table II for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before Gain calibration.

Gain Adjustment

Apply the digital input code (0000_H) that gives the maximum positive output voltage or current. Adjust the gain potentiometer for this positive full-scale voltage or current. See Table II for positive full-scale values and the Connection Diagram for gain adjustment circuit connections.

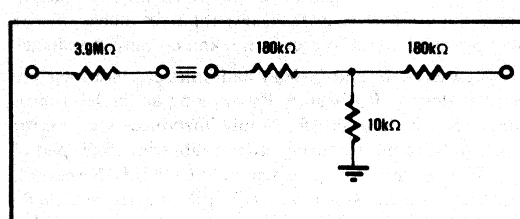


FIGURE 3. Equivalent Resistances.

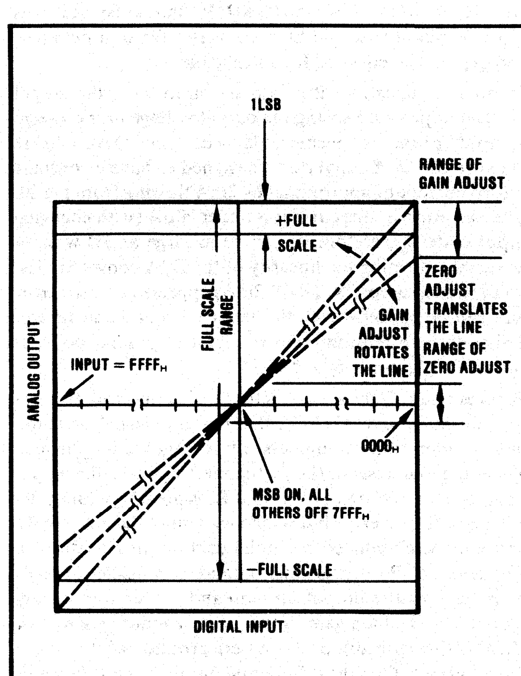


FIGURE 4. Relationship of Zero and Gain Adjustments.

TABLE II. Digital Input and Analog Output Relationships.

Digital Input Code	Analog Output							
	DAC710 Current Output				DAC711 Voltage Output			
	16-bit	15-bit	14-bit	Units	16-bit	15-bit	14-bit	Units
1LSB	0.031	0.061	0.122	μA	305	610	1224	μV
0000_H	−0.99997	−0.99994	−0.99988	mA	+9.99960	+9.99939	+9.99878	V
$7FFF_H$	0.00000	0.00000	0.00000	mA	0.00000	0.00000	0.00000	V
$FFFF_H$	+1.00000	+1.00000	+1.00000	mA	−10.0000	−10.0000	−10.0000	V

INSTALLATION CONSIDERATIONS

Due to the extremely high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Ignoring contact resistance, less than six inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 5, 6, and 7, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance (R_L) is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at COMMON (pin 20), and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at pin 20. Sensing the output voltage at the system ground point is permissible with the DAC710/711 because the D/A converter is designed to have a constant return current of approximatley 2mA flowing from pin 20. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times 2$mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 5, 6, and 7.

Figures 6 and 7 show two methods of connecting the current output model (DAC710KH) with external precision output operational amplifiers. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain. If the output cannot be sensed at COMMON (pin 20), or the system ground point as mentioned above, then the differential output circuit shown in Figure 7 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 7 can be reduced to the one shown in Figure 6. Again, the effect of R_4 is negligible.

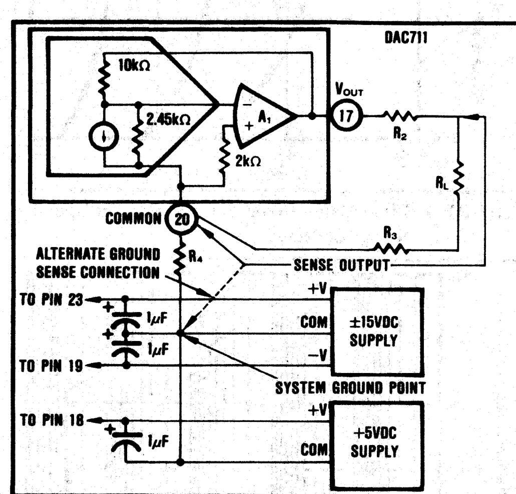


FIGURE 5. Output Circuit for DAC711.

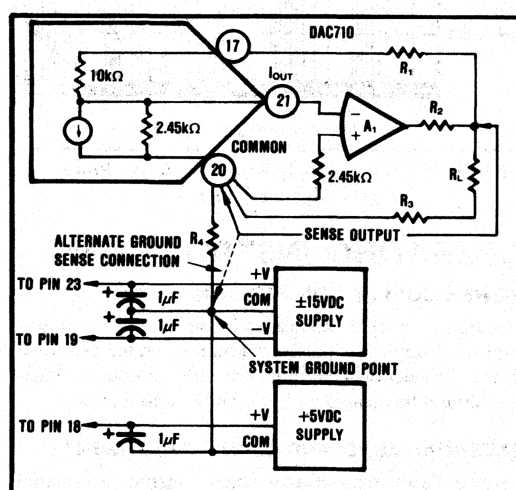


FIGURE 6. Preferred External Op Amp Configuration for DAC710.

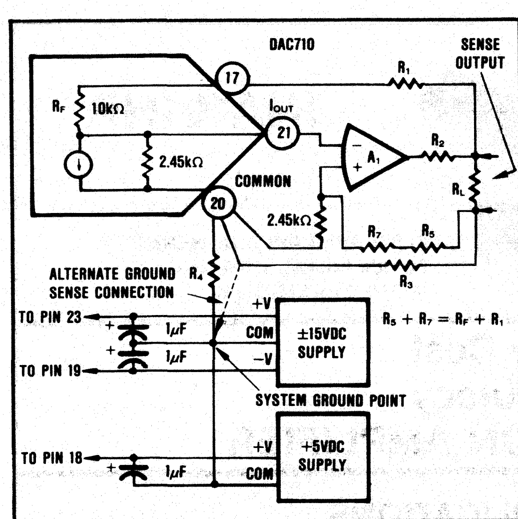


FIGURE 7. Differential Sensing Output Op Amp Configuration for DAC710.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation pickup is small loop area. If a signal lead and its return conductor are wired close together, they present a small flux-capture cross section for external fields.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT D/A'S

DAC710KH is a current output device and will drive the summing junction of an op amp to produce an output voltage as shown in Figure 8. Use of the internal feedback resistor (pin 17) is required to obtain specified gain accuracy and low gain drift.

DAC710KH can be scaled for any desired voltage range with an external feedback resistor at the expense of increased drift with temperature. The resistors in the DAC710KH ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 9.

OUTPUTS LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use an I_{OUT} value of ±1mA to calculate the output voltage range (see Figure 10). Use protection diodes as shown when a high voltage op amp is used.

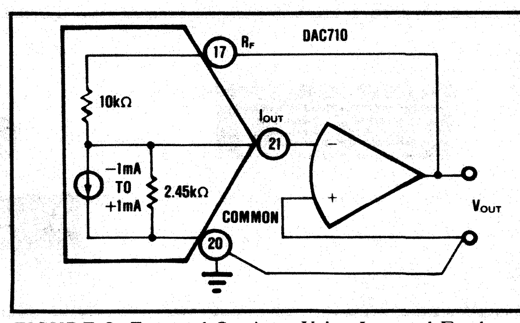


FIGURE 8. External Op Amp Using Internal Feedback Resistors (DAC710).

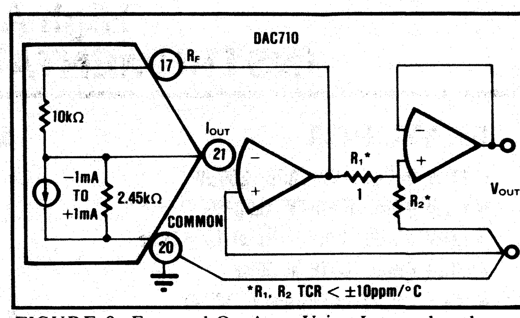


FIGURE 9. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift (DAC710).

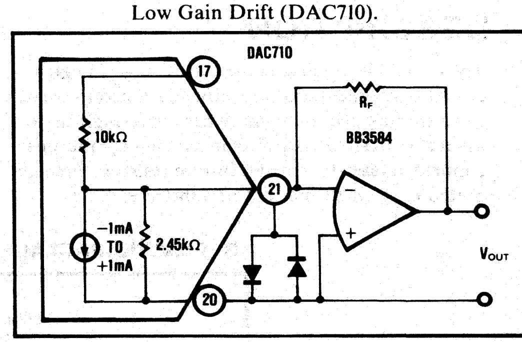


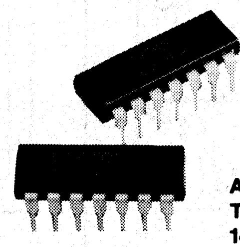
FIGURE 10. External Op Amp Using External Feedback Resistors (DAC710).

ORDERING INFORMATION

Model	Package	Temp. Range	Output
DAC710KH	Hermetic Ceramic	0°C to +70°C	Current, ±1mA
DAC711KH	Hermetic Ceramic	0°C to +70°C	Voltage, ±10V

BURR-BROWN®

INA101HP



ALSO AVAILABLE IN HERMETIC TO-100 METAL CAN AND 14-PIN CERAMIC DIP

Very-Low Cost High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 250μV
- LOW NONLINEARITY: 0.002%
- LOW NOISE: 13nV/$\sqrt{Hz}$ at f_O = 1kHz
- HIGH CMR: 100dB at 60Hz
- HIGH INPUT IMPEDANCE: $10^{10}\Omega$
- LOW COST

APPLICATIONS

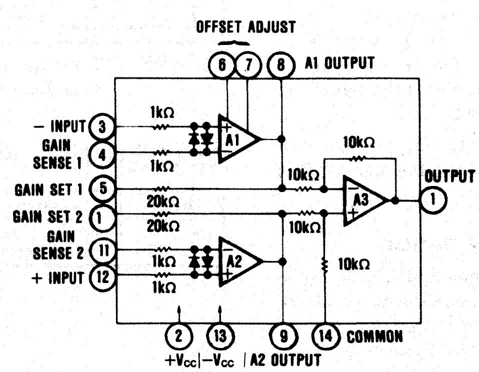
- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS: Strain Gages
  Thermocouples
  RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS
- MEDICAL INSTRUMENTATION

DESCRIPTION

The INA101 is a high-accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very-high performance is desired. All circuits, including the interconnected laser-trimmed thin-film resistors, are integrated on a single monolithic substrate.

A multiamplifier design is used to provide the highest performance and maximum versatility with monolithic construction for low cost. The input stage uses Burr-Brown's ultra-low-drift, low-noise technology to provide exceptional input characteristics.

"P" PLASTIC PACKAGE



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SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply.

MODEL	INA101HP			
	MIN	TYP	MAX	UNITS
GAIN				
Range of Gain	1		1000	V/V
Gain Equation		G = 1 + (40k/R_G)		V/V
Error From Equation, DC(1)		±(0.1 + 0.00015G − 0.05/G)	±(0.3 + 0.0002G − 0.10/G)	%
Gain Temp. Coefficient(2)				
G = 1		2	5	ppm/°C
G = 10		20	100	ppm/°C
G = 100		22	110	ppm/°C
G = 1000		22	110	ppm/°C
Nonlinearity, DC(3)		±(0.002 + 10^{-6}G)	±(0.005 + 2 × 10^{-6}G)	% of p-p FS
RATED OUTPUT				
Voltage	±10	±12.5		V
Current	±5	±10		mA
Output Impedance		0.2		Ω
INPUT OFFSET VOLTAGE				
Initial Offset at +25°C(4)		±(125 + 450/G)	±(250 + 900/G)	μV
vs. Temperature		±(2 + 20/G)		μV/°C
vs. Supply		±(1 + 20/G)		μV/V
vs. Time		±(1 + 20/G)		μV/mo
INPUT BIAS CURRENT				
Initial Bias Current (each input)		±15	±30	nA
vs. Temperature		±0.2		nA/°C
vs. Supply		±0.1		nA/V
Initial Offset Current		±15	±30	nA
vs. Temperature		±0.5		nA/°C
INPUT IMPEDANCE				
Differential		10^{10} ∥ 3		Ω ∥ pF
Common-mode		10^{10} ∥ 3		Ω ∥ pF
INPUT VOLTAGE RANGE				
Range, Linear Response	±10			V
CMR with 1kΩ Source Imbal.				
DC to 60Hz, G = 1	65	85		dB
DC to 60Hz, G = 10	90	95		dB
DC to 60Hz, G = 100 to 1000	100	105		dB
INPUT NOISE				
Input Voltage Noise				
f_B = 0.01Hz to 10Hz		0.8		μV, p-p
Density, G = 1000: f_o = 10Hz		18		nV/√Hz
f_o = 100Hz		15		nV/√Hz
f_o = 1kHz		13		nV/√Hz
Input Current Noise				
f_B = 0.01Hz to 10Hz		50		pA, p-p
Density: f_o = 10Hz		0.8		pA/√Hz
f_o = 100Hz		0.46		pA/√Hz
f_o = 1kHz		0.35		pA/√Hz
DYNAMIC RESPONSE				
Small Signal, ±3dB Flatness				
G = 1		300		kHz
G = 10		140		kHz
G = 100		25		kHz
G = 1000		2.5		kHz
Small Signal, ±1% Flatness				
G = 1		20		kHz
G = 10		10		kHz
G = 100		1		kHz
G = 1000		200		Hz
Full Power, G = 1 to 100		6.4		kHz
Slew Rate, G = 1 to 100	0.2	0.4		V/μsec
Settling Time (0.1%)				
G = 1		30	40	μsec
G = 100		40	55	μsec
G = 1000		35	470	μsec
Settling Time (0.01%)				
G = 1		30	45	μsec
G = 100		50	70	μsec
G = 1000		500	650	μsec
POWER SUPPLY				
Rated Voltage		±15		V
Voltage Range	±5		±20	V
Current, Quiescent		±6.7	±8.5	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operation	−25		+85	°C
Storage	−25		+85	°C

NOTES: (1) Typically the tolerance of R_G will be the major source of gain error. (2) Not including the TCR of R_G. (3) Nonlinearity is the maximum peak deviation from the best straight-line as a percent of peak-to-peak full scale output. (4) Adjustable to zero at any one gain.

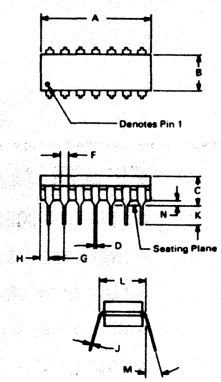
ABSOLUTE MAXIMUM RATINGS

Supply	±20V
Internal Power Dissipation	600mW
Input Voltage Range	±V_{CC}
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−25°C to +85°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration	Continuous to ground

MECHANICAL

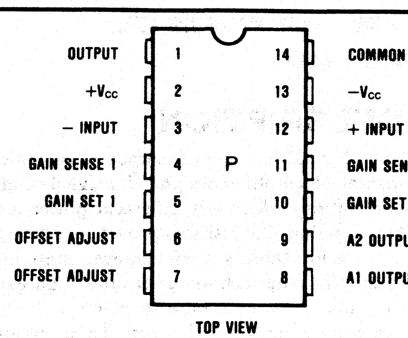
EPOXY DUAL-IN-LINE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.660	.785	16.76	19.94
B	.220	.280	5.59	7.11
C	–	.200	–	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095		
J	.008	.015	0.20	0.38
K	.100	–	2.54	–
L	.300 BASIC		7.62 BASIC	
M	–	15°	–	15°
N	.020	.050	0.51	1.27

PIN CONFIGURATION



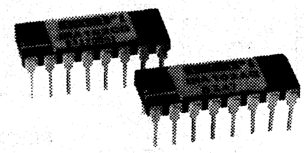
ORDERING INFORMATION

INA101 H P

Basic Model Number — INA101
Performance Grade — H
H = 0°C to +70°C
Package Code — P
P = 14-pin plastic DIP

BURR-BROWN®

INA102



Low Power
High Accuracy
INSTRUMENTATION AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 750μA, max
- INTERNAL GAINS: X 1, 10, 100, 1000
- LOW GAIN DRIFT: 5ppm/°C, max
- HIGH CMR: 90dB, min
- LOW OFFSET VOLTAGE DRIFT: 2μV/°C, max
- LOW OFFSET VOLTAGE: 100μV, max
- LOW NONLINEARITY: 0.01%, max
- HIGH INPUT IMPEDANCE: $10^{10}\Omega$
- LOW COST

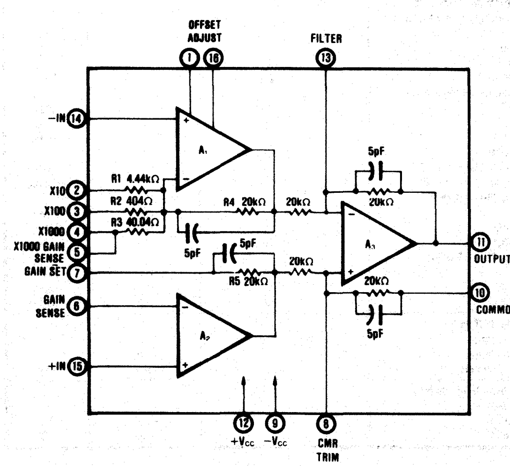
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gauges
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCER AMPLIFIER
- LOW LEVEL SIGNAL AMPLIFIER
- MEDICAL INSTRUMENTATION
- MULTICHANNEL SYSTEMS
- BATTERY POWERED EQUIPMENT

DESCRIPTION

The INA102 is a high-accuracy monolithic instrumentation amplifier designed for signal conditioning applications where low quiescent power is desired. On-chip thin-film resistors provide excellent temperature and stability performance. State-of-the-art laser trimming technology insures high gain accuracy and common-mode rejection while avoiding expensive external components. These features make the INA102 ideally suited for battery powered and high volume applications.

The INA102 is also convenient to use. A gain of 1, 10, 100, or 1000 may be selected by simply strapping the appropriate pins together. 5ppm/°C gain drift in low gains can then be achieved without external adjustment. When higher than specified CMR is required, CMR can be trimmed using the pins provided. In addition, balanced filtering can be accomplished in the output stage.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At $T_A = +25°C$ with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

MODEL		INA102AG			INA102CG			
	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN								
Range of Gain		1		1000	*		*	V/V
Gain Equation			$G = 1 + (40k/R_G)$[1]			*		V/V
Error, DC: G = 1	$T_A = +25°C$		±0.01	±0.1		±0.01	±0.05	%
G = 10	$T_A = +25°C$		±0.02	±0.1		±0.02	±0.05	%
G = 100	$T_A = +25°C$		±0.1	±0.25		±0.07	±0.15	%
G = 1000	$T_A = +25°C$		±0.15	±0.75		±0.08	±0.5	%
G = 1	$T_A = T_{min}$ to T_{max}			±0.16			±0.08	%
G = 10	$T_A = T_{min}$ to T_{max}			±0.19			±0.11	%
G = 100	$T_A = T_{min}$ to T_{max}			±0.37			±0.21	%
G = 1000	$T_A = T_{min}$ to T_{max}			±0.93			±0.62	%
Gain Temp. Coefficient								
G = 1			±1	±10		±1	±5	ppm/°C
G = 10			±2.5	±15		±1.5	±10	ppm/°C
G = 100			±3	±20		±2	±15	ppm/°C
G = 1000			±5	±30		±4	±20	ppm/°C
Nonlinearity, DC								
G = 1	$T_A = +25°C$		±0.005	±0.03		±0.002	±0.01	% of FS
G = 10	$T_A = +25°C$		±0.005	±0.03		±0.002	±0.01	% of FS
G = 100	$T_A = +25°C$		±0.01	±0.05		±0.006	±0.02	% of FS
G = 1000	$T_A = +25°C$		±0.015	±0.1		±0.01	±0.05	% of FS
G = 1	$T_A = T_{min}$ to T_{max}			±0.045			±0.015	% of FS
G = 10	$T_A = T_{min}$ to T_{max}			±0.045			±0.015	% of FS
G = 100	$T_A = T_{min}$ to T_{max}			±0.075			±0.03	% of FS
G = 1000	$T_A = T_{min}$ to T_{max}			±0.15			±0.1	% of FS
RATED OUTPUT								
Voltage	$R_L = 10kΩ$	$\pm\lvert V_{CC}\rvert - 3.5$			*			V
Current		±1			*			mA
Short-Circuit Current			±2			*		mA
Output Impedance								
G = 1000			0.1			*		Ω
INPUT								
OFFSET VOLTAGE								
Initial Offset[2]	$T_A = +25°C$		±(30 + 30/G)	±(300 + 300/G)		50	±(100 + 200/G)	μV
vs Temperature			±(1 + 2/G)	±(5 + 10/G)		±(0.5 + 1/G)	±(2 + 5/G)	μV/°C
vs Supply			±(8 + 10/G)	±(40 + 50/G)		±(2 + 5/G)	±(10 + 20/G)	μV/V
vs Time			±(20 + 30/G)			*		μV/mo
BIAS CURRENT								
Initial Bias Current								
(each input)	$T_A = T_{min}$ to T_{max}		+16	+50		+16	+30	nA
vs Temperature			±0.1			*		nA/°C
vs Supply			±0.1			*		nA/V
Initial Offset Current	$T_A = T_{min}$ to T_{max}		±0.3	±15		±0.2	±10	nA
vs Temperature			±0.1			*		nA/°C
IMPEDANCE								
Differential			$10^{10}\|\|2$			*		Ω‖pF
Common-mode			$10^{10}\|\|2$			*		Ω‖pF
VOLTAGE RANGE								
Range, Linear Response	$T_A = T_{min}$ to T_{max}	$\pm\lvert V_{CC}\rvert - 3.5$			*			V
CMR with 1kΩ								
Source Imbalance								
G = 1	DC to 60 Hz	80	94		90	94		dB
G = 10	DC to 60 Hz	80	100		90	100		dB
G = 10 to 1000	DC to 60 Hz	80	100		90	100		dB
NOISE								
Input Voltage Noise								
f_B = 0.1Hz to 10Hz			1			*		μV, p-p
Density, G = 1000								
f_o = 10Hz			40			*		nV/√Hz
f_o = 100Hz			30			*		nV/√Hz
f_o = 1kHz			30			*		nV/√Hz
Input Current Noise								
f_B = 0.01Hz to 10Hz			25			*		pA p-p
Density: f_o = 10Hz			0.3			*		pA/√Hz
f_o = 100Hz			0.2			*		pA/√Hz
f_o = 1kHz			0.15			*		pA/√Hz
DYNAMIC RESPONSE								
Small Signal								
±3dB Flatness	$V_{OUT} = 0.1V_{rms}$							
G = 1			300			*		kHz
G = 10			30			*		kHz
G = 100			3			*		kHz
G = 1000			0.3			*		kHz

ELECTRICAL [CONT]

MODEL	CONDITIONS	INA102AG MIN	INA102AG TYP	INA102AG MAX	INA102CG MIN	INA102CG TYP	INA102CG MAX	UNITS
Small Signal,								
±1% Flatness	$V_{OUT} = 0.1V_{rms}$							
G = 1			30			*		kHz
G = 10			3			*		kHz
G = 100			0.3			*		kHz
G = 1000			0.03			*		kHz
Full Power, G = 1 to 100	$V_{OUT}=10V, R_L=10k\Omega$	2.4	3		*	*		kHz
Slew Rate, G = 1 to 100	$V_{OUT}=10V, R_L=10k\Omega$	0.15	0.2		*	*		V/μsec
Settling Time	$R_L=10k\Omega, C_L=100pF$							
0.1%: G = 1	10V step		50			*		μsec
G = 100			360			*		μsec
G = 1000			3300			*		μsec
0.01%: G = 1	10V step		60			*		μsec
G = 100			500			*		μsec
G = 1000			4500			*		μsec
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range	Derated	±3.5		±18	*		*	V
Quiescent Current	$V_O = 0V$, $T_A = T_{min}$ to T_{max}		±500	±750		*	*	μA
TEMPERATURE RANGE								
Specification		−25		+85	*		*	°C
Operation		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C

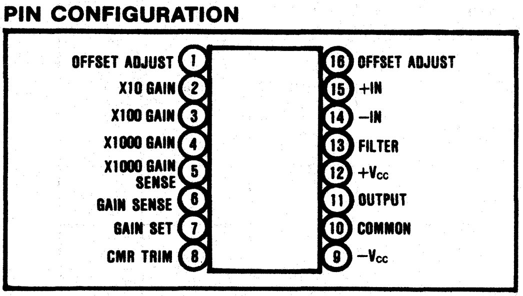
*Specifications same as for INA102AG.

NOTES: (1) The internal gain set resistors have an absolute tolerance of ±20%; however, their typical TCR is ±50ppm/°C. R_G will add to the gain error if gains other than 1, 10, 100 or 1000 are set externally. (2) Adjustable to zero at any one time.

ABSOLUTE MAXIMUM RATINGS

Supply .... ±18V
Input Voltage Range .... $\pm V_{CC}$
Operating Temperature
Range .... −25°C to +85°C
Storage Temperature
Range .... −65°C to +150°C
Lead Temperature
(soldering 10 seconds) .... +300°C
Output Short-Circuit
Duration .... Continuous to ground

PIN CONFIGURATION



ORDERING INFORMATION

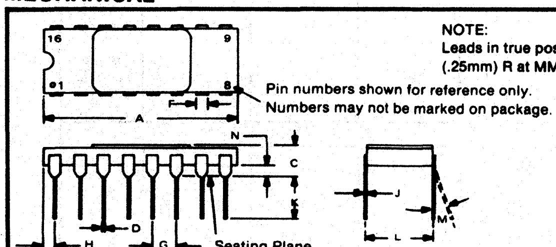
INA102 X G

Basic Model Number
Performance Grade Code
A, C: −25°C to +85°C

Package Code
G: 16-pin Hermetic DIP

INA102AG, INA102CG

MECHANICAL

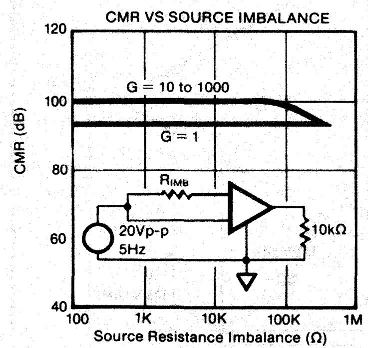


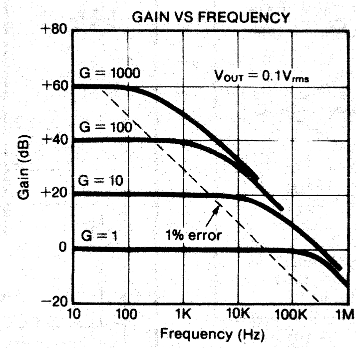
NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

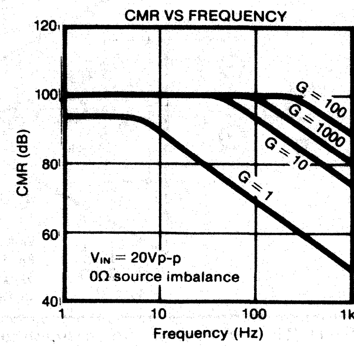
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

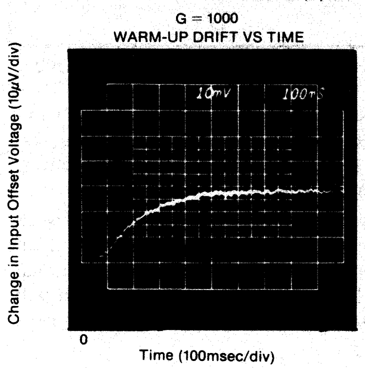
TYPICAL PERFORMANCE CURVES

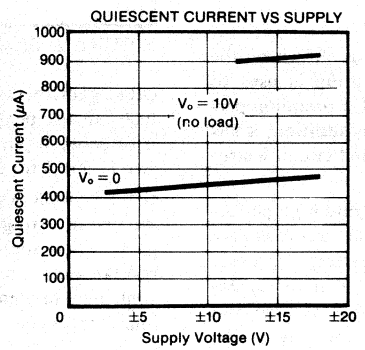
At +25°C and in circuit of Figure 2 unless otherwise noted.

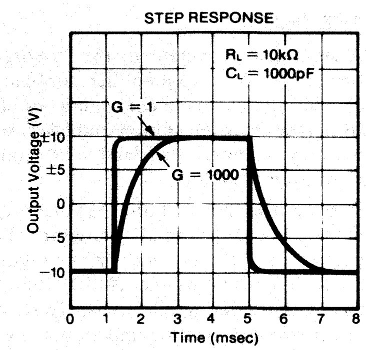


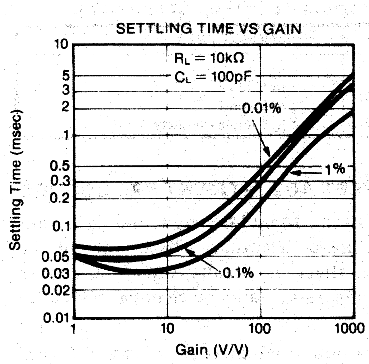


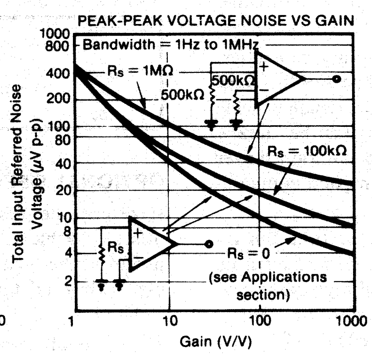


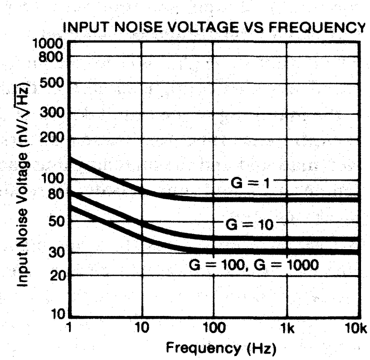












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond mainly to the difference between the two input signals and exhibit extremely-high input impedance, both differential and common-mode. The feedback networks of this instrumentation amplifier are included on the monolithic chip. No external resistors are required for gains of 1, 10, 100 and 1000 in the INA102.

An operational amplifier, on the other hand, is an open-loop, uncommitted device that requries external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems.

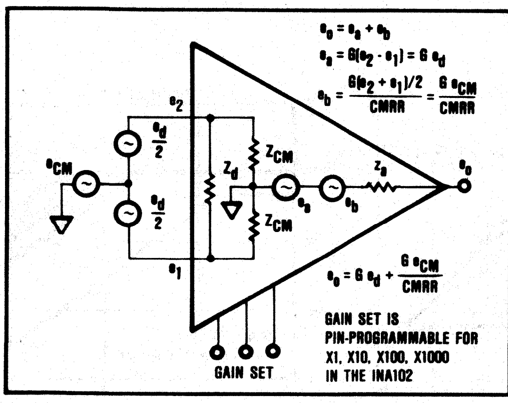


FIGURE 1. Model of an Instrumentation Amplifier.

THE INA102

A simplified schematic of the INA102 is shown on the first page. A three-amplifier configuration is used to provide the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers.

The input buffers (A1 and A2) incorporate high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in instrumentation amplifier applications. The offset voltage and offset voltage versus temperature are low due to the monolithic design, and improved even further by state-of-the-art laser-trimming techniques.

The output stage (A3) is connected in a unity-gain differential amplifier configuration. A critical part of this stage is the matching of the four 20kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain good common-mode rejection.

All of the internal resistors are made of thin-film nichrome on the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability and provides excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA102 is operated over wide temperature ranges.

USING THE INA102

Figure 2 shows the simplest configuration of the INA102. The output voltage is a function of the differential input voltage times the gain.

A gain of 1, 10, 100, or 1000 is selected by programming pins 2 through 7 (see Table I). Notice that for the gain of 1000, a special gain sense is provided to preserve accuracy. Although this is not always required, gain errors caused by external resistance in series with the low value 40.04Ω internal gain set resistor are thus eliminated.

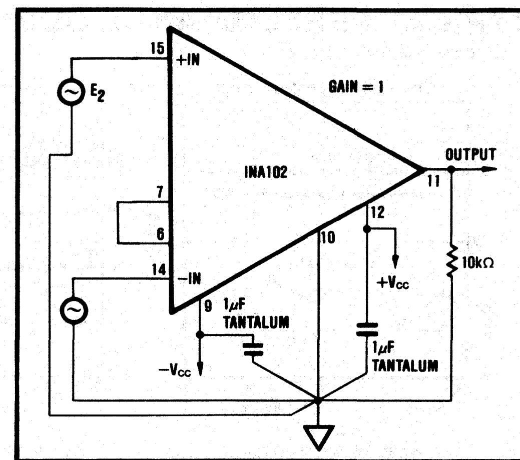


FIGURE 2. Basic Circuit Connection for the INA102.

Other gains between 1 and 10, 10 and 100, and 100 and 1000 can also be obtained by connecting an external resistor between pin 6 and either pin 2, 3, or 4, respectively (see Figure 6 for application).

$G = 1 + (40/R_G)$ where R_G is the total resistance between the two inverting inputs of the input op amps. At high gains, where the value of R_G becomes small, additional resistance (i.e., relays or sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

TABLE I. Pin-Programmable Gain Connections.

GAIN	CONNECT PINS
1	6 to 7
10	2 to 6 and 7
100	3 to 6 and 7
1000	4 to 7 and separately 5 to 6

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is sometimes desirable to null the input and/or output offset to achieve higher accuracy. The quality of the potentiometer will affect the results; therefore, choose one with good temperature and mechanical-resistance stability.

The optional offset null capabilities are shown in Figure 3. R_4 adjustment affects only the input stage component of the offset voltage. Note that the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately 0.31µV/°C per 100µV of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offset correction can be accomplished with A_1, R_1, R_2, and R_3, by applying a voltage to Common (pin 10) through a buffer amplifier. This buffer limits the resistance in series with pin 10 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 100dB. Be certain to keep this resistance low.

It is important to not exceed the input amplifier's

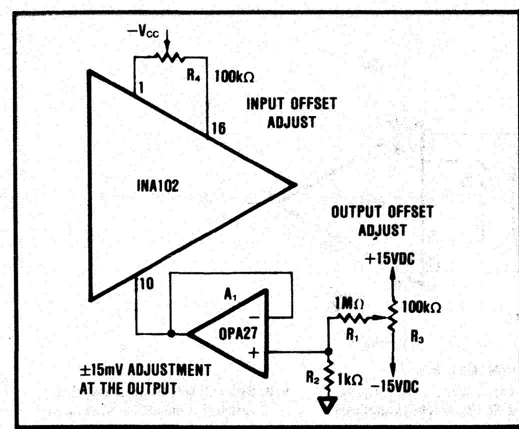


FIGURE 3. Optional Offset Nulling

dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately ±12V with ±15V supplies or nonlinear operation will result.

OPTIONAL FILTERING

The INA102 has provisions for accomplishing filtering with one external capacitor between pins 11 and 13. This single-pole filter can be used to reduce noise outside the signal bandwidth, but with degradation to AC CMR.

When it is important to preserve CMR versus frequency (especially at 60Hz), two capacitors should be used. The additional capacitor is connected between pins 8 and 10. This will maintain a balance of impedances in the output stage. Either of these capacitors could also be trimmed slightly to maximize CMR, if desired. Note that their ratio tracking will affect CMR over temperature.

OPTIONAL COMMON-MODE REJECTION TRIM

The INA102 is laser-adjusted during manufacturing to assure high CMR. However, if desired, a small resistance can be added in series with pin 10 to trim the CMR to an improved level. Depending upon the nature of the internal imbalances, either a positive or negative resistance

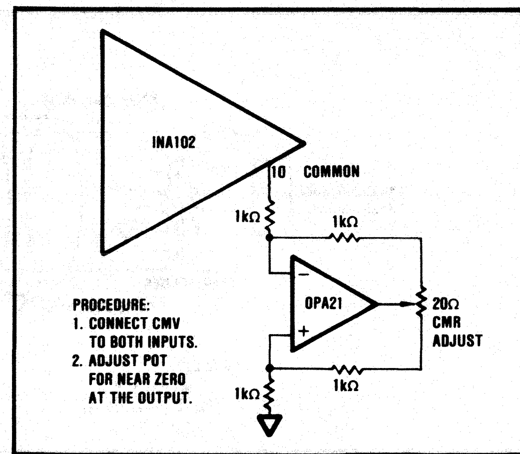


FIGURE 4. Optional Circuit for Externally Trimming CMR.

value could be required. The circuit shown in Figure 4 acts as a bipolar potentiometer and allows easy adjustment of CMR.

TYPICAL APPLICATIONS

Many applications of instrumentaition amplifiers involve the amplification of low level differential signals from bridges and transducers such as strain gauges, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA102 accomplishes all of these with high precision at surprisingly low quiescent current. However, in higher gains (>10) with high source impedances (>100kΩ), the bias current can cause a large offset at the output. This can saturate the output unless the source impedance is separated, e.g., two 500kΩ paths instead of one 1MΩ unbalanced input. The input offset current times 500kΩ will then generate a small DC voltage error.

Figures 5 through 11 show some typical applications circuits.

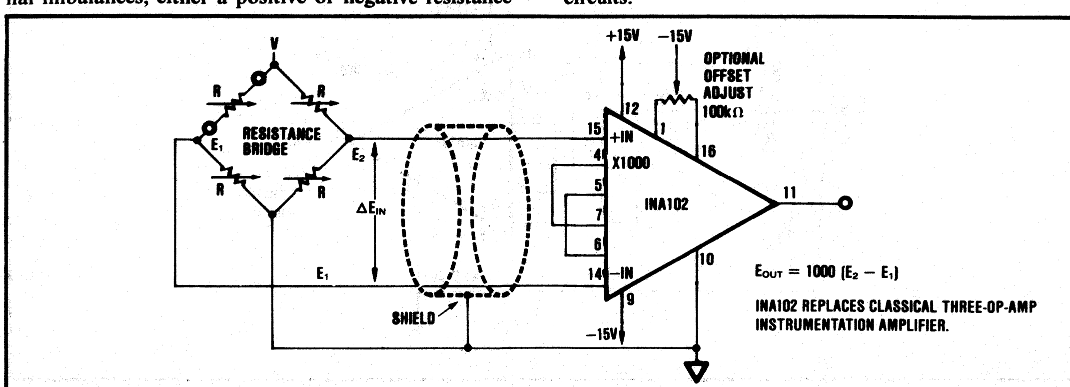


FIGURE 5. Amplification of a Differential Voltage from a Resistance Bridge.

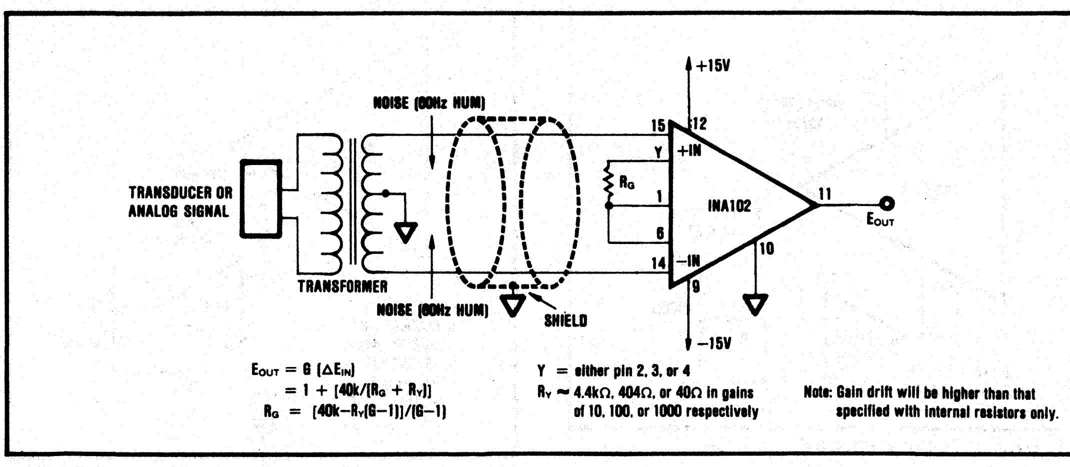


FIGURE 6. Amplification of a Transformer-Coupled Analog Signal Using External Gain Set.

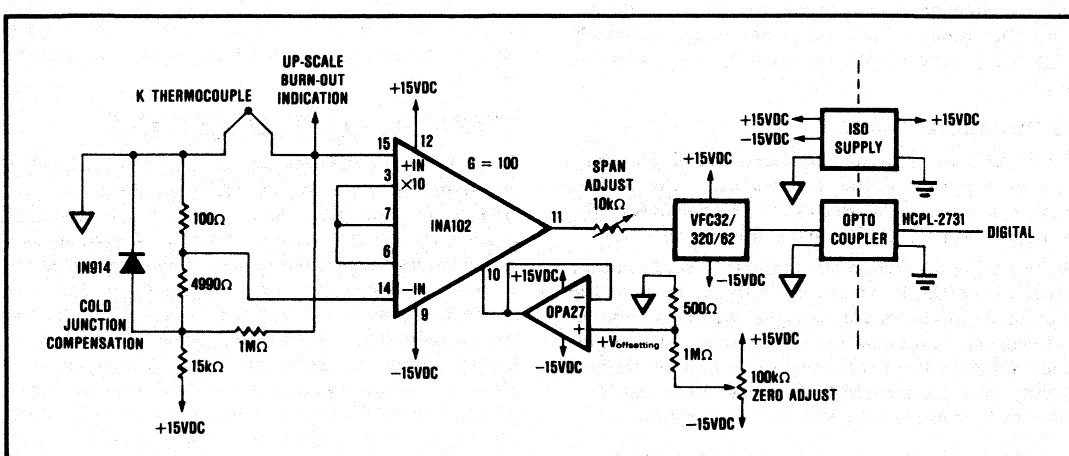


FIGURE 7. Isolated Thermocouple Amplifier with Cold Junction Compensation.

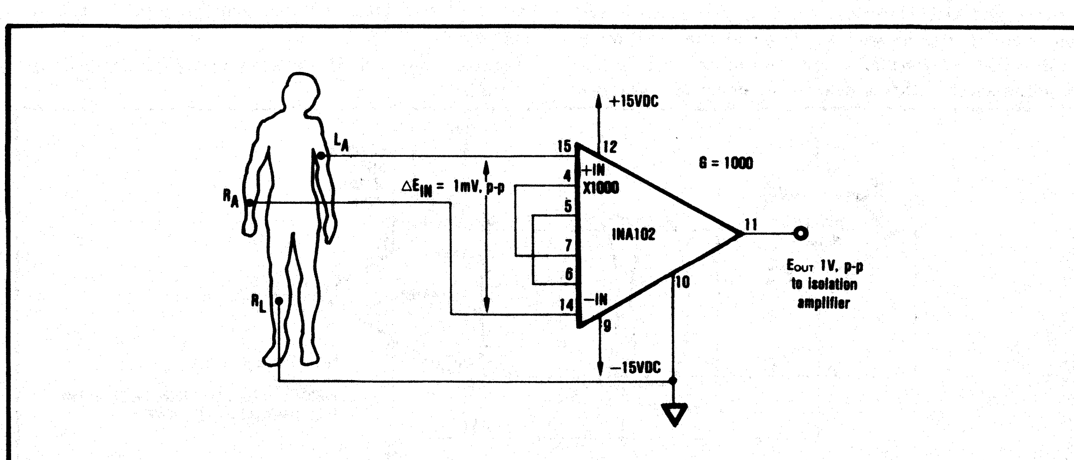


FIGURE 8. ECG Amplifier or Recorder Preamp for Biological Signals.

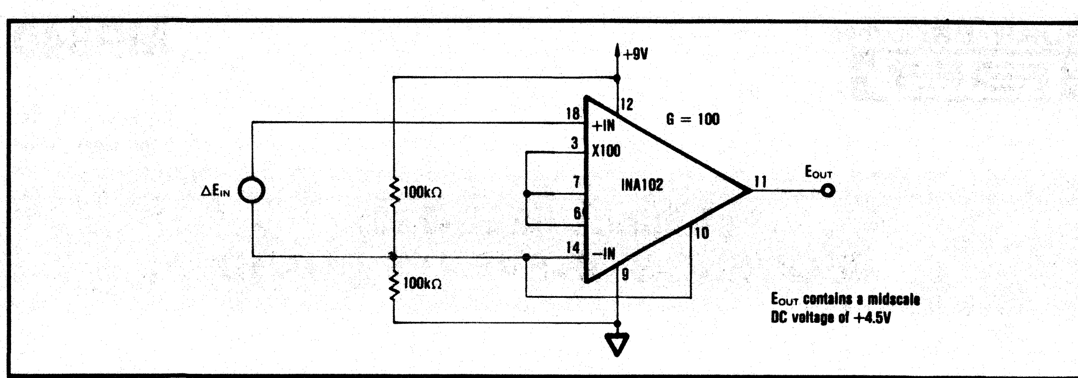


FIGURE 9. Single Supply Low Power Instrumentation Amplifier.

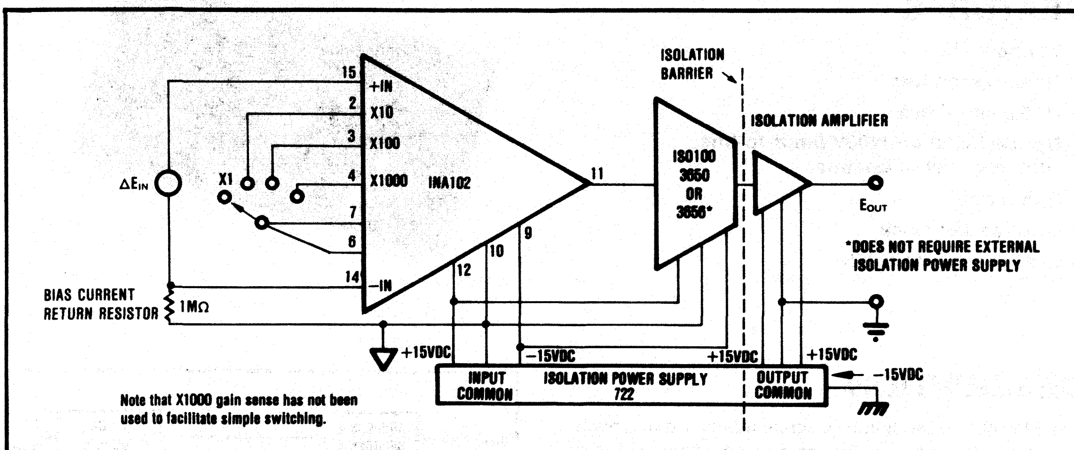


FIGURE 10. Precision Isolated Instrumentation Amplifier.

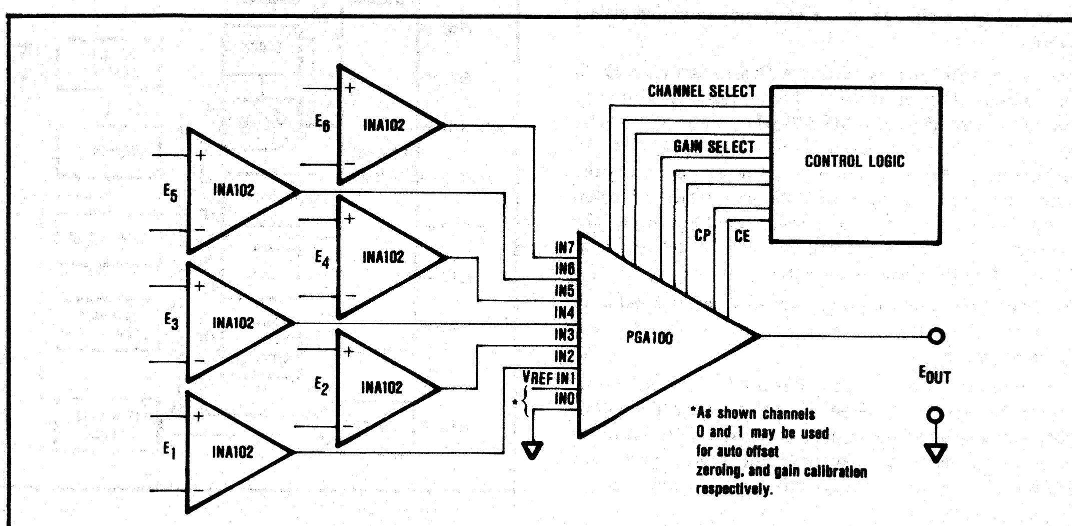


FIGURE 11. Multiple Channel Precision Instrumentation Amplifier.

BURR-BROWN®

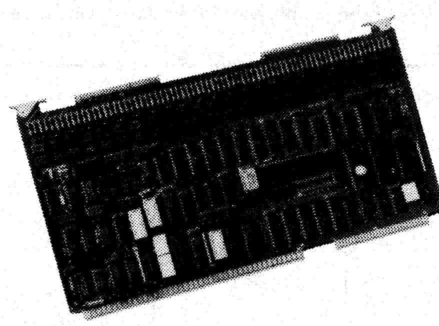
MP840

Effective: 7/1/85
Supersedes: None

Multibus (IEEE-796) SEQUENCE-OF-EVENTS BOARD

FEATURES

- **24 channels**
- **1msec resolution**
- **1100 event times**
- **Optical isolation 1200V input-to-bus, 300V channel-to-channel**
- **Debounce**
- **Time-of-day clock**
- **Clock synchronization**



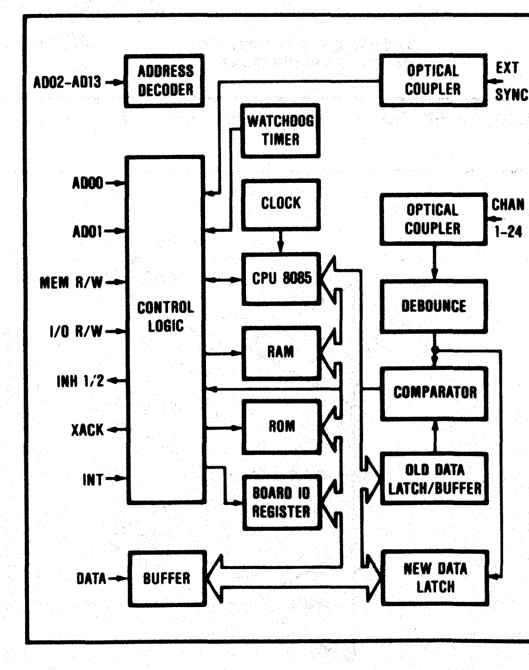
DESCRIPTION

The MP840 is a 24-channel discrete input card that reads the static state of an input or monitors the state of a discrete input and records any change in state of that input. This information records the sequence in which a series of inputs change or the sequence in which events occur.

Events are recorded by setting a flag to indicate which channel has changed state. A flag and polarity for each channel is stored by the MP840 when an event occurs. This data is time-stamped with a Julian day and time to within one millisecond and is held for later access by the system computer. A total of 1100 event times or 26,400 events can be stored by the MP840; unused points can be masked out. The on-board clock can be set and synchronized by the system computer.

The MP840 is reset on power-up, low power condition, bus reset, by software command or by an on-board watchdog timer.

A command/response protocol is used to transfer information between the MP840 and the system computer. Data is transferred through four registers: the ID register, status register, data register and reset register. An I/O port is used to pass a synchronization command.



Data Acquisition and Control Systems Division • 3631 E. 44th Street • Tucson, Arizona 85713 • Telephone: (602) 747-0711 • TWX: 910-952-1115 • Cable: BBRCORP

Memory Map

Base Address	b7	b6	b5	b4	b3	b2	b1	b0	Register
+0	1	1	0	0	0	S	S	S	ID
+1	X	M7	M6	M5	M4	M3	M2	M1	Status
+2	D	D	D	D	D	D	D	D	Data
+3	X	X	X	X	X	X	X	X	Reset

S = switch selectable
D = data
X = don't care
M1 = output buffer full
M2 = input buffer full
M3 = data reg. disabled
M4 = event memory empty
M5 = event memory full
M6 = interrupt enable
M7 = error

Command Summary

00	read-mask	30	sync-start	C0	interrupt enable [1]
03	set-mask	40	start-detect	D0	interrupt disable [1]
05	set-clock	50	stop-detect	E0	abort [1]
10	read-clock	60	read-input	F0	read-error
20	sync-enable	70	read-event		

NOTE: (1) Can be written at any time except when set-mask and set-clock are in progress.

Reply Summary

00	set-reply	60	end-of-data	A0	sync-error
03	mask-data	63	input-data	B0	no-error
15	clock-data	75	event-time	C0	start-error
20	sync-enable	78	event-data	D0	stop-error
30	sync-start	80	set-error	E0	abort
40	start-detect	90	reset	F0	empty
50	stop-detect				

Jumper Summary

W1-W24	Input range	W33, W34	Synchronize port add.
W25-W28	Debounce time	W35, W36, W41	Board ID
W29	Reset enable	W37, W38	Memory/IO map
W30-W31	Memory size	W39, W40	Memory inhibit
W32	Acknowledge enable	W42	Clock rate

Switch Options

SW1	Interrupt level
SW2-SW4, SW6	Base address
SW5	Synchronize port address

I/O CONNECTOR PINOUT

Pin[1]	P3[2]	P4[2]
49-50	Channel 1	Channel 13
46-45	Channel 2	Channel 14
42-41	Channel 3	Channel 15
38-37	Channel 4	Channel 16
34-33	Channel 5	Channel 17
30-29	Channel 6	Channel 18
26-25	Channel 7	Channel 19
22-21	Channel 8	Channel 20
18-17	Channel 9	Channel 21
14-13	Channel 10	Channel 22
10-9	Channel 11	Channel 23
6-5	Channel 12	Channel 24
1	NC	+sync
2	NC	−sync

NOTE: (1) All unlisted pins are not used.
(2) Channels 1-24 are not polarized.

ELECTRICAL SPECIFICATIONS

Typical at +25°C.

CHANNELS	24
RANGE	
DC Voltage:	
Range A	4VDC to 58VDC at 1mA to 15mA
Range B	60VDC to 140VDC at 1mA to 2.4mA
AC Voltage:	
Range A	8Vrms to 58Vrms at 1.5mA to 15mA
Range B	90Vrms to 140Vrms at 1.5mA to 2.4mA
Contact Closure	Wetting current must be provided externally
ISOLATION	
Input-to-bus	1200V peak
Channel-to-channel	300V peak
DEBOUNCE TIME	
Ranges	0, 2.5, 10, 20, and 40msec
Accuracy	±12.5%
Type	Hardware, selectable in groups of six channels
IMPUT IMPEDANCE	
Range A	4kΩ, nominal
Range B	60kΩ, nominal
SYNCHRONIZED INPUT	4VDC TO 15VDC at 5mA to 30mA, 200μs minimum duration
EVENT STORAGE	
Event times	1100
Total events	26,400 (24 events per event time)
RESOLUTION	1ms
Clock synchronization skew	500ns
REAL TIME CLOCK	Day, hour, minute, seconds and milliseconds
CPU	8085
MEMORY	
RAM	10k bytes
EPROM	4k bytes
TIME BASE	8.0MHz, 50ppm/°C stability
BUS	Multibus (IEEE-796) compatible
POWER	5VDC ±5% at 0.5A
ENVIRONMENT	
Operating temperature	0°C to +70°C
Storage temperature	−25°C to +85°C
Relative humidity	95% noncondensing

MECHANICAL SPECIFICATIONS

Compatible with Multibus (IEEE-796) specifications
Minimum board spacing .... 0.6" (15.2mm)
Board thickness .... 0.062" (1.57mm)
Bus connector .... 86 pin edge 0.156 contact spacing
I/O connector .... 50 pin edge 0.100 contact spacing
Mating connectors:
Burr-Brown 2250MC (Viking 3VH25/1JNS, solder tab).
3M Corp. 3415-0001 (Scotchflex, for flat cable).

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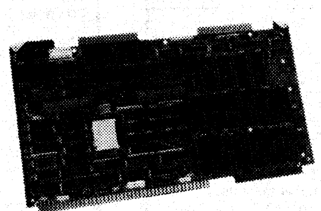

MP85188

SINGLE-BOARD COMPUTER

85188 SINGLE-BOARD COMPUTER
MULTIBUS™ (IEEE-796)-COMPATIBLE

FEATURES

- 80188 CPU
- 8MHz
- 16 JEDEC 28-PIN MEMORY SOCKETS
  UP TO 96k RAM
  UP TO 256k EPROM
  UP TO 64k EEPROM
- EEPROM SUPPORTED
- 1M BYTE ADDRESSABLE MEMORY
- DUAL SERIAL RS-232C PORTS
- 24 PARALLEL TTL I/O
- THREE COUNTERS (16 bit)
- TWO SBX SITES
- VECTORED INTERRUPTS
  10 inputs
  18 sources
- WATCHDOG TIMER
- USER-DEFINABLE FEATURES

DESCRIPTION

The MP85188 is a complete computer system on a single Multibus board with technological advances implemented to maximize computing power, memory expansion, and system performance. As a complete computer system the MP85188 includes an 80188 CPU, clock, memory (RAM, EPROM, EEPROM), serial I/O, parallel I/O, interrupt controller, timers, watchdog security timer, user-defined board status I/O, and SBX expansion. Advantages of the MP85188 include speed, flexible byte-wide JEDEC memory sites for EPROM, RAM, and EEPROM, EEPROM memory write support, popular 8088/8086 instruction set, watchdog timer for system integrity, low power consumption, and user-defined status I/O for board diagnostics and configuration.

The high speed of the Intel 80188 coupled with no-wait-state system design makes the MP85188 extremely valuable for real-time applications. Memory is designed to allow for EPROM-intensive applications that use RAM only for temporary data storage during operation. Critical set point data requiring permanent retention can be stored in EEPROM. The byte-oriented memroy configuration allows system memory to be expanded one chip at a time rather than two chips at a time as required in most 16-bit systems. Therefore only required memory need be installed and this reduces overall system cost. The Intel 80188 supports the popular 8086/8088 instruction set. Power consumption is much lower for the 80188 system approach than for equivalent 16-bit systems. The MP85188 supports multimaster capability allowing for the design of parallel processing systems. Twenty-four discrete I/O points can be controlled directly by the parallel port. Expansion can be achieved by the addition of SBX modules or other Burr-Brown Multibus industrial I/O boards.

Multibus™—Intel Corp.

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CENTRAL PROCESSING UNIT (CPU)

The Intel 80188 is a fast and versatile 16-bit microprocessor that gives the MP85188 the capability of handling the sophisticated requirements inherent to multitasking operating systems. This highly integrated microprocessor contains most system functions on one chip. These functions include clock generator, chip select, timers, interrupt controller, and dual 20-bit direct memory access (DMA). This single component approach greatly reduces component count, which enhances system reliability. The MP85188 is ideal for distributed control or data acquisition systems.

Completely compatible with iAPX86, iAPX188 and iAPX88 software, the 80188 is a high-performance microprocessor system. A powerful instruction set allows simplified programming, easy implementation of high-level languages, and efficient memory storage. Capabilities included are logical and arithmetic operations (addition, subtraction, multiplication, and division), bit, BCD, and ASCII character manipulation, string instructions, flexible addressing modes, loop instructions, enhanced control transfers, stack manipulation, and I/O handling.

MEMORY

Sixteen 28-pin, byte-oriented, JEDEC memory sites provide flexible memory configuration. Configuration is simplified through a mixture of dedicated and multipurpose sites. Four sites located in lower memory space are dedicated to RAM. Four sites located in upper memory space are dedicated to EPROM. The remaining eight sites are multipurpose and accommodate RAM, EPROM, or EEPROM. Four additional sites can be made available through an iSBC341 expansion module.

The MP85188 is provided with 8k bytes of static RAM. RAM capacity can be expanded to 96k (max) by using the eight multipurpose sockets or 128k (max) with the iSBC341 memory expansion module. The four dedicated EPROM sockets support up to 128k bytes of memory with 27256-type devices. A typical system could include 128k RAM and 128k EPROM. Other memory combinations are possible to meet special requirements. All memory is local to the CPU and is not accessible from the bus.

EEPROM SUPPORT

Electrically-erasable programmable read only memories (EEPROMs) can be installed in the multipurpose memory sites. A timer that can be set for either 1msec or 10msec is dedicated to timing the EEPROM write cycle. Completion of the write cycle can be monitored through polling or interrupt techniques. The MP85188 will support both 2k and 8k EEPROM devices.

SERIAL I/O

Serial I/O capability is provided by an 8274 dual multiprotocol serial controller. Dual RS-232C channels support both byte-asynchronous and bit- or byte-synchronous modes of operation. The asynchronous mode transmits 5-bit to 8-bit characters at baud rates of 300 to 19.2k and supports full duplex operation including complete modem control. The synchronous mode responds to either an internal or external synchronizing source. SDLC and HDLC flags may be generated and recognized. Data and device status are accessed via polling or interrupt operation.

PARALLEL I/O

The 24 TTL I/O channels are provided by an 8255 PIO chip. Signal lines are interfaced through sockets that allow either line drivers or resistor networks to buffer the signals. The I/O card edge connector interfaces to OPTO 22 I/O module panels.

COUNTER TIMERS

Three 16-bit counter timers on the 80188 chip provide timer functions for the MP85188. These timers are controlled by 16-bit registers internal to the 80188. One of the counters can be used to prescale the other two. Two of the timers provide the serial controller baud rate clocks.

INTERRUPT CAPABILITY

The 80188 CPU interrupt handling capabilities fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Five interrupt lines to the 80188, including one nonmaskable interrupt, are provided. The number of interrupt inputs can be expanded from 5 to 10 through an on-board 8259 slave interrupt controller. Two interrupts are dedicated to the serial controller. The remaining 8 interrupt inputs can be jumper-connected to a wide variety of sources including: eight lines from the Multibus, the EEPROM ready/busy write line, or two inputs from each of the SBX connectors.

WATCHDOG TIMER

A user-selectable hardware watchdog timer is available on the MP85188. This timer is cleared by a write operation to the status LEDs. When the 300msec timeout occurs, a hardware reset will reinitialize the MP85188.

USER-DEFINABLE FEATURES

Eight LEDs are mounted on the top edge of the MP85188. These may be used for status indication or diagnostics.

An eight-position DIP switch is provided to allow the user to set an application-specific status code on the board. These switches can be monitored by software to cause the program to branch to diagnostic routines or perform special application functions.

SBX SITES

The two SBX connectors accommodate two single-wide modules, or one single-and one double-wide module. DMA capability is supported by both sites.

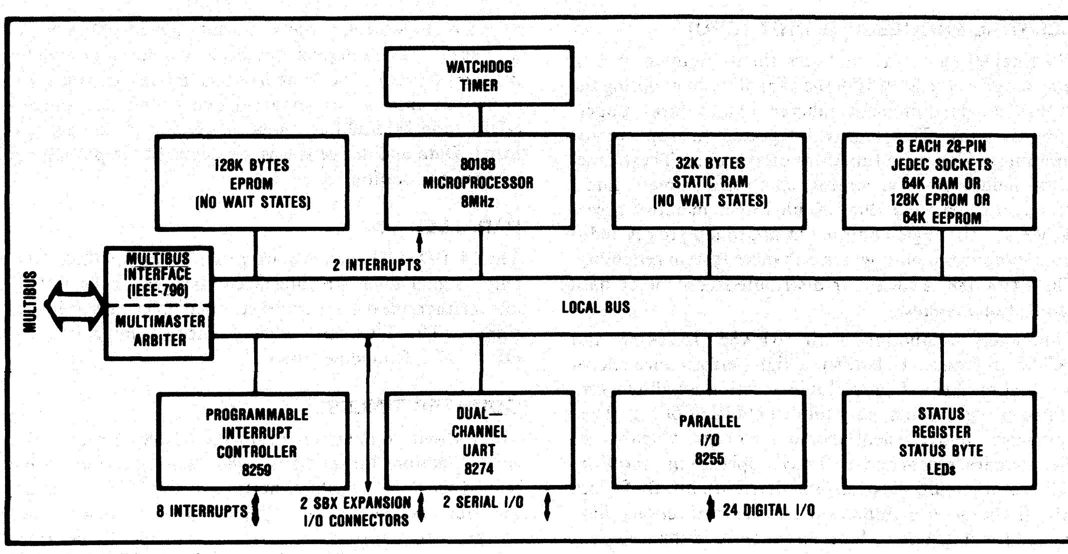


FIGURE 1. Block Diagram of MP85188.

MULTIBUS COMPATIBLE

The Multibus (IEEE-796) system bus is available for system expansion including address support to one megabyte and eight-bit data transfers. System functionality can be enhanced using Burr-Brown's wide selection of industrial I/O boards or other general-purpose peripheral boards. Both serial and parallel bus arbitration methods are supported. Arbitration synchronization signals are provided by the MP85188 and can be optionally disconnected. The 8259 interrupt controller allows the MP85188 to support all eight bus-vectored priority interrupts.

SPECIFICATIONS

CPU
80188 (8MHz)

CLOCK
7.37MHz

BUS
IEEE-796 (Multibus)

MEMORY
Sixteen 28-pin JEDEC sockets:
- 4 RAM (32k max), 8k supplied
- 4 EPROM (128k max)
- 8 multipurpose (64k RAM, 128k EPROM, or 64k EEPROM)
- iSBC341 memory expansion module (32k RAM or 32k EEPROM)

SERIAL I/O
Two RS-232C ports (8274 serial controller): asynchronous, synchronous

PARALLEL I/O
24 TTL I/O points (8255)

COUNTERS
Three 16-bit (internal to 80188)

INTERRUPT
10 inputs, 18 sources

SBX EXPANSION
Two connectors, IEEE-P959-compatible

WATCHDOG TIMER
300msec

USER-DEFINED FEATURES
Eight LEDs, user-defined; eight switch inputs

ENVIRONMENT
Operating temperature: 0°C to +50°C, 200 linear feet per minute air velocity
Storage temperature: −40°C to +85°C
Humidity: 90% noncondensing

POWER(1)
Voltage required:
±12V at 50mA
5V at 1.5A with 8k RAM or 2.0A with 32k RAM and 16k EPROM

NOTE: (1) Does not include expansion memory.

BURR-BROWN®

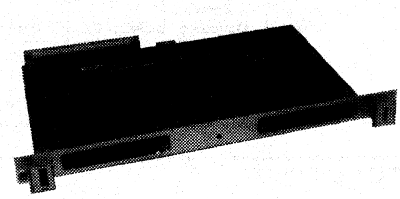
MPV902

Effective: 7/1/85
Supersedes: None

VMEbus RELAY OUTPUT BOARD

FEATURES

- **32 channels**
- **Latched outputs**
- **Power-up reset**
- **600VDC isolation, field-to-bus**
- **300VDC isolation, channel-to-channel**
- **Status LEDs**



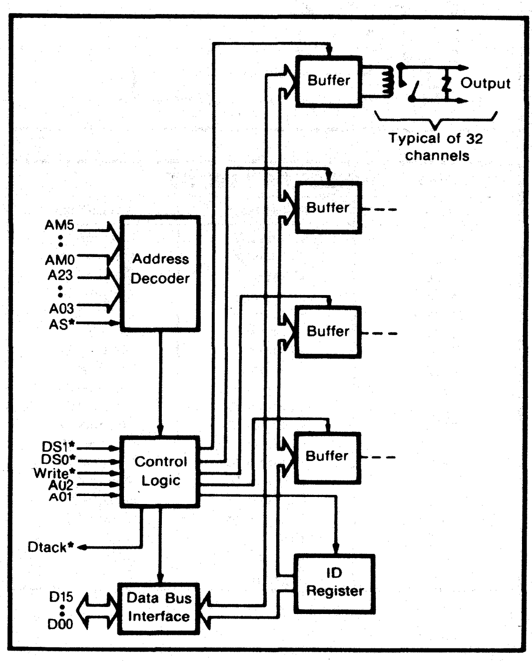
DESCRIPTION

The MPV902 is a 32-channel digital output board that is electrically and mechanically compatible with the VME-bus-based microcomputer systems.

Each of 32 channels is implemented by a protected reed relay and can handle up to 10W. Relays provide low "on-impedance", high output current and isolation between the computer and the field. Isolation assures that ground-loop problems are avoided. The computer is protected from component failures caused by voltage transients and malfunctions from outside sources. Each output contact set is protected by a transient suppressor.

Full hardware integration allows cards to be inserted directly into the system back panel. Power for the card is provided by the system bus. No external power supplies are required.

MPV902 appears as a memory location and data written on the data bus controls the status of each output. A logic "1" will close a contact. A logic "0" will open a contact. Any memory write operation may be used. The base address of the MPV902 is factory-set to FFF000 hexadecimal but may be changed to any value by setting the appropriate switches. The ID code is the lower byte of the base address and may be set to any 8-bit value.



Memory Map and Channel Position

Base Address	D15							D08	D07							D00	Data Bit
+0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0	Type/ID code
+2	ch 15	ch 14	ch 13	ch 12	ch 11	ch 10	ch 9	ch 8	ch 7	ch 6	ch 5	ch 4	ch 3	ch 2	ch 1	ch 0	P3
+4	ch 31	ch 30	ch 29	ch 28	ch 27	ch 26	ch 25	ch 24	ch 23	ch 22	ch 21	ch 20	ch 19	ch 18	ch 17	ch 16	P4
+6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	not used

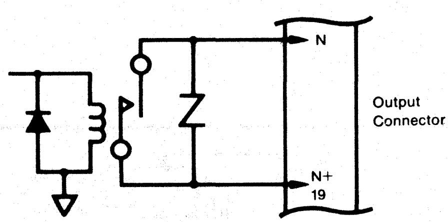
ADDRESSING MODES

The MPV902 can be operated in a variety of address modes. It will respond to either a 16-bit address or a 24-bit address. Additionally, address modifiers can be enabled to establish privilege levels as defined by the VME specifications.

Address/Address Modifier (AM) Response

Response Type	AM Codes	Address Decoding	Set to On	Set to Off
16-bit	N/A	A01-A15	SW3-1	SW3-2, -3
24-bit	N/A	A01-A23	None	SW3-1, -2, -3
Short	29, 2D	A01-A15	SW3-1, -2	SW3-3
Standard	39, 3D	A01-A23	SW3-3	SW3-1, -2

OUTPUT CIRCUIT



OUTPUT CONNECTOR PINOUT

Pins	P3 Function	P4 Function
1-20	Channel 1	Channel 17
2-21	Channel 2	Channel 18
3-22	Channel 3	Channel 19
4-23	Channel 4	Channel 20
5-24	Channel 5	Channel 21
6-25	Channel 6	Channel 22
7-26	Channel 7	Channel 23
8-27	Channel 8	Channel 24
9-28	Channel 9	Channel 25
10-29	Channel 10	Channel 26
11-30	Channel 11	Channel 27
12-31	Channel 12	Channel 28
13-32	Channel 13	Channel 29
14-33	Channel 14	Channel 30
15-34	Channel 15	Channel 31
16-35	Channel 16	Channel 32
17-36	+5V	+5V
18	N/C	N/C
19-37	Common	Common

ELECTRICAL SPECIFICATIONS

Typical at +25°C.

NUMBER OF CHANNELS	32
DIGITAL OUTPUT	
Watts DC (resistive load), max	10W
Amps (resistive load), max	0.5A
Voltage (resistive load), max	28VDC, rms
Life (resistive load), min	10^4 operations
Initial contact resistance, max	0.3Ω
Actuate Time	1msec
Deactuate Time	250μsec
Bounce Time	150μsec
TRANSIENT PROTECTION	
Continuous power rating	250mW
Discharge capacity	30 watt-seconds
Leakage current through transient suppressor at 28V	5mA
POWER REQUIREMENTS	
Voltage	5VDC, ±5%
Supply Drain, max.	0.3A
ISOLATION VOLTAGE	
Between microcomputer bus and output	600VDC
Between outputs	300VDC
OPERATING TEMPERATURE	0°C to +70°C
STORAGE TEMPERATURE	−55°C to +125°C

MECHANICAL SPECIFICATIONS

Compatible with VMEbus specifications

Minimum card spacing .... 0.8" (20.3mm)

Board thickness .... 0.062" (1.57mm)

Bus connector: P1 .... 96-pin DIN

P2 .... NA

I/O connectors, P3/P4 .... 37-pin D-subminiature

Accessories: Connectors for the digital inputs are standard 37-pin, male, D-subminiature types. Mating connectors such as AMP P/N 206650-1 or 3M P/N 3636-1000 may be used with mass-terminated ribbon cable or Canon P/N DCMA-37P may be used with solder connections.

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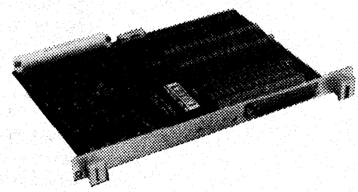
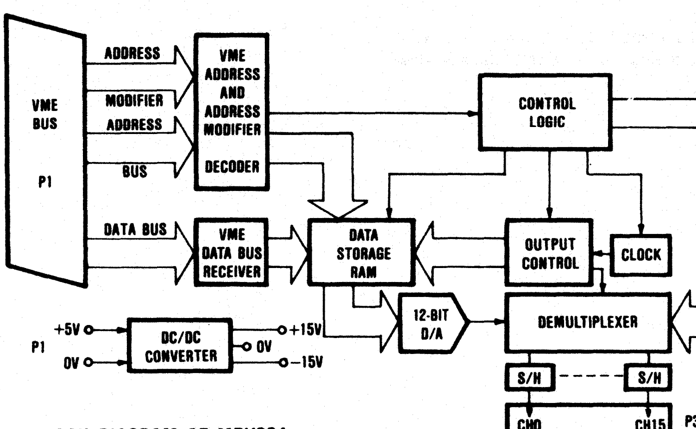
MPV904



VMEbus Analog Output Board

Features:
- 16 analog output channels
- Output voltage selectable between ±2.5V and ±10V
- 12-bit resolution

Applications:
- Factory automation and instrumentation
- Laboratory instrumentation
- Process control
- Machine control and monitoring
- Data logging systems



BLOCK DIAGRAM OF MPV904

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16 Channels of Analog Output on One Board

The high channel density of the MPV904 is made possible by using a dynamic refreshing technique on output sample/hold amplifiers.

Instead of the traditional method of providing one DAC (digital-to-analog converter) per output channel, only one DAC is used for all 16 channels, providing one of the lowest cost-per-output-channel boards on the market. The DAC output is sequentially switched between sample/hold amplifiers with each channel value stored digitally in RAM. The values held in this on-board RAM are easily changed from VMEbus.

Specifications

Typical at 25°C unless otherwise stated.

Number of Output Channels	16
Resolution	12 bits
Ranges (jumper selectable)	±10V, ±5V, ±2.5V, 0 to +5V, 0 to +10V
Total Error max	±0.075% FSR
Settling Time to 0.1% of FSR	2msec
Settling Time to 0.01% for 20V step	3.5msec max
Power Requirements	+5V ±5% at 1.5A max
Operating Temperature	0°C to +60°C
Storage Temperature	−25°C to +85°C
Relative Humidity	90% noncondensing

Note: FSR means Full Scale Range.

Ordering Information

MPV904	16-channel analog voltage output board
OM904	Operating Manual for MPV904 (as supplied with board)

TOP QUALITY VMEbus PRODUCTS FROM BURR-BROWN

In addition to the full Q.C. vetting of incoming components, the boards are subjected to a comprehensive temperature cycled burn-in (8 cycles between −20°C and +50°C).

Exhaustive tests before and after burn-in ensure that any problems are identified before the product leaves the factory.

SUPPORT DOCUMENTATION

Each VMEbus board is fully supported with a comprehensive operating manual. In addition to detailed set-up and operating instructions, the manual includes schematics and assembly language software written for the 68000 processor.

THE SYSTEMS APPROACH

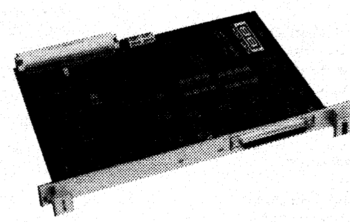
This board is one of a family of VMEbus boards in which a systems approach has been taken in the design of the bus interface. This ensures software compatibility between the boards as well as giving the system designer a wide range of VMEbus features.

- Configuration A24, D16, DTB slave
- Address block selectable within 16M bytes memory space
- Short addressing available if required (64K bytes)
- Multiple address modifier capability
- 150nsec response to CPU interrogation

Contact Burr-Brown for details of the full range of analog I/O and DSP boards on the VMEbus.

BURR-BROWN®

MPV905

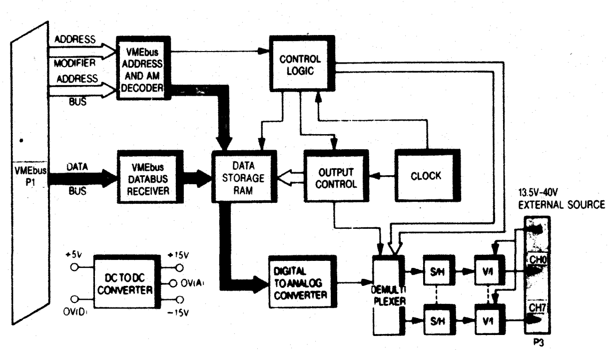


VMEbus Analog Output Board

Features
- 8 current source analog output channels
- 3 selectable output current ranges
- 12-bit resolution
- Address block selectable in whole 16 Mbyte memory space
- Fully VMEbus compatible

Applications
- Factory automation and instrumentation
- Laboratory instrumentation
- Process control
- Machine control and monitoring

MPV905 Block Diagram



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MPV905—8 Channels of Current Output

The MPV905 is an 8-channel analog output board (current source) with 12-bit resolution and full VMEbus capability.
The board features three standard output current ranges enabling a flexible solution to noise-free industrial applications.
High channel density is achieved by using dynamic analog outputs. This approach utilises a single digital to analog converter to drive all 8 outputs. Digital data for each channel is stored in an on-board RAM and the corresponding analog output is stored in separate sample and hold circuits. A voltage to current converter on each channel then provides the current output from the board.
The host CPU changes data in RAM by a write operation to the appropriate channel. Glitch-free operation is ensured as the refresh circuitry is disabled while new data is being written into the RAM.
The current source outputs are powered from a user supply in the range +13.5V to +40V through the P3 connector.

TOP QUALITY VMEbus PRODUCTS FROM BURR-BROWN

In addition to the full Q.C. vetting of incoming components, the boards are subjected to a comprehensive temperature cycled burn-in (8 cycles between −20°C and +50°C).

Exhaustive tests before and after burn-in ensure that any problems are identified before the product leaves the factory.

SUPPORT DOCUMENTATION

Each VMEbus board is fully supported with a comprehensive operating manual. In addition to detailed set-up and operating instructions, the manual includes schematics and assembly language software written for the 68000 processor.

THE SYSTEMS APPROACH

This board is one of a family of VMEbus boards in which a systems approach has been taken in the design of the bus interface. This ensures software compatibility between the boards as well as giving the system designer a wide range of VMEbus features.

- Configuration A24, D16, DTB slave
- Address block selectable within 16M byte memory space
- Short addressing available if required (64K bytes)
- Multiple address modifier capability

Contact Burr-Brown for the full range of Analog I/O and DSP boards on the VMEbus

Specification Typical at 25°C

Number of output channels	8
Resolution	12 bits
Output ranges (jumper selectable)	0-20mA 4-20mA 5-25mA
Total Error (max)	±0.05% FSR
Settling time to 0.1% of FSR	2msec
Settling time to 0.01% for 20mA step	3.5msec max
Power from VMEbus	+5V ±5% at 1.5A max
Power from user supply (V_{CC})	13.5V to 40V at 250mA max
Operating temperature	0°C to 60°C
Storage temperature	−25°C to 85°C
Relative humidity	5% to 90% non-condensing

Note: FSR means Full Scale Range.

Ordering Information
MPV905 – 8-Channel Analog Current Output Board
OM905 – Operating Manual for MPV905 (as supplied with board)

BURR-BROWN®

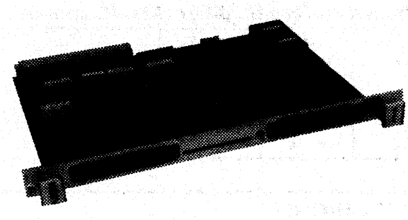
MPV910

Effective: 7/1/85
Supersedes: None

VMEbus ISOLATED DIGITAL INPUT BOARD

FEATURES

- 32 channels
- Contact closure
- Contact wetting current
- Voltage inputs
- TTL-compatible inputs
- 600VDC isolation field-to-computer
  300VDC isolation channel-to-channel
- Debounce
- Status LEDs
- Board type and ID codes



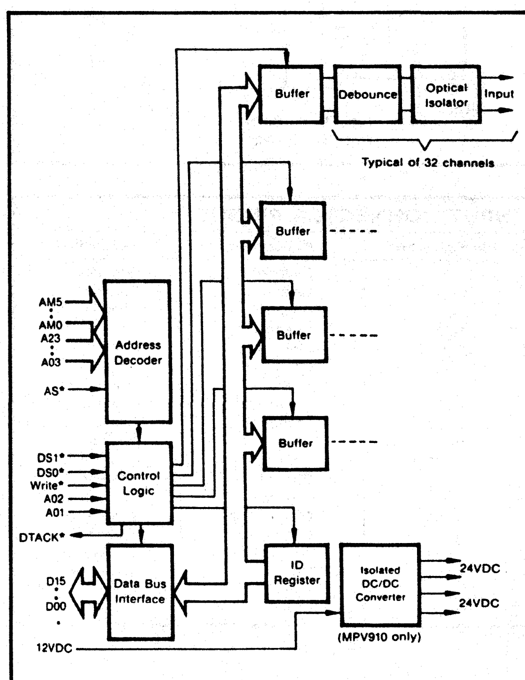
DESCRIPTION

The MPV910 is a 32-channel optically isolated discrete input board that is electrically and mechanically compatible with VMEbus-based microcomputer systems. Input signal types include dry contact closures, wetted contact closures, and DC voltages.

Input isolation protects the computer from input voltage transients and malfunctions of field inputs. Channel-to-channel isolation minimizes channel interaction and avoids ground-loop problems. Contact debounce, which prevents erroneous data caused by relay contact bounce, is provided on all models.

There are three versions of the MPV910. The MPV910 includes a contact wetting source to provide sense current for dry contacts. The MPV910-LV has reduced input impedance to allow TTL level inputs. The MPV910-NS has had the contact wetting source removed.

The MPV910 appears as a memory location. Data is acquired through any memory read operation. Each input is one bit of a byte. An open contact (low voltage) is represented by a logic "0". A closed contact (high voltage) is represented by a logic "1". The base address of the MPV910 is factory-set to FFF000 hexadecimal but may be changed to any value by setting the appropriate switches. The ID code is the lower byte of the base address and may be set to any 8-bit value.



Memory Map and Channel Position

Base Address	D15							D08	D07							D00	Data Bit
+0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0	Type/ID code
+2	ch 15	ch 14	ch 13	ch 12	ch 11	ch 10	ch 9	ch 8	ch 7	ch 6	ch 5	ch 4	ch 3	ch 2	ch 1	ch 0	P3
+4	ch 31	ch 30	ch 29	ch 28	ch 27	ch 26	ch 25	ch 24	ch 23	ch 22	ch 21	ch 20	ch 19	ch 18	ch 17	ch 16	P4
+6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	not used

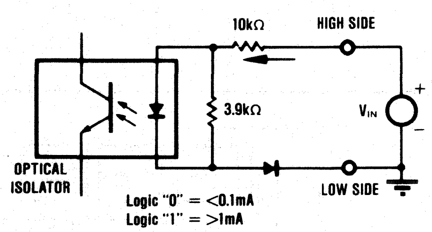
ADDRESSING MODES

The MPV910 can be operated in a variety of address modes. It will respond to either a 16-bit address or a 24-bit address. Additionally, address modifiers can be enabled to establish privilege levels as defined by the VME specifications.

Address/Address Modifier (AM) Response

Response Type	AM Codes	Address Decoding	Set to On	Set to Off
16-bit	N/A	A01-A15	SW3-1	SW3-2, -3
24-bit	N/A	A01-A23	none	SW3-1, -2, -3
Short	29, 2D	A01-A15	SW3-1, -2	SW3-3
Standard	39, 3D	A01-A23	SW3-3	SW3-1, -2

INPUT CIRCUIT



INPUT CONNECTOR PINOUT

Pin High-Low	P3 Function	P4 Function
1-20	Channel 1	Channel 17
2-21	Channel 2	Channel 18
3-22	Channel 3	Channel 19
4-23	Channel 4	Channel 20
5-24	Channel 5	Channel 21
6-25	Channel 6	Channel 22
7-26	Channel 7	Channel 23
8-27	Channel 8	Channel 24
9-28	Channel 9	Channel 25
10-29	Channel 10	Channel 26
11-30	Channel 11	Channel 27
12-31	Channel 12	Channel 28
13-32	Channel 13	Channel 29
14-33	Channel 14	Channel 30
15-34	Channel 15	Channel 31
16-35	Channel 16	Channel 32
17-36	+V	+V
18	N/C	N/C
19-37	−V	−V

ELECTRICAL SPECIFICATIONS

Typical at +25°C.

INPUT CHARACTERISTICS	
Number of Inputs	32
Input Resistor: MPV910	10kΩ, 1/2W
MPV910NS	10kΩ, 1/2W
MPV910LV	1kΩ, 1/2W
Delay Times: Open-to-Closed	10msec
Closed-to-Open	10msec
VOLTAGE SENSE	
Logic 0: MPV910	Open
MPV910NS	4VDC, max
MPV910LV	2VDC, max
Logic 1: MPV910	Closed
MPV910NS	17VDC, min
MPV910LV	3.5VDC, min
MAXIMUM VOLTAGE (V_S) ACROSS INPUT WITHOUT DAMAGE	60VDC, max 120VAC, max
VOLTAGE SOURCE (contact wetting)(1)	
MPV910	24VDC
MPV910NS	None
MPV910LV	None
ISOLATION VOLTAGE	
System-to-Field	600VDC
Channel-to-Channel	300VDC
Input Blocks(2)	300VDC
POWER REQUIREMENTS	
MPV910	+5VDC/500mA; +12VDC, 250mA
MPV910NS	+5VDC/500mA
MPV910LV	+5VDC/500mA
ENVIRONMENT	
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +125°C
Relative Humidity	95% noncondensing

NOTES: (1) Common power supplies used for contact wetting degrade channel-to-channel isolation. (2) The on-board DC-to-DC converter provides two isolated voltages. Each voltage services one block of sixteen input channels.

MECHANICAL SPECIFICATIONS

Compatible with VMEbus specifications
Minimum card spacing .... 0.8" (20.3mm)
Board thickness .... 0.062" (1.57mm)
Bus connector: P1 .... 96-pin DIN
P2 .... NA
I/O connectors, P3/P4 .... 37-pin D-subminiature

Accessories: Connectors for the digital inputs are standard 37-pin, male, D-subminiature types. Mating connectors such as AMP P/N 206655-1 or 3M P/N 3837-1000 may be used with mass-terminated ribbon cable or Canon P/N DCMA-37S may be used with solder connections.

BURR-BROWN®

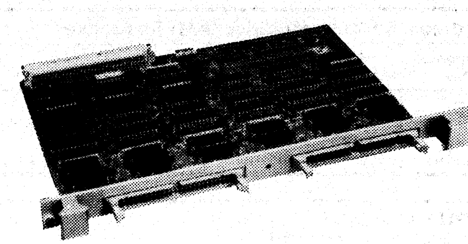
MPV930-48

Effective: 7/1/85
Supersedes: None

VMEbus TTL INPUT/OUTPUT BOARD

FEATURES

- **48 channels**
- **Socketed I/O terminations**
- **Latched outputs**
- **Output read back**
- **No power-up glitch**
- **Status LED**
- **Board type and ID codes**



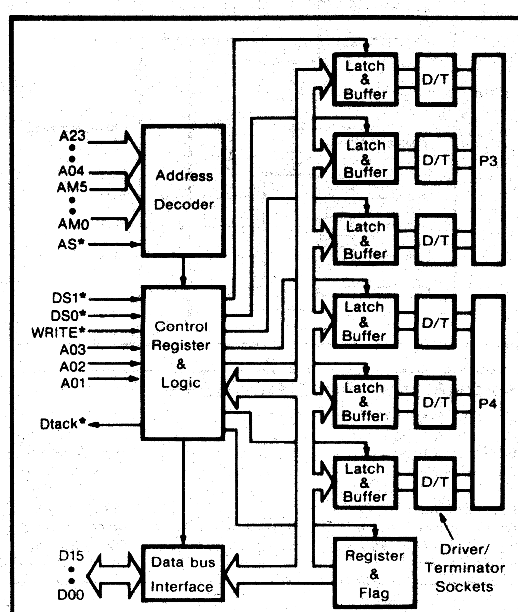
DESCRIPTION

The MPV930-48 is 48-channel TTL I/O board that is electrically and mechanically compatible with VMEbus-based microcomputer systems. I/O channels are organized as six 8-bit ports. Each port may be configured as an input or output by installing the appropriate driver or termination network in the socket provided.

Data from the output ports can be read by the system CPU. Outputs are enabled under software control. At power-up the outputs can be set to a desired value prior to enabling them.

Full hardware integration allows cards to be inserted directly into the system back panel. Power for the card is provided by the system bus. No external power supplies are required.

The MPV930-48 appears as a memory location and is both byte- and word-accessible. Data is transferred through read and write operations. The base address of the MPV930-48 is factory-set to FFF000 hexidecimal but may be changed to any value by setting the appropriate switches. The ID code is the lower byte of the base address and may be set to any 8-bit value.



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Memory Map and Channel Position																	
Base Address	**D15**							**D08**	**D07**							**D00**	**Data Bit**
+0	0	0	0	0	0	0	1	0	Y	Y	Y	Y	Y	Y	Y	Y	BD IC code
+2	X	X	X	X	X	X	X	X	X	X	P6	P5	P4	P3	P2	P1	O/P CTRL
+4 P2	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	P1
+6 P4	C32	C31	C30	C29	C28	C27	C26	C25	C24	C23	C22	C21	C20	C19	C18	C17	P3
+8 P6	C48	C47	C46	C45	C44	C43	C42	C41	C40	C39	C38	C37	C36	C35	C34	C33	P5
+10	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Not Used
+12	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Not Used
+14	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Not Used

CXX = Channel data PX = logic "1" enables output

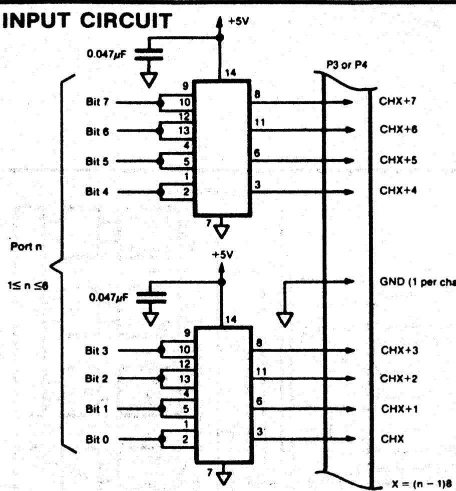
ADDRESSING MODES

The MPV930 can be operated in a variety of address modes. It will respond to either a 16-bit address or a 24-bit address. Additionally, address modifiers can be enabled to establish privilege levels as defined by the VME specifications.

Address/Address Modifier (AM) Response

Response Type	AM Codes	Address Decoding	Set to On	Set to Off
16-bit	N/A	A01-A15	SW3-1	SW3-2, -3
14-bit	N/A	A01-A23	None	SW3-1, -2, -3
Short	29, 2D	A01-A15	SW3-1, -2	SW3-3
Standard	39, 3D	A01-A23	SW3-3	SW3-1, -2

INPUT CIRCUIT



MECHANICAL SPECIFICATIONS

Compatible with VMEbus specifications
Minimum card spacing .... 0.8" (20.3mm)
Board thickness .... 0.062" (1.57mm)
Bus connector: P1 .... 96-pin DIN
P2 .... NA
I/O connectors, P3/P4 .... 50-pin header
Connectors for the I/O ports are standard 50-pin headers. Mating connectors such as Ansley type 609-5030, Berg type 66900-350, 3M type 3425-6000.

ELECTRICAL SPECIFICATIONS

Typical at +25°C.

INPUT CHARACTERS	
Number of Inputs	48[1]
Input Levels	
Logic 0	0.8VDC
Logic 1	2.0VDC
Input Load	One TTL load plus load of terminators installed.
Maximum Input Voltage	5.5VDC
OUTPUT CHARACTERISTICS	
Number of Outputs	48[1]
Output Levels	Depends on installed driver.[2]
POWER REQUIREMENTS	+5VDC at 600mA
ENVIRONMENT	
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +125°C
Relative Humidity	95% noncondensing

NOTES: (1) Board has 48 channels. All channels may be changed by software from input to output in groups of eight. (2) Board-mounted sockets will accommodate standard S, LS, and ALS versions of 7400, 7403, 7408, 7409, 7426, 7432, 7437, 7438 or 74132 as output drivers.

I/O CONNECTOR PINOUT

Pin No.*	P3 Function		P4 Function	
	Port	Channel	Port	Channel
50	1	1	4	25
48	1	2	4	26
46	1	3	4	27
44	1	4	4	28
42	1	5	4	29
40	1	6	4	30
38	1	7	4	31
36	1	8	4	32
34	2	9	5	33
32	2	10	5	34
30	2	11	5	35
28	2	12	5	36
26	2	13	5	37
24	2	14	5	38
22	2	15	5	39
20	2	16	5	40
18	3	17	6	41
16	3	18	6	42
14	3	19	6	43
12	3	20	6	44
10	3	21	6	45
8	3	22	6	46
6	3	23	6	47
4	3	24	6	48

*All odd pins are grounded.

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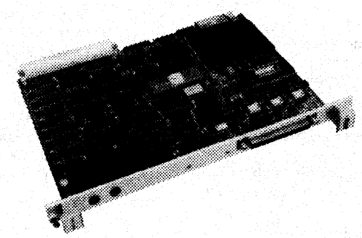


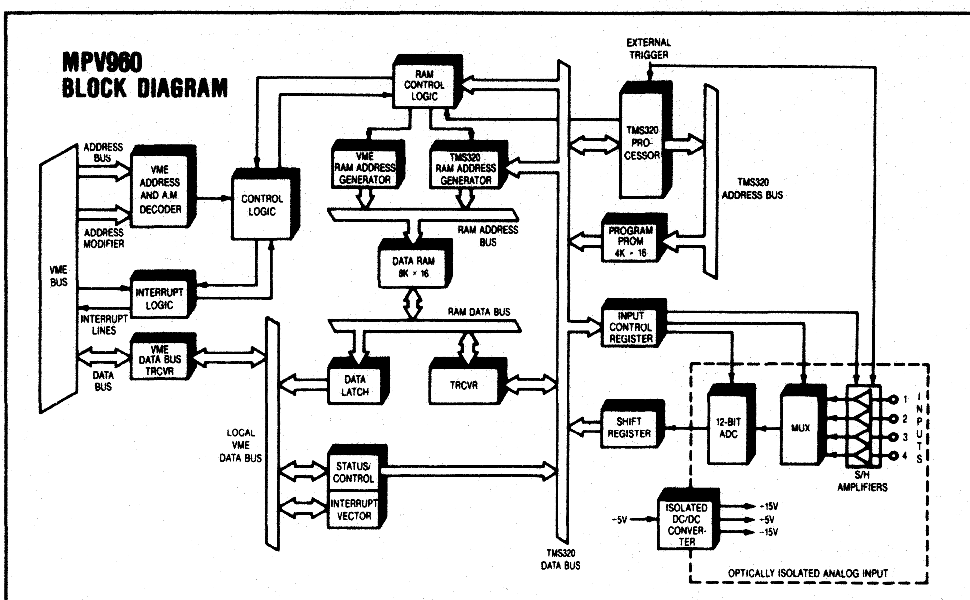
MPV960

VMEbus Analog Input and DSP Board

Features
- 4 analog input channels with simultaneous sampling
- On board TMS320 Digital Signal Processor
- Dual-port swinging-buffer RAM
- Transient capture and continuous input modes
- 12-bit resolution
- Optical isolation between analog and digital circuits

Applications
- Real-time digital filtering
- Speech processing
- Signal pre-processing
- Vibration analysis
- Correlation

VMEdsp™



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MPV960—For real-time digital signal processing

The MPV960 is a 4-channel high-speed analog input board incorporating on-board signal processing and is fully compatible with the VMEbus. Analog inputs are optically isolated from the digital section of the board and can be sampled simultaneously on 2 or 4 channels. The board incorporates the Texas Instruments TMS320 signal processing chip which has a 200nsec instruction cycle and a specialized arithmetic section for high-speed signal processing applications.

Analog data is captured at sampling rates defined by the MPV960 or an external trigger source. Data can be processed in real time by the TMS320 and stored in data RAM for access by the host CPU via the VMEbus. In this way analog signals can be continuously sampled at fixed rates independent of asynchronous events in the host system such as dynamic RAM refreshing and servicing of other tasks.

Software Support: The MPV960 is supplied with PROMs containing programs for data acquisition averaging and spike removal. Software packages for digital filtering and other functions will be produced. Customized software can also be developed by the user.

Availability of software packages on request.

TOP QUALITY VMEbus PRODUCTS FROM BURR-BROWN

In addition to the full QC inspection of incoming components, the boards are subjected to a comprehensive temperature-cycled burn-in (8 cycles between −20°C and +50°C.)

Exhaustive tests before and after burn-in ensure that problems are eliminated before the product leaves the factory.

SUPPORT DOCUMENTATION

Each VMEbus board is fully supported with a comprehensive operating manual. In addition to detailed set-up and operating instructions, the manual includes schematics and assembly language software written for the 68000 processor.

THE SYSTEMS APPROACH

This board is one of a family of VMEbus boards in which a systems approach has been taken in the design of the bus interface. This ensures software compatibility between the boards, as well as giving the system designer a wide range of VMEbus features.

- Configuration A24, D16, DTB slave
- Address block selectable within 16M byte memory space
- Short addressing available if required (64k bytes)
- Multiple address modifier capability
- Seven vectored interrupt levels

Specification (Typical at 25°C)

Analog Input Section		
Input channels		4, with simultaneous sampling
Input ranges		0 to 5V, 0 to 10V, ±2.5V, ±5V, ±10V
Sampling rates, max:	1 channel	86kHz per channel
	2 channels	44kHz per channel
	4 channels	22kHz per channel
Resolution		12 bits
System accuracy		0.05%
Digital Section		
Processor		TMS320 with 200nsec instruction cycle
Data storage memory		16k bytes (8k × 16)
Program memory		8k bytes (4k × 16)
Triggering modes		internal/external/event
Power requirement		3.5A at +5V
Environmental Characteristics		
Operating temperature		0°C to +60°C
Relative humidity		5% to 90% noncondensing

ORDERING INFORMATION

MPV960 —4-channel analog-input DSP board
OM960 —Operating Manual for MPV960 (as supplied with board)

Contact Burr-Brown for details of the full range of analog I/O and DSP boards on the VMEbus.

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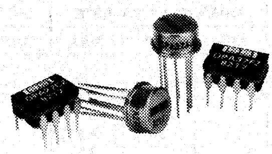


OPA27
OPA37

Ultra-Low Noise Precision OPERATIONAL AMPLIFIERS

FEATURES

- LOW NOISE: 100% tested, 3.8nV/$\sqrt{Hz}$ max at 1kHz
- LOW OFFSET: 25μV max
- LOW DRIFT: 0.6μV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 114dB min
- HIGH POWER SUPPLY REJECTION: 100dB min
- FITS OP-07, OP-05, AD510, AD517 SOCKETS

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- TRANSDUCER AMPLIFIER
- RADIATION HARD EQUIPMENT

DESCRIPTION

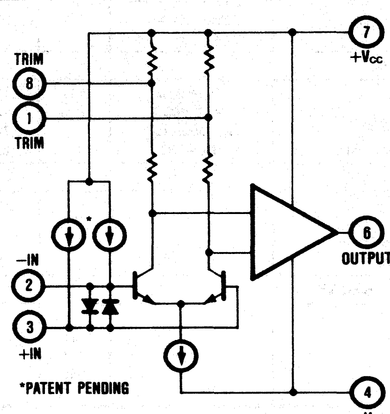
The OPA27/37 is an ultra-low noise, high precision monolithic operational amplifier.

Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.

A unique bias current cancellation circuit (patent pending) allows bias and offset current specifications to be met over the full −55°C to +125°C temperature range.

The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain ≥ 5.

The Burr-Brown OPA27/37 is an improved replacement for the industry-standard OP-27/OP-37.



OPA27/37 SIMPLIFIED CIRCUIT

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SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

		OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT											
NOISE											
Voltage, f_o = 10Hz	100% tested, (A, E)		3.1	5.5		3.5	5.5		3.8	8.0	$nV/\sqrt{Hz}$
f_o = 30Hz	100% tested, (A, E)		2.9	4.5		3.1	4.5		3.3	5.6	$nV/\sqrt{Hz}$
f_o = 1kHz	100% tested, (A, E)		2.7	3.8		3.0	3.8		3.2	4.5	$nV/\sqrt{Hz}$
f_B = 0.1Hz to 10Hz			0.07	0.18		0.08	0.18		0.09	0.25	μV, p-p
Current,[1] f_o = 10Hz	100% tested, (A, E)		1.7	4.0		1.7	4.0		1.7		$pA/\sqrt{Hz}$
f_o = 30Hz	100% tested, (A, E)		1.0	2.3		1.0	2.3		1.0		$pA/\sqrt{Hz}$
f_o = 1kHz	100% tested, (A, E)		0.4	0.6		0.4	0.6		0.4	0.6	$pA/\sqrt{Hz}$
OFFSET VOLTAGE[2]											
Input Offset Voltage			±6	±25		±12	±60		±25	±100	μV
Average Drift[3]	$T_{A\,MIN}$ to $T_{A\,MAX}$		±0.2	±0.6		±0.3	±1.3		±0.4	±1.8	μV/°C
Long Term Stability[4]			0.2	1		0.3	1.5		0.4	2.0	μV/mo
Supply Rejection	±V_{CC} = 4 to 18V	100	134		100	125		94	120		dB
	±V_{CC} = 4 to 18V		±0.2	±10		±0.6	±10		±1	±20	μV/V
BIAS CURRENT											
Input Bias Current			±11	±40		±13	±55		±15	±80	nA
OFFSET CURRENT											
Input Offset Current			6	35		8	50		10	75	nA
IMPEDANCE											
Common-Mode			3			2.5			2		GΩ
VOLTAGE RANGE											
Common-Mode Input Range		±11	±12.3		±11	±12.3		±11	±12.3		V
Common-Mode Rejection	V_{IN} = ±11VDC	114	128		106	125		100	122		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	120	126		120	125		117	124		dB
	R_L ≥ 1kΩ	118	125		118	125			124		dB
FREQUENCY RESPONSE											
Gain-Bandwidth Product	OPA27	5	8		5	8		5	8		MHz
	OPA37	45	63		45	63		45	63		MHz
Slew Rate	V_o = ±10V, R_L = 2kΩ										
	OPA27, G = +1	1.7	1.9		1.7	1.9		1.7	1.9		V/μsec
	OPA37, G = +5	11	11.9		11	11.9		11	11.9		V/μsec
Settling Time, 0.01%	OPA27, G = +1		25			25			25		μsec
	OPA37, G = +5		25			25			25		μsec
RATED OUTPUT											
Voltage Output	R_L ≥ 2kΩ	±12	±13.8		±12	±13.8		±12	±13.8		V
	R_L ≥ 600Ω	±10	±12.8		±10	±12.8		±10	±12.8		V
Output Resistance	DC, open loop		70			70			70		Ω
Short Circuit Current	R_L = 0Ω		25	60		25	60		25	60	mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±4		±22	±4		±22	±4		±22	VDC
Current, Quiescent	I_o = 0mADC		3	4.7		3	4.7		3.3	5.7	mA
TEMPERATURE RANGE											
Specification											
A, B, C		−55		+125	−55		+125	−55		+125	°C
E, F, G		−25		+85	−25		+85	−25		+85	°C
Operating		−55		+125	−55		+125	−55		+125	°C
Storage		−65		+150	−65		+150	−65		+150	°C

NOTES: (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only. (2) Offset voltage specifications on grades A and E are guaranteed with units fully warmed up. Grades B, C, F, and G are measured with automatic test equipment after approximately 0.5 second from power turn-on. (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range											
A, B, C		−55		+125	−55		+125	−55		+125	°C
E, F, G		−25		+85	−25		+85	−25		+85	°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage											
A, B, C			±24	±60		±45	±200		±60	±300	μV
E, F, G			±17	±50		±33	±140		±48	±220	μV
Average Drift[2]	$T_{A\,MIN}$ to $T_{A\,MAX}$		±0.2	±0.6		±0.3	±1.3		±0.4	±1.8	μV/°C
Supply Rejection											
A, B, C	±V_{CC} = 4.5 to 18V	96	130		94	127		86	122		dB
E, F, G	±V_{CC} = 4.5 to 18V	97	130		96	127		90	122		dB
BIAS CURRENT											
Input Bias Current											
A, B, C			±16	±60		±22	±95		±29	±150	nA
E, F, G			±13	±60		±16	±95		±21	±150	nA
OFFSET CURRENT											
Input Offset Current											
A, B, C			23	50		25	85		35	135	nA
E, F, G			12	50		14	85		20	135	nA
VOLTAGE RANGE											
Common-Mode Input Range											
A, B, C		±10.3	±11.5		±10.3	±11.5		±10.3	±11.5		V
E, F, G		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8		V
Common-Mode Rejection	V_{IN} = ±11VDC										
A, B, C		108	124		100	122		94	120		dB
E, F, G		110	126		102	124		96	122		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$										
A, B, C		116	121		114	120		110	118		dB
E, F, G		118	123		117	122		113	120		dB
RATED OUTPUT											
Voltage Output	$R_L = 2k\Omega$										
A, B, C		±11.5	±13.7		±11.0	±13.5		±10.5	±13.3		V
E, F, G		±11.7	±13.8		±11.4	±13.6		±11.0	±13.4		V
Short Circuit Current	V_o = 0VDC		25			25			25		mA

NOTES: (1) Offset voltage specifications on grades A and E are guaranteed with the units fully warmed up. Grades B, C, F, and G are measured with automatic equipment after approximately 0.5 second. (2) Unnulled or nulled with 8kΩ to 20kΩ potentiometer.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
Internal Power Dissipation(1) 500mW
Input Voltage(2) .... ±22V
Output Short Circuit Duration(3) .... Indefinite
Differential Input Voltage(4) .... ±0.7V
Differential Input Current(4) .... ±25mA
Storage Temperature Range .... −65°C to +150°C
Operating Temperature Range
- A, B, C .... −55°C to +125°C
- E, F, G .... −55°C to +125°C

Lead Temperature Range
- (Soldering, 60sec) .... +300°C

NOTES:

1. Maximum package power dissipation vs ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 J	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. For supply voltages less than ±22V the absolute maximum input voltage is equal to the supply voltage.
3. To common with ±V_{CC} = 15V.
4. The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

ORDERING INFORMATION

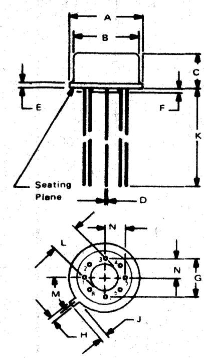
OPAXX Y Z

Basic Model Number — OPAXX
Performance Grade Code — Y
  A, B, C: −55°C to +125°C
  E, F, G: −25°C to +85°C
Package Code — Z
  J = TO-99
  Z = 8-Pin Hermetic DIP

TO-99		8-PIN HERMETIC DIP	
OPA27AJ	OPA27EJ	OPA27AZ	OPA27EZ
OPA27BJ	OPA27FJ	OPA27BZ	OPA27FZ
OPA27CJ	OPA27GJ	OPA27CZ	OPA27GZ
OPA37AJ	OPA37EJ	OPA37AZ	OPA37EZ
OPA37BJ	OPA37FJ	OPA37BZ	OPA37FZ
OPA37CJ	OPA37GJ	OPA37CZ	OPA37GZ

MECHANICAL

"J" PACKAGE, TO-99



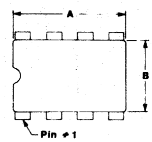
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	-	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE:
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

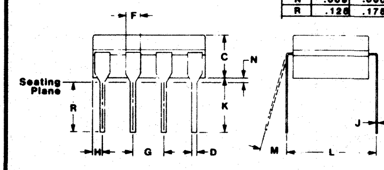
Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD—883 (except paragraph 3.2).

"Z" PACKAGE, 8-PIN HERMETIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.375	.405	9.53	10.28
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	–	.098	–	2.49
J	.008	.012	0.20	0.30
K	.150	–	3.80	–
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45



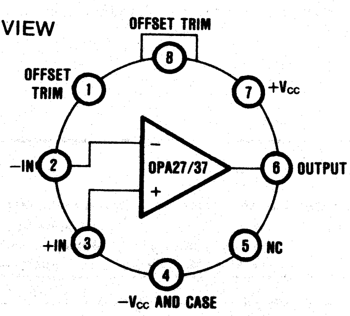
NOTE:
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

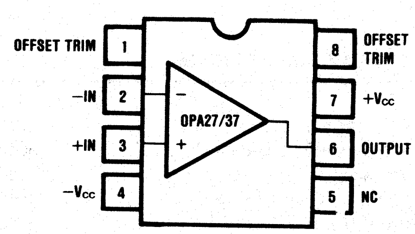
Pin material and plating composition conform to method 2003 (solderability) of MIL-STD—883 (except paragraph 3.2).

CONNECTION DIAGRAMS

TOP VIEW



TOP VIEW



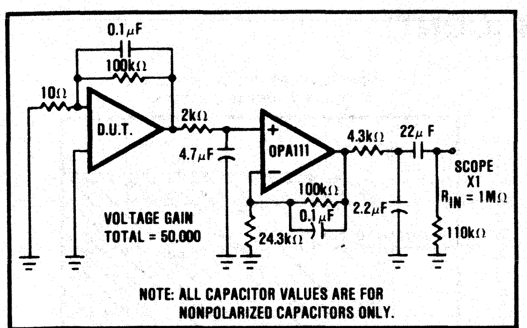


FIGURE 1. 0.1Hz to 10Hz Noise Test Circuit.

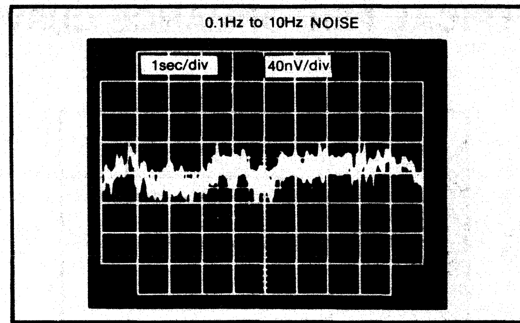
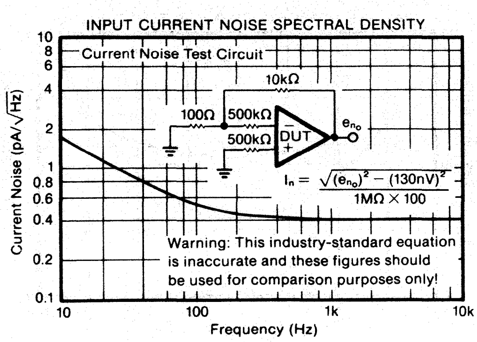
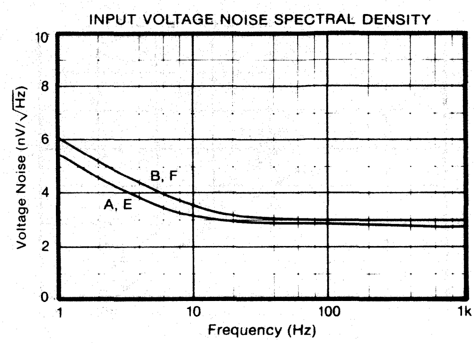


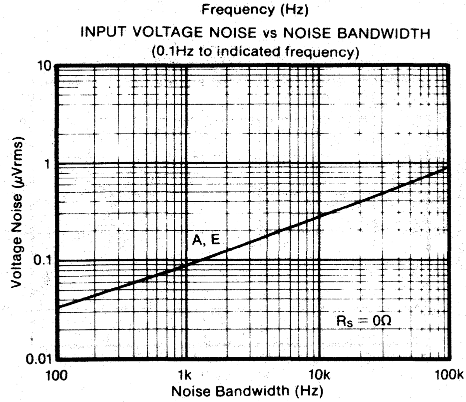
FIGURE 2. Low Frequency Noise.

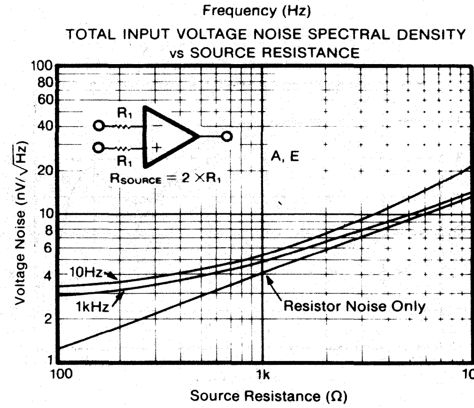
TYPICAL PERFORMANCE CURVES

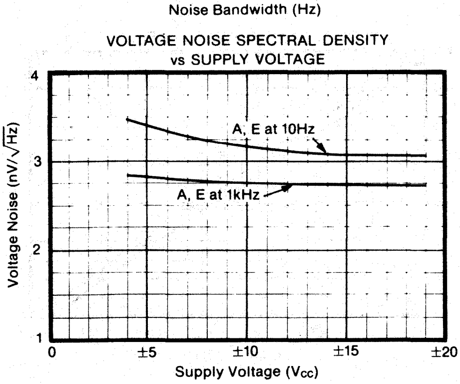
T_A = +25°C, $\pm V_{CC}$ = ±15VDC unless otherwise noted.

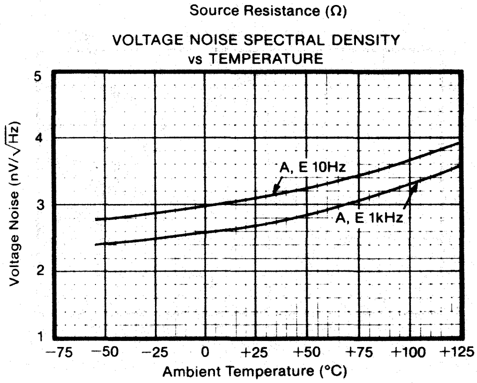








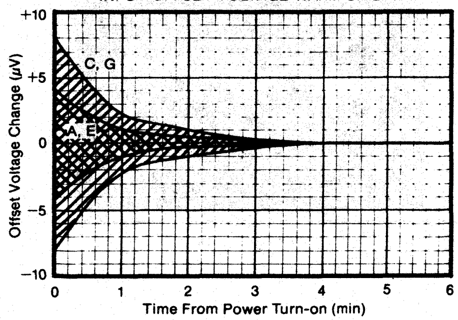




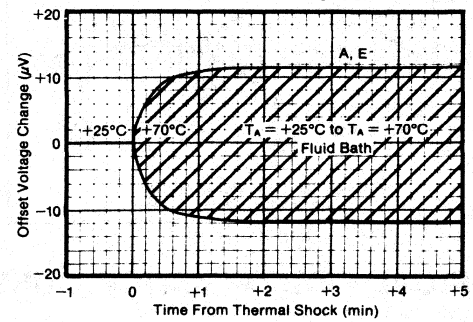
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $\pm V_{CC} = \pm15VDC$ unless otherwise noted.

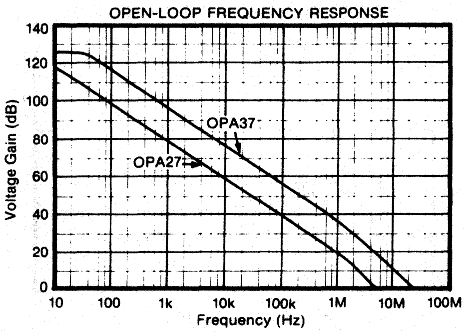
INPUT OFFSET VOLTAGE WARM-UP DRIFT



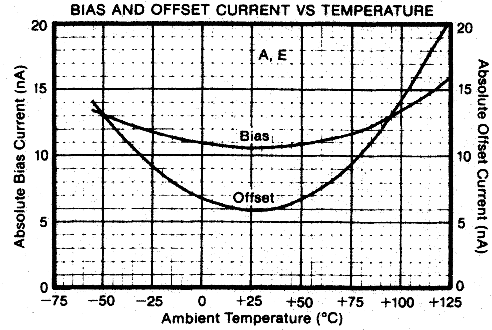
INPUT OFFSET VOLTAGE CHANGE
DUE TO THERMAL SHOCK



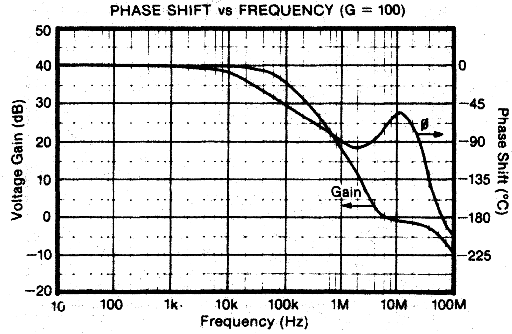
OPEN-LOOP FREQUENCY RESPONSE



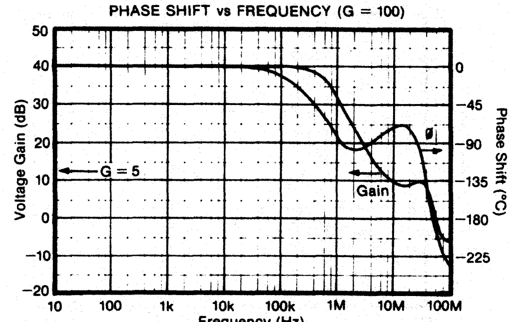
BIAS AND OFFSET CURRENT VS TEMPERATURE



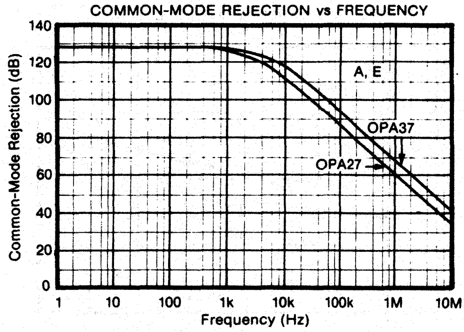
OPA27 CLOSED-LOOP VOLTAGE GAIN AND
PHASE SHIFT vs FREQUENCY (G = 100)



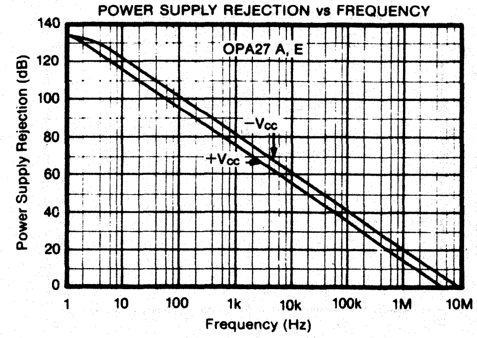
OPA37 CLOSED-LOOP VOLTAGE GAIN AND
PHASE SHIFT vs FREQUENCY (G = 100)



COMMON-MODE REJECTION vs FREQUENCY



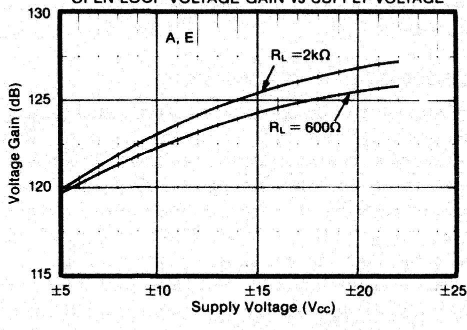
POWER SUPPLY REJECTION vs FREQUENCY



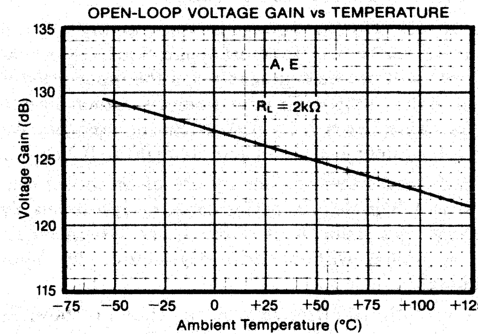
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $\pm V_{CC} = \pm 15VDC$ unless otherwise noted.

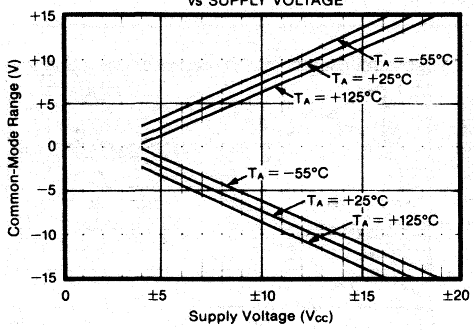
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



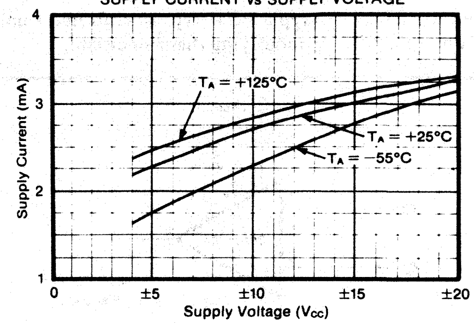
OPEN-LOOP VOLTAGE GAIN vs TEMPERATURE



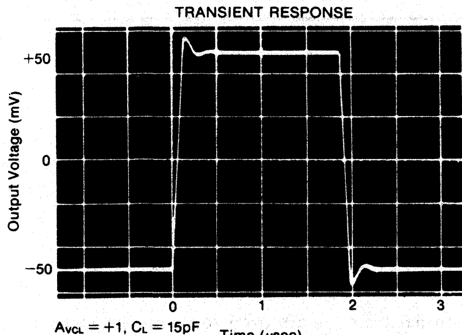
COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



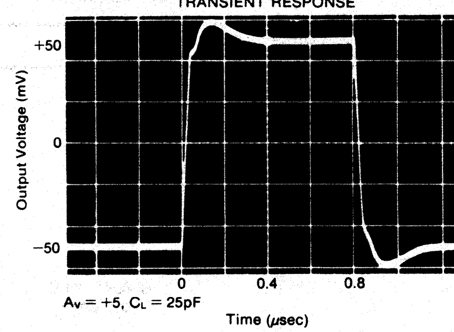
SUPPLY CURRENT vs SUPPLY VOLTAGE



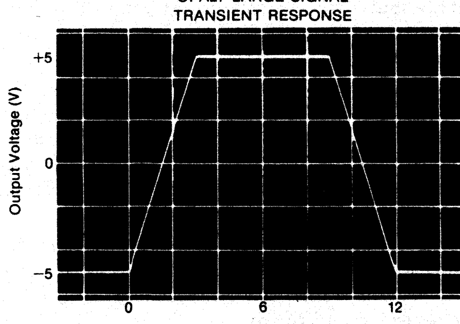
OPA27 SMALL SIGNAL TRANSIENT RESPONSE



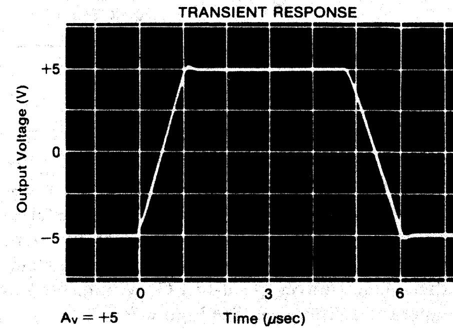
OPA37 SMALL SIGNAL TRANSIENT RESPONSE



OPA27 LARGE SIGNAL TRANSIENT RESPONSE



OPA37 LARGE SIGNAL TRANSIENT RESPONSE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA27/37 offset voltage is laser-trimmed and will require no further trim for most applications. Offset voltage drift will not be degraded when the input offset is nulled with a 10kΩ trim potentiometer. Other potentiometer values from 1kΩ to 1MΩ can be used but V_{OS} drift will be degraded by an additional 0.1 to 0.2μV/°C.

Nulling large system offsets by use of the offset trim adjust will degrade drift performance by approximately 0.3μV/°C per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

The conventional offset voltage trim circuit is shown in Figure 3. For trimming very-small offsets, the higher resolution circuit shown in Figure 4 is recommended.

The OPA27/37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

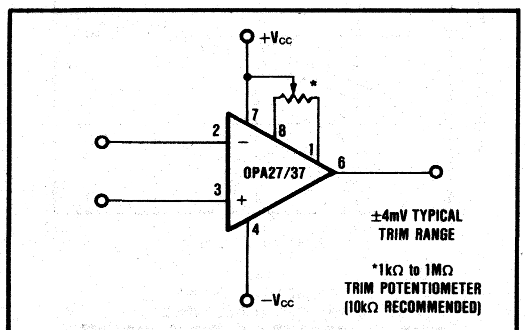


FIGURE 3. Offset Voltage Trim.

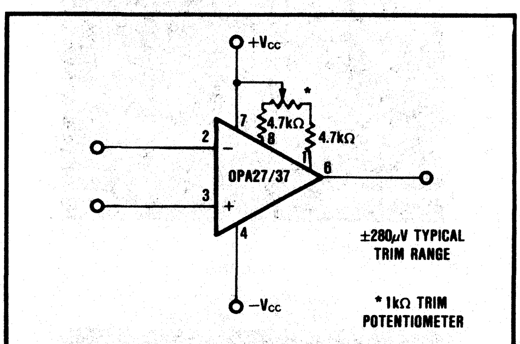


FIGURE 4. High Resolution Offset Voltage Trim.

THERMOELECTRIC POTENTIALS

The OPA27/37 is laser-trimmed to microvolt-level input offset voltage and for very-low input offset voltage drift.

Careful layout and circuit design techniques are necessary to prevent offset and drift errors from external thermoelectric potentials. Dissimilar metal junctions can generate small EMF's if care is not taken to eliminate either their sources (lead-to-PC, wiring, etc.) or their temperature difference. See Figure 7.

Short, direct mounting of the OPA27/37 with close spacing of the input pins is highly recommended. Poor layout can result in circuit drifts and offsets which are an order of magnitude greater than the operational amplifier alone.

NOISE: BIPOLAR VERSUS FET

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the Burr-Brown OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27 (see Figure 5).

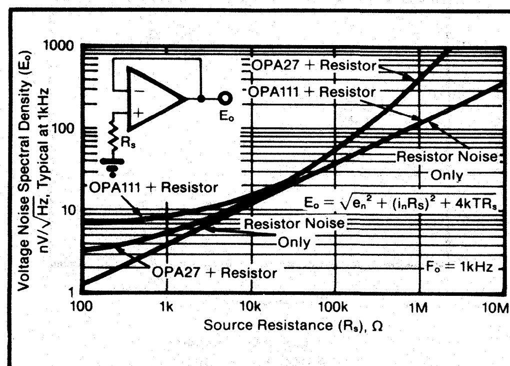


FIGURE 5. Voltage Noise Spectral Density Versus Source Resistance.

COMPENSATION

Although internally compensated for unity-gain stability, the OPA27 may require a small capacitor in parallel with a feedback resistor (R_f) which is greater than 2kΩ. This capacitor will compensate the pole generated by R_f and C_{IN} and eliminate peaking or oscillation.

INPUT PROTECTION

Back-to-back diodes are used for input protection on the OPA27/37. Exceeding a few hundred millivolts differential input signal will cause current to flow and without external current limiting resistors the input will be destroyed.

Accidental static discharge as well as high current can damage the amplifier's input circuit. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may be permanently damaged if any precision operational amplifier is subjected to abuse.

Transient conditions can cause feedthrough due to the amplifier's finite slew-rate. When using the OP-27 as a unity-gain buffer (follower) a feedback resistor of 1kΩ is recommended (see Figure 6).

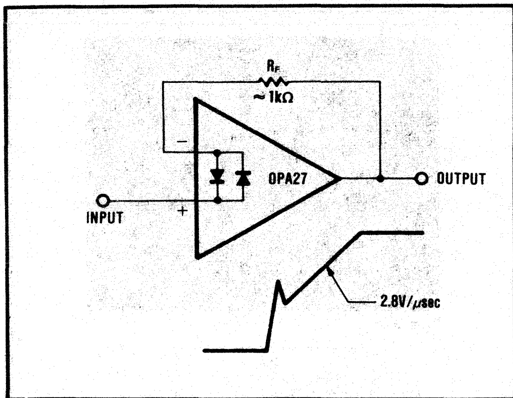


FIGURE 6. Pulsed Operation.

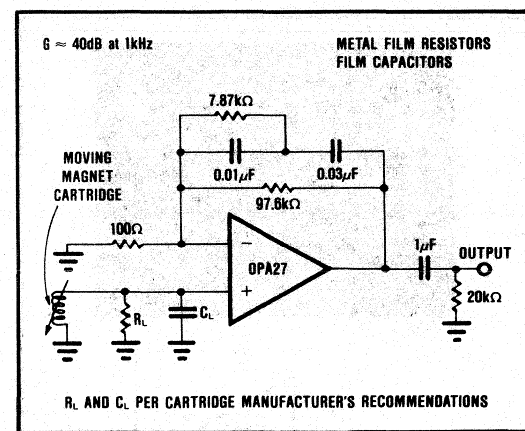


FIGURE 8. Low-Noise RIAA Preamplifier.

APPLICATIONS CIRCUITS

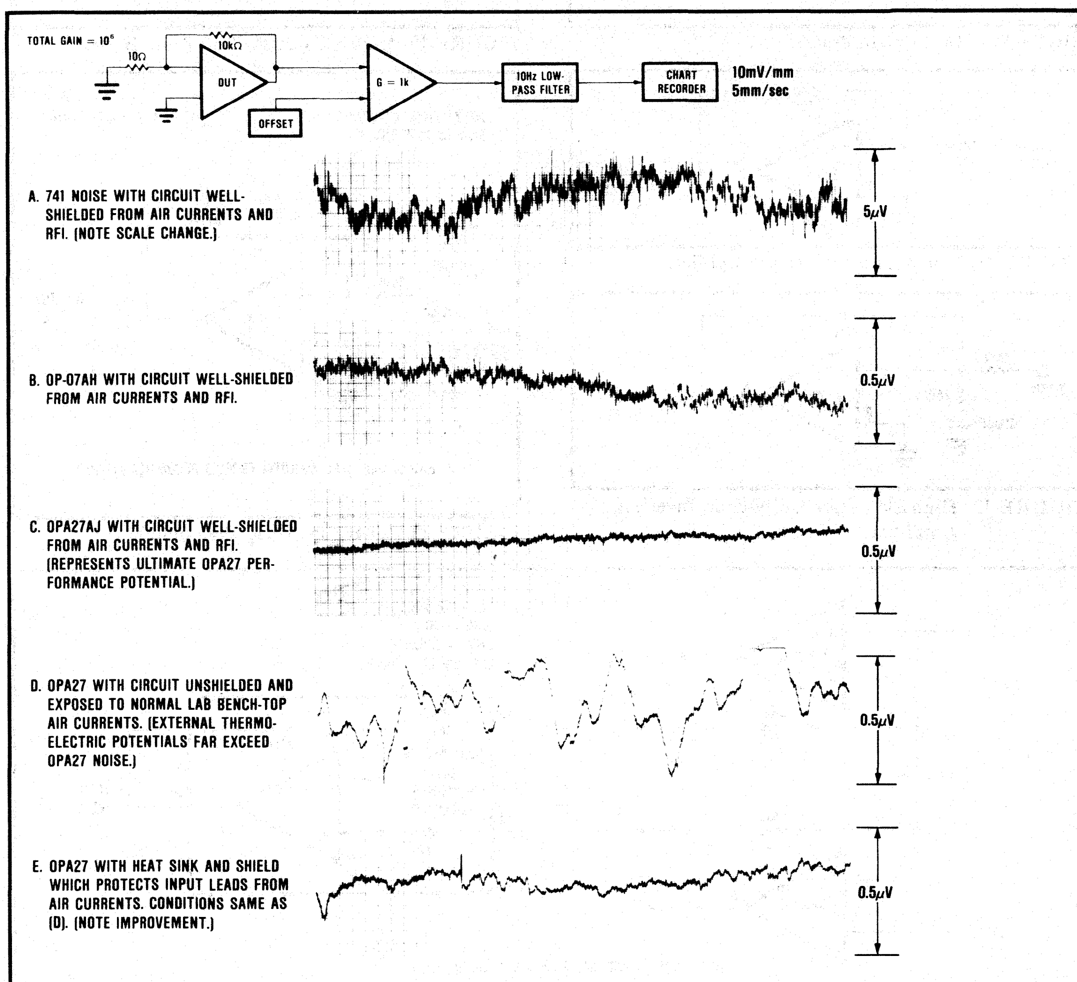


FIGURE 7. Low Frequency Noise Comparison.

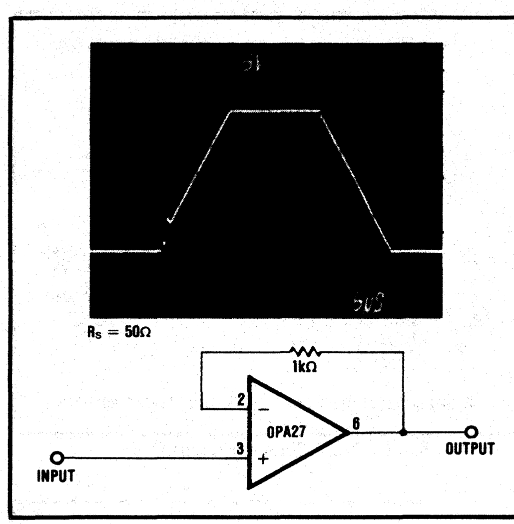


FIGURE 9. Unity-Gain Buffer.

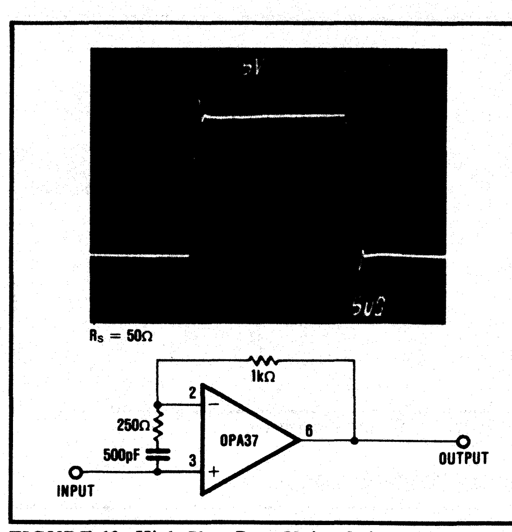


FIGURE 10. High Slew Rate Unity-Gain Buffer.

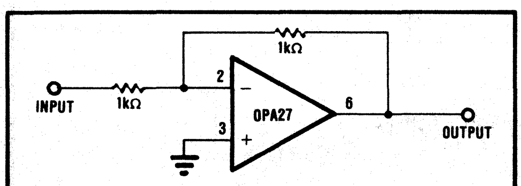


FIGURE 11. Unity-Gain Inverting Amplifier.

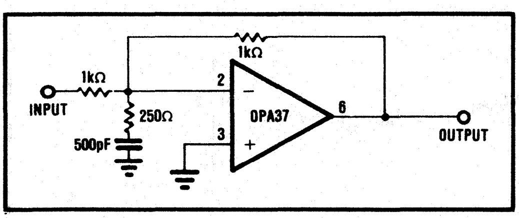


FIGURE 12. High Slew Rate Unity-Gain Inverting Amplifier.

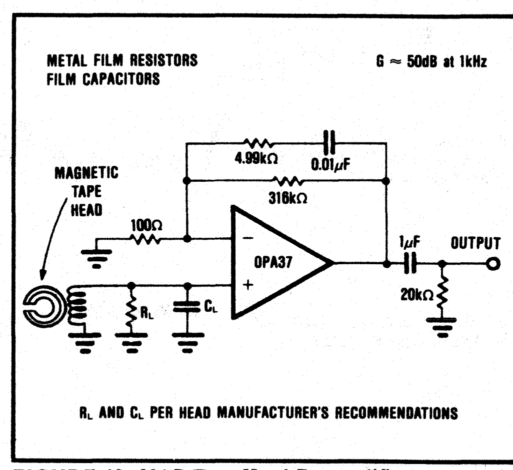


FIGURE 13. NAB Tape Head Preamplifier.

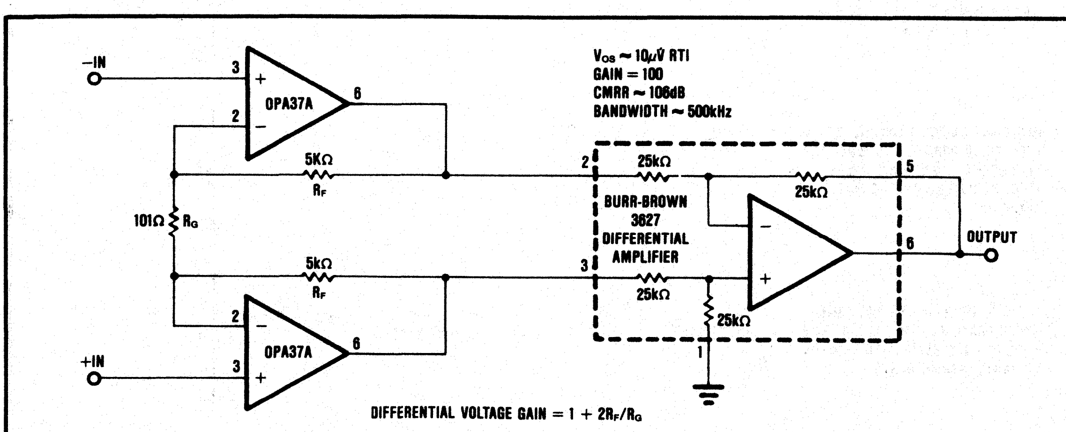
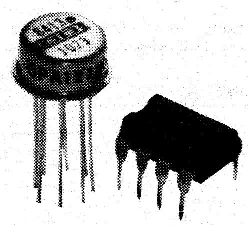


FIGURE 14. Low Noise Instrumentation Amplifier.

BURR-BROWN®



OPA121

Low Cost Precision *Difet*™ OPERATIONAL AMPLIFIER

FEATURES

- **LOW NOISE: 6nV/$\sqrt{Hz}$ typ at 10kHz**
- **LOW BIAS CURRENT: 5pA max**
- **LOW OFFSET: 2mV max**
- **LOW DRIFT: 3μV/°C typ**
- **HIGH OPEN-LOOP GAIN: 110dB min**
- **HIGH COMMON-MODE REJECTION: 86dB min**

APPLICATIONS

- **OPTOELECTRONICS**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**
- **PROFESSIONAL AUDIO EQUIPMENT**
- **MEDICAL EQUIPMENT**
- **RADIATION HARD EQUIPMENT**

DESCRIPTION

The OPA121 is a precision monolithic dielectrically-isolated FET (*Difet*™) operational amplifier. Outstanding performance characteristics are now available for low-cost applications.

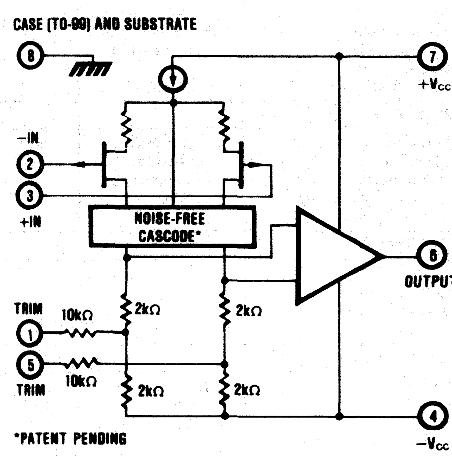
Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patent pending). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.

BIFET® National Semiconductor Corp., *Difet*™ Burr-Brown Corp.



OPA121 SIMPLIFIED CIRCUIT

International Airport Industrial Park · P.O. Box 11400 · Tucson, Arizona 85734 · Tel. (602) 746-1111 · Twx: 910-952-1111 · Cable: BBRCORP · Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA121KM MIN	OPA121KM TYP	OPA121KM MAX	OPA121KP MIN	OPA121KP TYP	OPA121KP MAX	UNITS
INPUT								
NOISE								
Voltage, f_o = 10Hz	(1)		40			50		nV/√Hz
f_o = 100Hz	(1)		15			18		nV/√Hz
f_o = 1kHz	(1)		8			10		nV/√Hz
f_o = 10kHz	(1)		6			7		nV/√Hz
f_B = 10Hz to 10kHz	(1)		0.7			0.8		µV, rms
f_B = 0.1Hz to 10Hz	(1)		1.6			2		µV, p-p
Current, f_B = 0.1Hz to 10Hz	(1)		15			21		fA, p-p
f_o = 0.1Hz thru 20kHz	(1)		0.8			1.1		fA/√Hz
OFFSET VOLTAGE(2)								
Input Offset Voltage	V_{cm} = 0VDC		±0.5	±2		±0.5	±3	mV
Average Drift	T_A = T_{MIN} to T_{MAX}		±3	±10		±3	±10	µV/°C
Supply Rejection		86	104		86	104		dB
			±6	±50		±6	±50	µV/V
BIAS CURRENT(2)								
Input Bias Current	V_{cm} = 0VDC Device operating		±1	±5		±1	±10	pA
OFFSET CURRENT(2)								
Input Offset Current	V_{cm} = 0VDC Device operating		±0.7	±4		±0.7	±8	pA
IMPEDANCE								
Differential			10^{13} ∥ 1			10^{13} ∥ 1		Ω ∥ pF
Common-Mode			10^{14} ∥ 3			10^{14} ∥ 3		Ω ∥ pF
VOLTAGE RANGE								
Common-Mode Input Range		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	104		82	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	R_L ≥ 2kΩ	110	120		106	114		dB
FREQUENCY RESPONSE								
Unity Gain, Small Signal			2			2		MHz
Full Power Response	20V p-p, R_L = 2kΩ		32			32		kHz
Slew Rate	V_o = ±10V, R_L = 2kΩ		2			2		V/µsec
Settling Time, 0.1%	Gain = −1, R_L = 2kΩ		6			6		µsec
0.01%	10V step		10			10		µsec
Overload Recovery, 50% Overdrive(3)	Gain = −1		5			5		µsec
RATED OUTPUT								
Voltage Output	R_L = 2kΩ	±10	±11		±10	±11		V
Current Output	V_o = ±10VDC	±5	±10		±5	±10		mA
Output Resistance	DC, open loop		100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000		pF
Short Circuit Current		10	40		10	40		mA
POWER SUPPLY								
Rated Voltage			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	VDC
Current, Quiescent	I_o = 0mADC		2.5	4.0		2.5	4.5	mA
TEMPERATURE RANGE								
Specification	Ambient temp.	0		+70	0		+70	°C
Operating	Ambient temp.	−40		+85	−25		+85	°C
Storage	Ambient temp.	−65		+150	−55		+125	°C
θ Junction-Ambient			200			150		°C/W

NOTES: (1) Sample tested. (2) Offset voltage, offset current, and bias current are specified with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

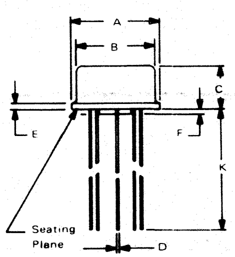
At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

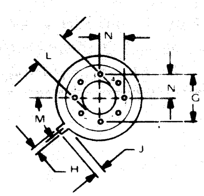
PARAMETER	CONDITIONS	OPA121KM MIN	OPA121KM TYP	OPA121KM MAX	OPA121KP MIN	OPA121KP TYP	OPA121KP MAX	UNITS
TEMPERATURE RANGE								
Specification Range	Ambient temp.	0		+70	0		+70	°C
INPUT								
OFFSET VOLTAGE(1)								
Input Offset Voltage	V_{cm} = 0VDC		±1	±3		±1	±5	mV
Average Drift			±3	±10		±3	±10	µV/°C
Supply Rejection		82	94		82	94		dB
			±20	±80		±20	±80	µV/V
BIAS CURRENT(1)								
Input Bias Current	V_{cm} = 0VDC Device operating		±23	±225		±23	±450	pA
OFFSET CURRENT(1)								
Input Offset Current	V_{cm} = 0VDC Device operating		±16	±180		±16	±360	pA
VOLTAGE RANGE								
Common-Mode Input Range		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	82	98		80	96		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	116		100	110		dB
RATED OUTPUT								
Voltage Output	$R_L = 2k\Omega$	±10	±11		±10	±11		V
Current Output	V_o = ±10VDC	±5	±10		±5	±10		mA
Short Circuit Current	V_o = 0VDC	10	40		10	40		mA
POWER SUPPLY								
Current, Quiescent	I_o = 0mADC		2.5	4.5		2.5	5.0	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

MECHANICAL

"M" PACKAGE TO-99 (Hermetic)





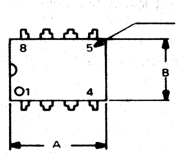
NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

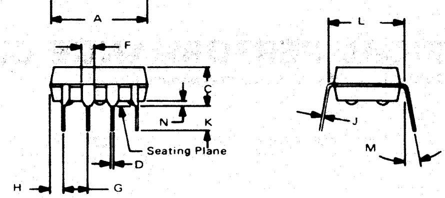
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

"P" PACKAGE 8-pin Plastic



Pin numbers shown for reference only Numbers may not be marked on package

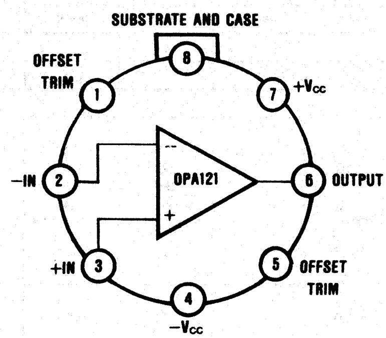


NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.370	.400	9.40	10.16
B	.230	.290	5.84	7.37
C	.120	.200	3.05	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.050	0.76	1.27
J	.008	.015	0.20	0.38
K	.070	.135	1.78	3.43
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.010	.030	0.25	0.76

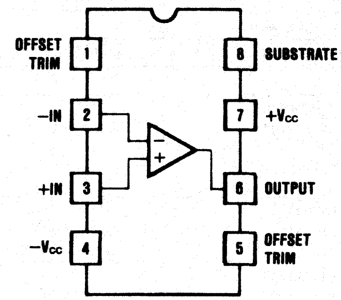
CONNECTION DIAGRAMS

"M" PACKAGE TO-99 (Hermetic)



TOP VIEW

"P" PACKAGE Plastic Mini-DIP



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	−65°C to +150°C (KM)
	−55°C to +125°C (KP)
Operating Temperature Range	−40°C to +85°C (KM)
	−25°C to +85°C (KP)
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[2]	Continuous
Junction Temperature	+175°C

NOTES:
1. Packages must be derated based on θ_{JA} = 150°C/W (KP) or θ_{JA} = 200°C/W (KM).
2. Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

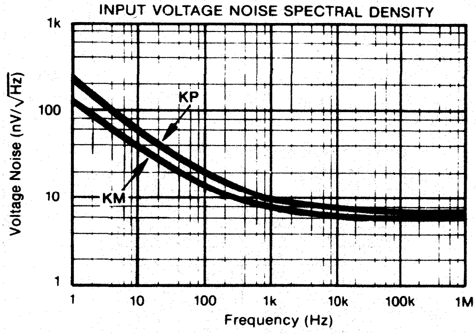
OPA121 K X

- Basic model number — OPA121
- Performance grade — K
  - K = 0°C to +70°C
- Package code — X
  - M = TO-99 metal can
  - P = Plastic mini-DIP

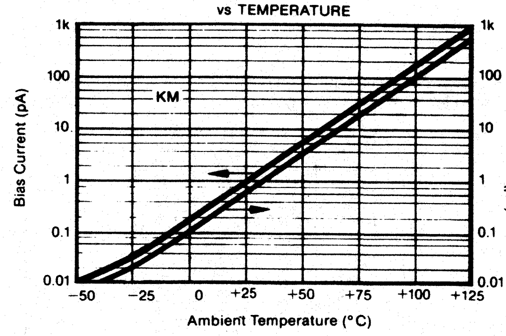
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

INPUT VOLTAGE NOISE SPECTRAL DENSITY



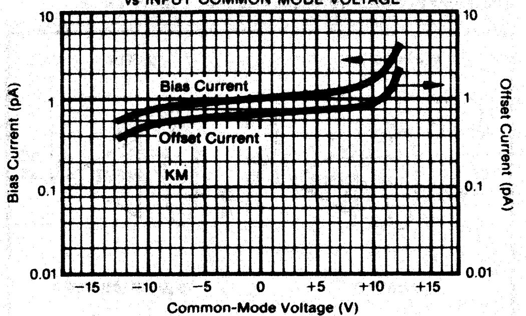
BIAS AND OFFSET CURRENT vs TEMPERATURE



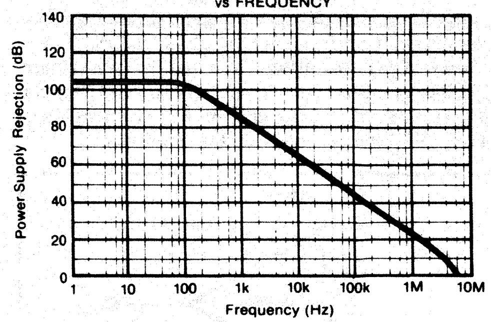
TYPICAL PERFORMANCE CURVES [CONT]

$T_A = +25°C$, $V_{CC} = \pm15VDC$ unless otherwise noted.

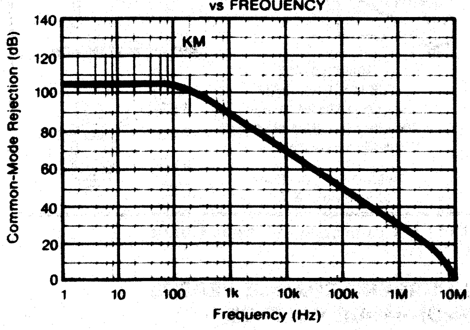
BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



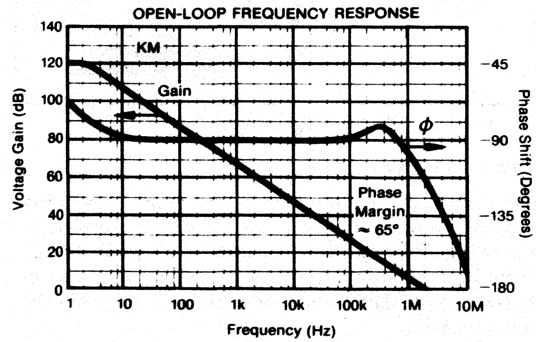
POWER SUPPLY REJECTION vs FREQUENCY



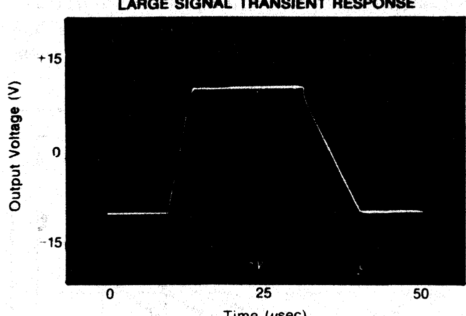
COMMON-MODE REJECTION vs FREQUENCY



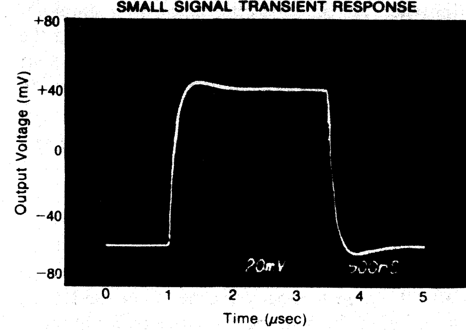
OPEN-LOOP FREQUENCY RESPONSE



LARGE SIGNAL TRANSIENT RESPONSE



SMALL SIGNAL TRANSIENT RESPONSE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA121 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about $0.3\mu V/°C$ for each $100\mu V$ of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA121 can replace most BIFET amplifiers by leaving the external null circuit unconnected.

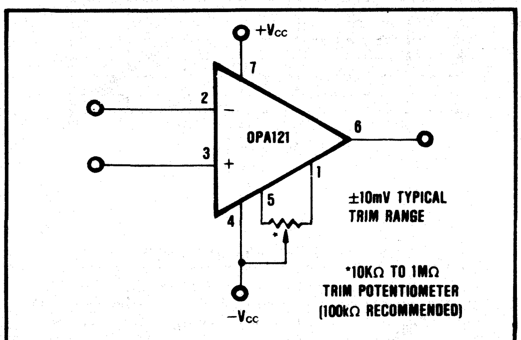


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of −Vcc.

Because of its dielectric isolation, no special protection is needed on the OPA121. Of course, the differential and common-mode voltage limits should be observed.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias curent of the OPA121. To avoid leakage problems, it is recommended that the signal input lead of the OPA121 be wired to a Teflon standoff. If the OPA121 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout.

A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).

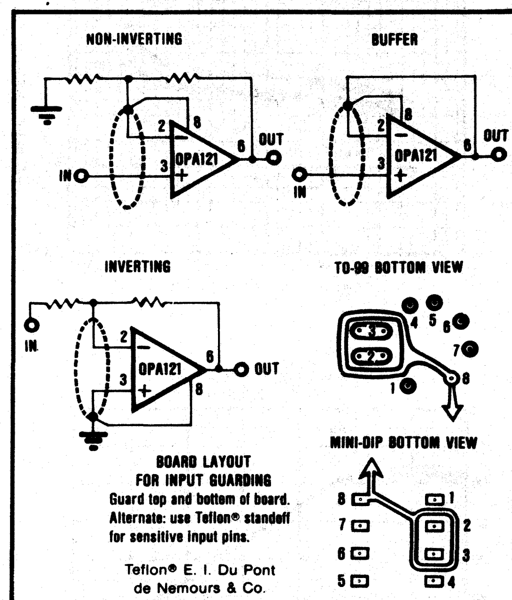


FIGURE 2. Connection of Input Guard.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 3). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA121 is not compromised by common-mode voltage.

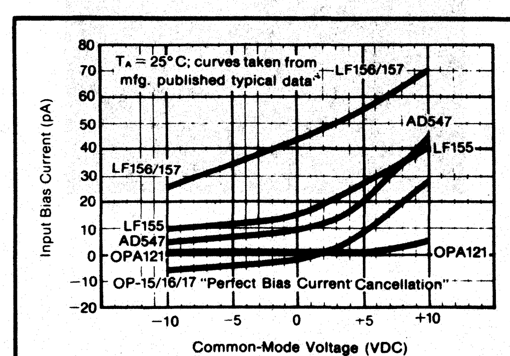


FIGURE 3. Input Bias Current Versus Common-Mode Voltage.

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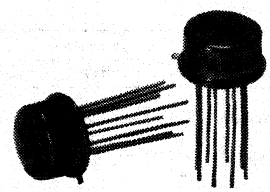


OPA156A
OPA356A

Wide-Bandwidth *Difet*™ OPERATIONAL AMPLIFIER

FEATURES

- **WIDE BANDWIDTH, 4MHz min**
- **HIGH SLEW RATE, 10V/μsec min**
- **LOW BIAS CURRENT, 50pA max at $T_A = +25°C$**
- **LOW OFFSET VOLTAGE, 2mV max**
- **LOW DRIFT, 5μV/°C max**

APPLICATIONS

- **OPTOELECTRONICS**
- **DATA ACQUISITION**
- **IMPROVED REPLACEMENT FOR INDUSTRY-STANDARD LF156A BIFET® OPERATIONAL AMPLIFIER**

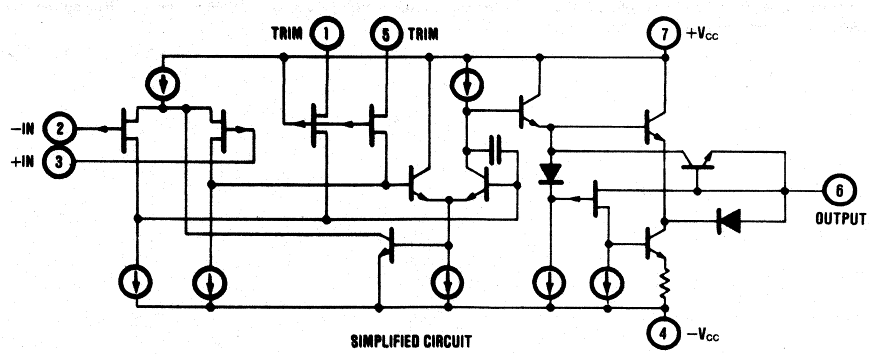
DESCRIPTION

The OPA156A/356A is a wide-bandwidth monolithic dielectrically-isolated FET (*Difet*™) operational amplifier. Improved circuit design and dielectric isolation allow lower bias current than BIFET® LF156A amplfiiers. Bias current is specified under warmed-up and operating conditions, not at a JUNCTION temperature of +25°C.

Laser-trimmed thin-film resistors offer improved offset voltage and noise performance.

The OPA156A is internally compensated for unity-gain stability.

Difet™ Burr-Brown Corp.
BIFET® National Semiconductor Corp.,



SIMPLIFIED CIRCUIT

International Airport Industrial Park · P.O. Box 11400 · Tucson, Arizona 85734 · Tel. (602) 746-1111 · Twx: 910-952-1111 · Cable: BBRCORP · Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At $\pm V_{CC}$ = 15VDC and T_A = +25°C unless otherwise specified.

PARAMETER	CONDITIONS	OPA156A MIN	OPA156A TYP	OPA156A MAX	OPA356A MIN	OPA356A TYP	OPA356A MAX	UNITS
FREQUENCY RESPONSE								
Slew Rate	V_o = ±10V, R_L = 2kΩ, G = +1	10	14		10	14		V/µsec
Settling Time, 0.01%(1)	10V Step, R_L = 2kΩ		4			4		µsec
Gain Bandwidth		4	6		4	6		MHz
INPUT								
NOISE								
Voltage: f_o = 100Hz	R_s = 100Ω		25			25		nV/√Hz
f_o = 1kHz	R_s = 100Ω		15			15		nV/√Hz
Current: f_o = 100Hz			0.005			0.005		pA/√Hz
f_o = 1kHz			0.005			0.005		pA/√Hz
OFFSET VOLTAGE(2)								
Input Offset Voltage	R_s = 50Ω		±1	±2		±1	±2	mV
Average Drift	T_A = T_{MIN} to T_{MAX}		±3	±5		±3	±5	µV/°C
Supply Rejection	$\Delta +V_{CC} = \Delta -V_{CC}$	85	100		85	100		dB
			±10	±57		±10	±57	µV/V
BIAS CURRENT(2)								
Input Bias Current	V_{cm} = 0VDC		30	50		30	50	pA
OFFSET CURRENT(2)								
Input Offset Current	V_{cm} = 0VDC		3	10		3	10	pA
INPUT IMPEDANCE								
Resistance ‖ Capacitance			10^{12} ‖ 3			10^{12} ‖ 3		Ω ‖ pF
VOLTAGE RANGE								
Common-Mode Input Range		±11	±12		±11	±12		V
Common-Mode Rejection	V_{IN} = ±10VDC	85	100		85	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq$ 2kΩ	94	106		94	106		dB
		50	200		50	200		V/mV
RATED OUTPUT								
Voltage Output	R_L = 10kΩ	±12	±13		±12	±13		V
	R_L = 2kΩ	±10	±12		±10	±12		V
POWER SUPPLY								
Rated Voltage			±15			±15		VDC
Voltage Range, Derated Performance		±5		±20	±5		±18	VDC
Current, Quiescent	I_o = 0mADC		5	7		5	10	mA
TEMPERATURE RANGE								
Specification	Ambient temp.	−55		+125	0		+70	°C
Storage	Ambient temp.	−65		+150	−65		+150	°C
θ Junction-Ambient			150			150		°C/W

NOTES: (1) Sample tested—this parameter is not guaranteed. See settling time test circuit (Figure 2). (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $\pm V_{CC}$ = 15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

		OPA156A			OPA356A			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE								
Specification Range	Ambient temp.	−55		+125	0		+70	°C
INPUT								
OFFSET VOLTAGE(1)								
Input Offset Voltage	$R_s = 50\Omega$		±1	±2.5		±1	±2.3	mV
Average Drift	$R_s = 50\Omega$		±3	±5		±3	±5	μV/°C
Supply Rejection	$\Delta{+V_{CC}} = \Delta{-V_{CC}}$	85	100		85	100		dB
			±10	±57		±10	±57	μV/V
BIAS CURRENT(1)								
Input Bias Current	V_{cm} = 0VDC		15	25		3	5	nA
OFFSET CURRENT(1)								
Input Offset Current	V_{cm} = 0VDC		6	10		0.6	1	nA
VOLTAGE RANGE								
Common-Mode Input Range		±11	±12		±11	±12		V
Common-Mode Rejection	V_{IN} = ±10VDC	85	100		85	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	88	92		88	92		dB
		25	40		25	40		V/mV
RATED OUTPUT								
Voltage Output	$R_L = 10k\Omega$	±12	±13		±12	±13		V
	$R_L = 2k\Omega$	±10	±12		±10	±12		V

NOTE: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply: OPA156A	±22VDC
OPA356A	+18VDC
Internal Power Dissipation(1)	670mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration(3)	Continuous
Junction Temperature	+150°C

NOTES: (1) Packages must be derated based on θ_{JC} = 45°C/W or θ_{JA} = 150°C/W. (2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

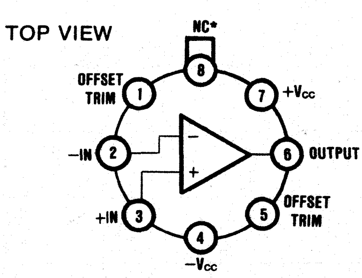
OPA X 56A X

Basic model number

Temperature range
- 1 = −55°C to +125°C
- 3 = 0°C to +70°C

Package code
- M = TO-99

CONNECTION DIAGRAMS

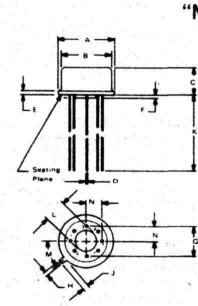


*NO INTERNAL CONNECTION

CASE IS CONNECTED TO V_{CC}

MECHANICAL

"M" PACKAGE: TO-99



NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

The TO-99 can and leads are bright acid tin plated.

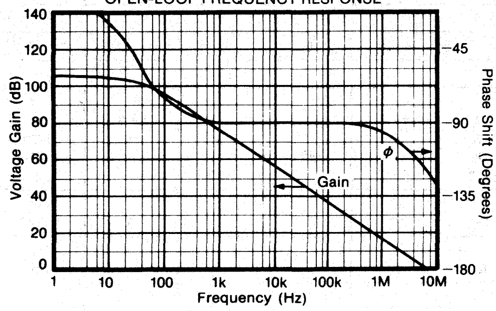
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

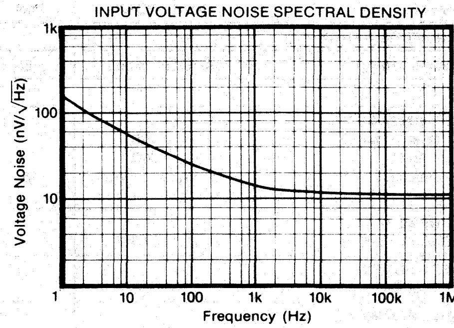
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = \pm15VDC$ unless otherwise noted.

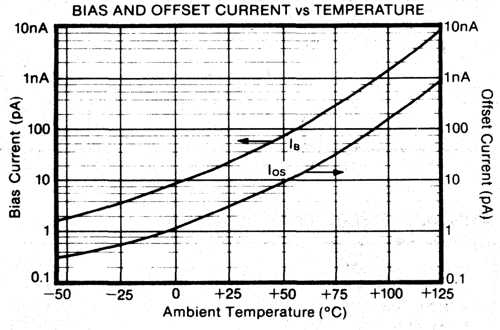
OPEN-LOOP FREQUENCY RESPONSE



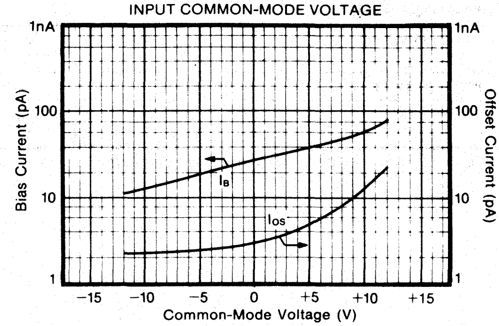
INPUT VOLTAGE NOISE SPECTRAL DENSITY



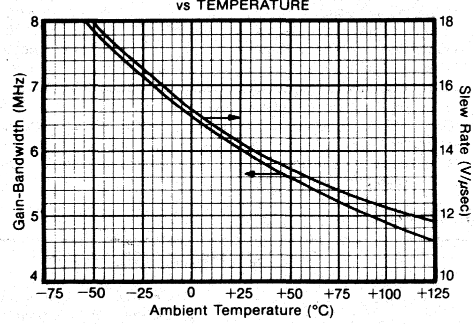
BIAS AND OFFSET CURRENT vs TEMPERATURE



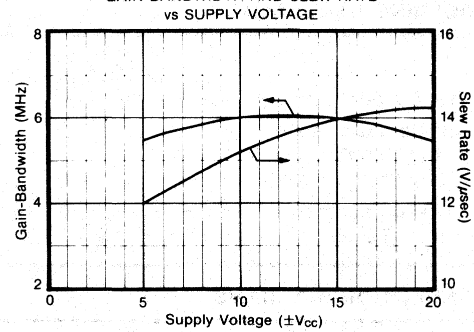
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



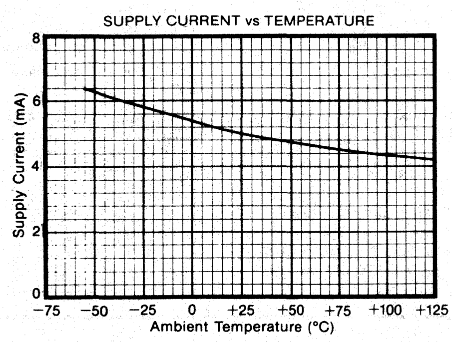
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



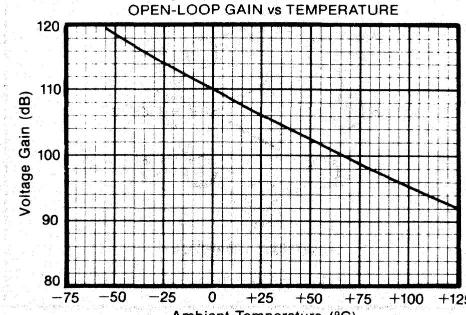
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



SUPPLY CURRENT vs TEMPERATURE



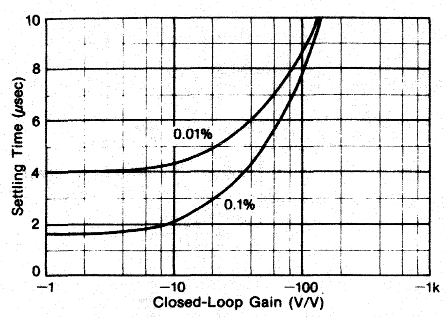
OPEN-LOOP GAIN vs TEMPERATURE



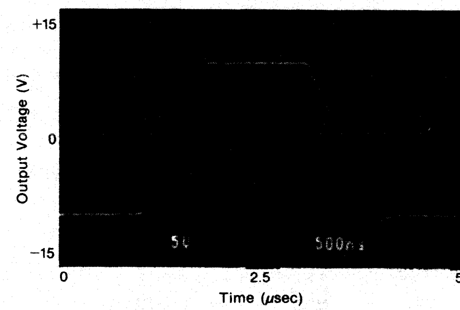
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_{CC} = \pm15VDC$ unless otherwise noted.

SETTLING TIME vs CLOSED-LOOP GAIN



LARGE SIGNAL TRANSIENT RESPONSE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA156A offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.5μV/°C for each millivolt of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as LF156 and OP-16. The OPA156A can replace most other amplifiers by leaving the external null circuit unconnected.

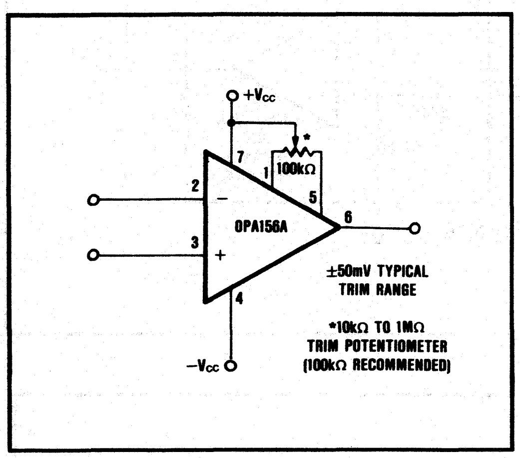


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

If the input voltage exceeds the amplifier's negative supply voltage, input current limiting must be used to prevent damage.

CIRCUIT LAYOUT

Wideband amplifiers require good circuit layout techniques and adequate power supply bypassing. Short, direct connections and good high frequency bypass capacitors (ceramic or tantalum) will help avoid noise pickup or oscillation.

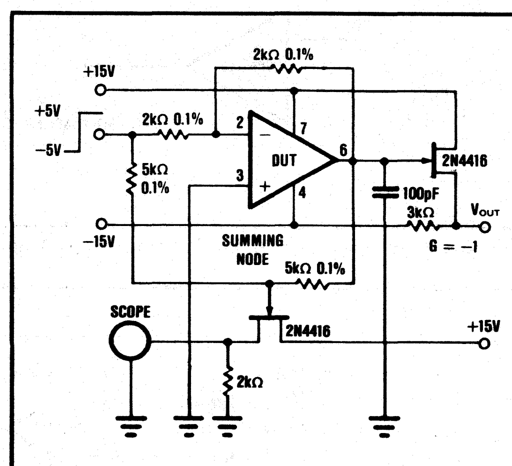


FIGURE 2. Settling Time Test Circuit.

APPLICATIONS CIRCUITS

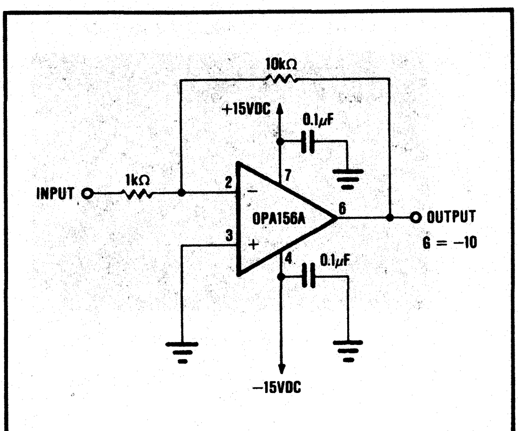


FIGURE 3. Inverting Amplifier.

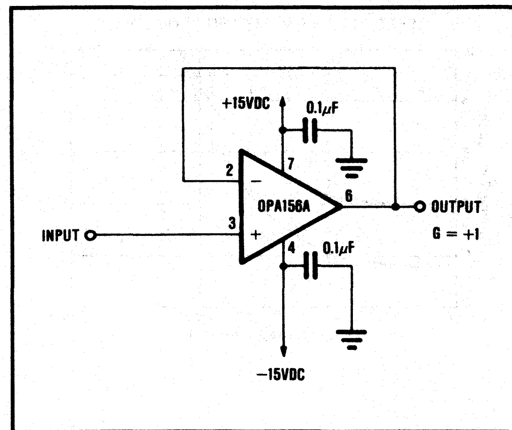


FIGURE 4. Noninverting Buffer.

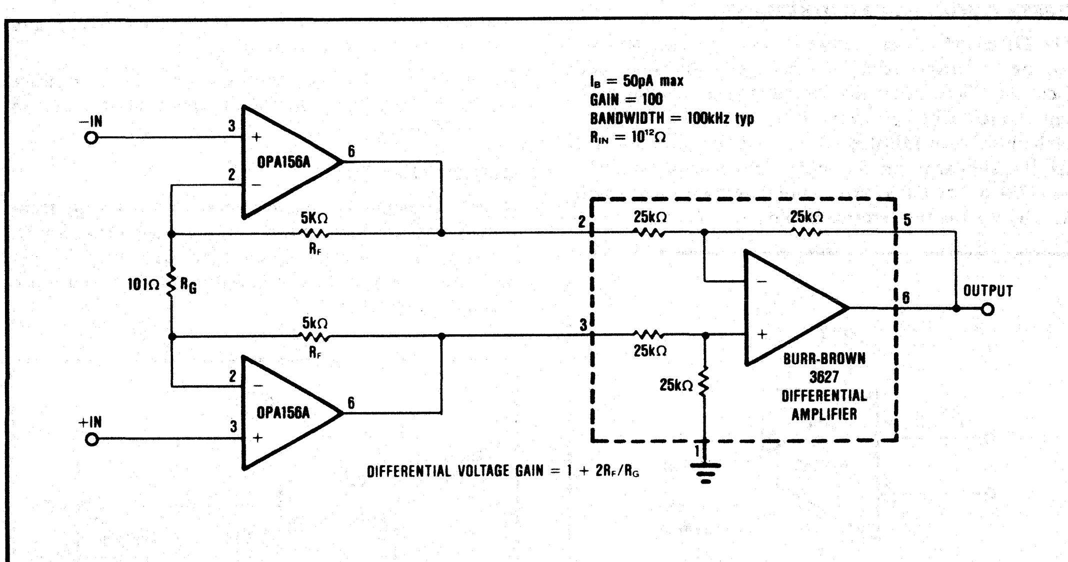


FIGURE 5. Wideband FET Input Instrumentation Amplifier.

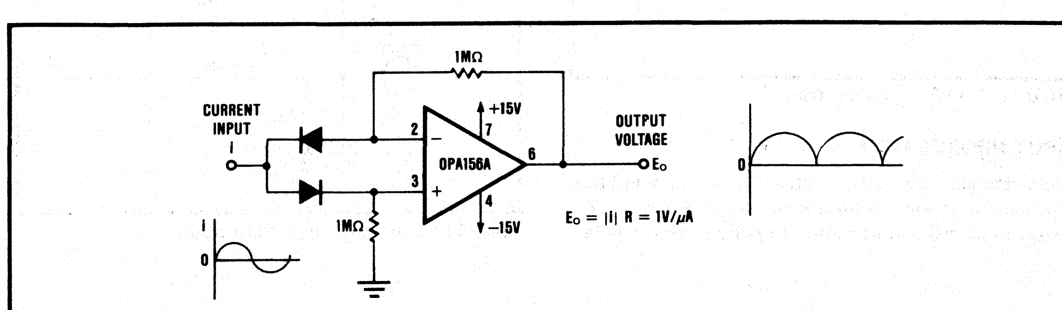


FIGURE 6. Absolute Value Current-to-Voltage Converter.

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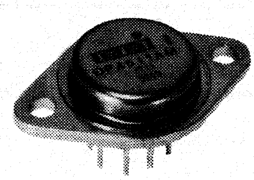


OPA511

High Current—High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE: ±10V to ±30V
- HIGH OUTPUT CURRENT: 5A peak
- CLASS A/B OUTPUT STAGE: Low distortion
- SMALL TO-3 PACKAGE

APPLICATIONS

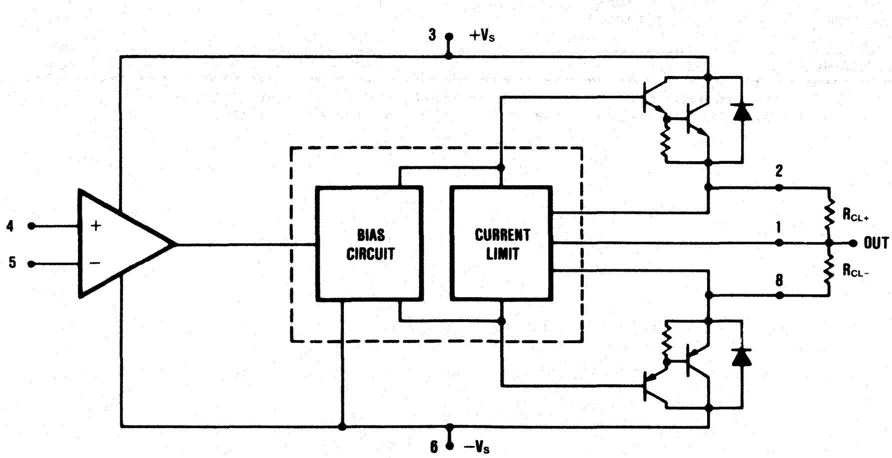
- SERVO AMPLIFIER
- MOTOR DRIVER
- SYNCRO EXCITATION
- AUDIO AMPLIFIER
- TEST PIN DRIVER

DESCRIPTION

The OPA511 is a high voltage, high current operational amplifier designed to drive a wide variety of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from cross-over distortion. User-set current limit circuitry provides protection to the amplifier and load in fault conditions.

The OPA511 employs a laser-trimmed monolithic integrated circuit to bias the output transistors, providing excellent low-level signal fidelity and high output voltage swing. The reduced internal parts count made possible with this bias IC improves performance and reliability.

This hybrid integrated circuit is housed in a hermetically sealed TO-3 package and all circuitry is electrically isolated from the case. This allows direct mounting to a chassis or heat sink without cumbersome insulating hardware and provides optimum heat transfer.



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SPECIFICATIONS

ELECTRICAL

At $T_C = +25°C$ and $V_S = \pm28VDC$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA511AM MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE					
Initial Offset			±5	±10	mV
vs Temperature	Full temperature range		±10	±65	μV/°C
vs Supply Voltage			±35	±200	μV/V
vs Power			±20		μV/W
BIAS CURRENT					
Initial			±15	±40	nA
vs Temperature	Full temperature range		±0.05	±0.4	nA/°C
vs Supply Voltage			±0.02		nA/V
OFFSET CURRENT					
Initial			±5	±10	nA
vs Temperature	Full temperature range		±0.01		nA/°C
INPUT IMPEDANCE					
Common-Mode			200		MΩ
Differential			10		MΩ
VOLTAGE RANGE[1]					
Common-Mode Voltage	Full temperature range	$\pm(\lvert V_S\rvert - 6)$	$\pm(\lvert V_S\rvert - 3)$		V
Common-Mode Rejection	$V_{CM} = V_S - 6V$	70	110		dB
GAIN					
Open-Loop Gain at 10Hz	Full temperature range, full load	91	113		dB
Gain-Bandwidth Product at 1MHz	$T_C = +25°C$, full load		1		MHz
Power Bandwidth	$T_C = +25°C$, $I_O = 4A$, $V_O = 40V$ p-p	15	23		kHz
Phase Margin	Full temperature range		45		Degrees
OUTPUT					
Voltage Swing	$I_O = 5A$	$\pm(\lvert V_S\rvert - 8)$	$\pm(\lvert V_S\rvert - 5)$		V
	Full temperature range, $I_O = 2A$	$\pm(\lvert V_S\rvert - 6)$	$\pm(\lvert V_S\rvert - 5)$		V
	Full temperature range, $I_O = 56mA$	$\pm(\lvert V_S\rvert - 5)$			V
Current, Peak		±5			A
Settling Time to 0.1%	2V step		2		μs
Slew Rate	$R_L = 2.5Ω$	±1.0	1.8		V/μs
Capacitive Load: Unity Gain	Full temperature range			3.3	nF
Gain > 4	Full temperature range			SOA[2]	
POWER SUPPLY					
Voltage	Full temperature range	±10	±28	±30	V
Current, Quiescent			20	30	mA
THERMAL					
RESISTANCE					
AC Junction to Case[3]	f > 60Hz		1.9	2.1	°C/W
DC Junction to Case	f > 60Hz		2.4	2.6	°C/W
Junction to Air			30		°C/W
TEMPERATURE RANGE, case		−25		+85	°C

NOTES: (1) $+V_S$ and $-V_S$ denote the positive and negative supply voltage respectively. Total V_S is measured from $+V_S$ to $-V_S$. (2) SOA = Safe Operating Area. (3) Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 68V
Output Current: source.................................... 5A
sink .... see SOA
Power Dissipation, internal[1] 67W
Input Voltage: differential......................... $\pm(|V_S| - 3V)$
common-mode .... $\pm V_S$
Temperature: junction[1] .... +200°C
pin solder, 10sec .... +300°C
Temperature Range: storage .... −65°C to +150°C
operating (case) .... −25°C to +85°C

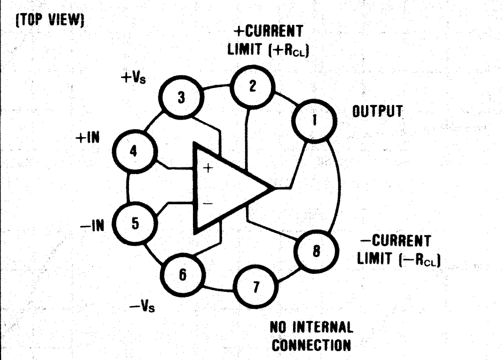
NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

ORDERING INFORMATION

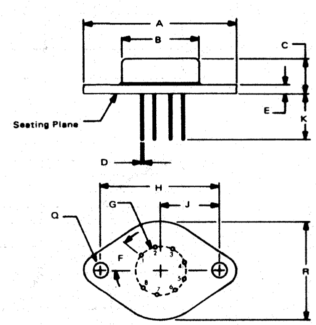
OPA511 A M

Basic Model Number — OPA511
Grade Code — A
Package Code (TO-3) — M

CONNECTION DIAGRAM



MECHANICAL

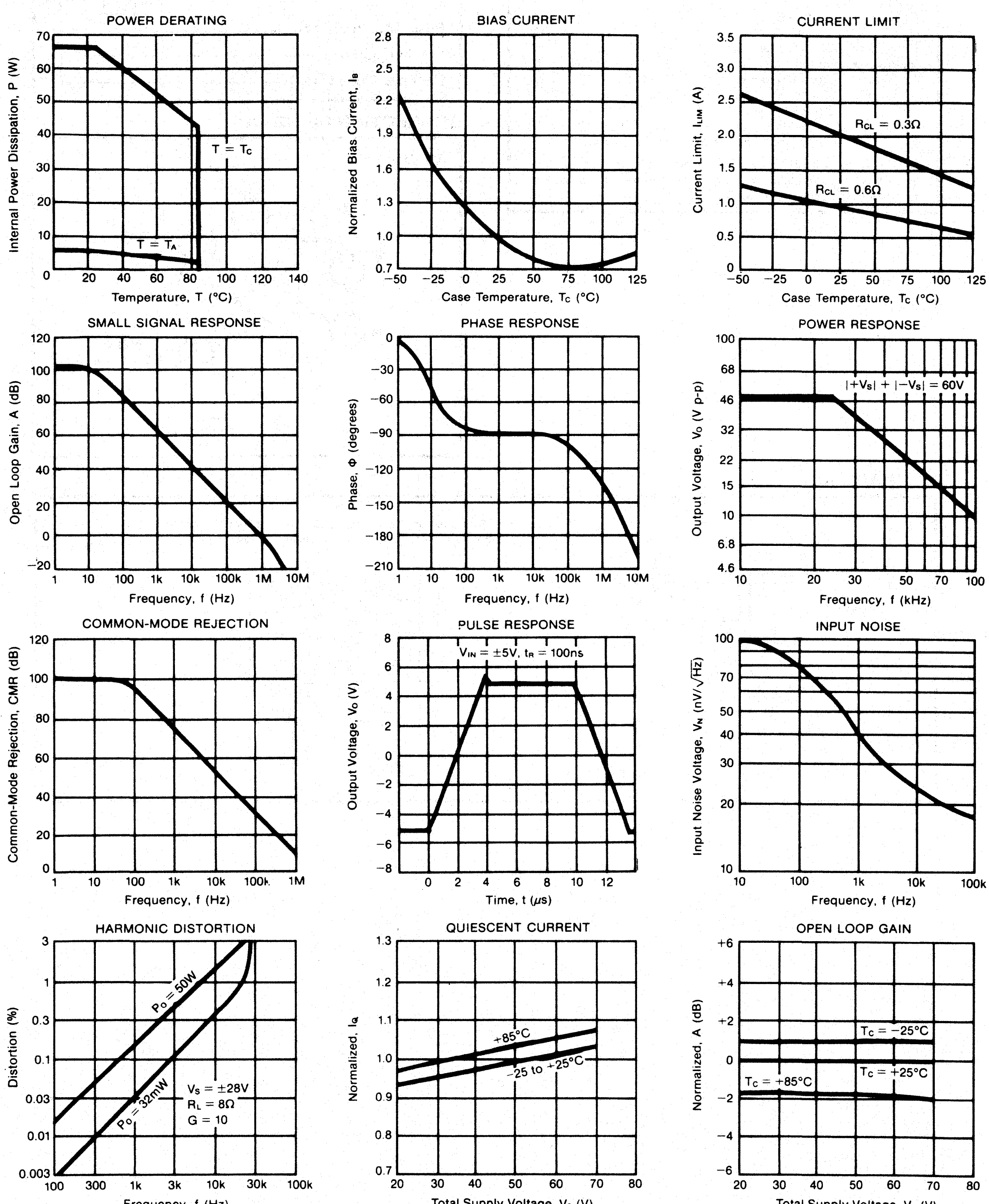


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.240	.290	6.10	7.37
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.583 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

TYPICAL PERFORMANCE CURVES

$T_A = 25°C$. $V_S = \pm 28VDC$ unless otherwise noted.



APPLICATIONS INFORMATION

POWER SUPPLIES

Specifications for the OPA511 are based on a nominal operating voltage of ±28V. A single power supply or unbalanced supplies may be used so long as the maximum total operating voltage (total of $+V_S$ and $-V_S$) is not greater than 68V.

CURRENT LIMITS

Current limit resistors must be provided for proper operation. Independent positive and negative current limit values may be selected by choice of R_{CL+} and R_{CL-} respectively. Resistor values are calculated by:

$$R_{CL} = 0.65/I_{LIM}\,(\text{amps}) - 0.01$$

This is the nominal current limit value at room temperature. The maximum output current decreases at high temperature as shown in the typical performance curve. Most wire-wound resistors are satisfactory, but some highly inductive types may cause loop stability problems. Be sure to evaluate performance with the actual resistors to be used in production.

HEAT SINKING

Power amplifiers are rated by case temperature (not ambient temperature). The maximum allowable power dissipation is a function of the case temperature as shown in the power derating curve. Load characteristics, signal conditions, and power supply voltage determine the power dissipated by the amplifier. The case temperature will be determined by the heat sinking conditions. Sufficient heat sinking must be provided to keep the case temperature within safe bounds given the power dissipated and ambient temperature. See Applications Note AN-83 for further details.

SAFE OPERATING AREA (SOA)

The safe area plot provides a comprehensive summary of the power handling limitations of a power amplifier, including maximum current, voltage and power as well as the secondary breakdown region (see Figure 1). It shows the allowable output current as a function of the power supply to output voltage differential (voltage across the conducting power device). See Applications Note AN-123 for details on SOA.

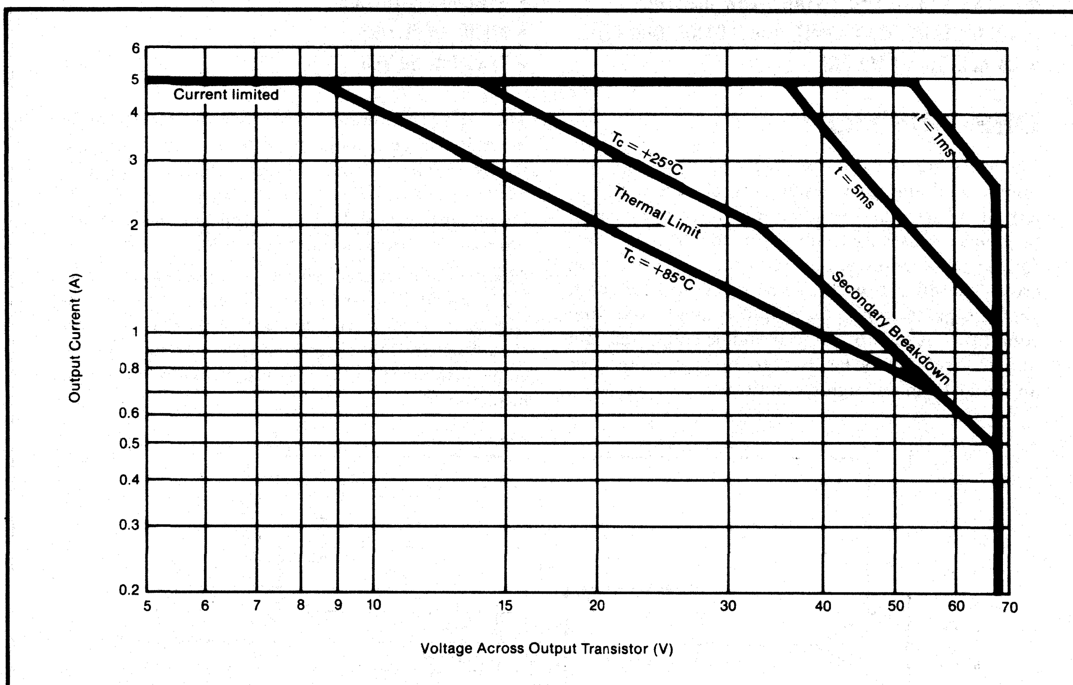


FIGURE 1. Safe Operating Area.

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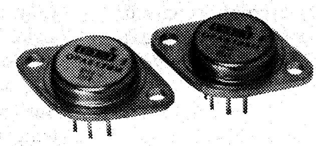
OPA512



Very-High Current—High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE: ±10V to ±50V
- HIGH OUTPUT CURRENT: 15A peak
- CLASS A/B OUTPUT STAGE: Low distortion
- VOLTAGE-CURRENT LIMIT PROTECTION CIRCUIT
- SMALL TO-3 PACKAGE

APPLICATIONS

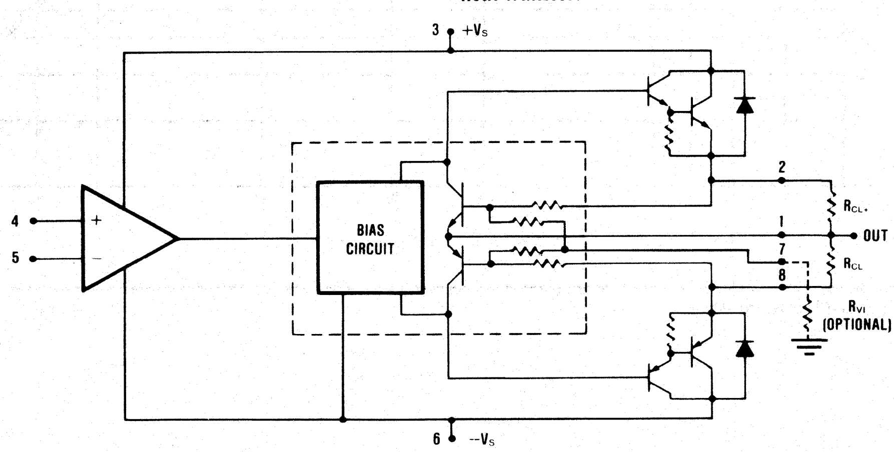
- SERVO AMPLIFIER
- MOTOR DRIVER
- SYNCRO EXCITATION
- AUDIO AMPLIFIER
- TEST PIN DRIVER

DESCRIPTION

The OPA512 is a high voltage, very-high current operational amplifier designed to drive a wide variety of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from cross-over distortion. User-set current limit circuitry provides protection to the amplifier and load in fault conditions. A resistor-programmable voltage-current limiter circuit may be used to further protect the amplifier from damaging conditions.

The OPA512 employs a laser-trimmed monolithic integrated circuit to bias the output transistors, providing excellent low-level signal fidelity and high output voltage swing. The reduced internal parts count made possible with this monolithic IC improves performance and reliability.

This hybrid integrated circuit is housed in a hermetically-sealed TO-3 package and all circuitry is electrically-isolated from the case. This allows direct mounting to a chassis or heat sink without cumbersome insulating hardware and provides optimum heat transfer.



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SPECIFICATIONS

ELECTRICAL

At $T_C = +25°C$ and $V_S = \pm 40VDC$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA512BM MIN	OPA512BM TYP	OPA512BM MAX	OPA512SM MIN	OPA512SM TYP	OPA512SM MAX	UNITS
INPUT								
OFFSET VOLTAGE								
Initial Offset			±2	±6		±1	±3	mV
vs Temperature	Specified temp. range		±10	±65		*	±40	μV/°C
vs Supply Voltage			±30	±200		*	*	μV/V
vs Power			±20			*		μV/W
BIAS CURRENT								
Initial			12	30		10	20	nA
vs Temperature	Specified temp. range		±50	400		*	*	pA/°C
vs Supply Voltage			±10			*		pA/V
OFFSET CURRENT								
Initial			±12	±30		±5	±10	nA
vs Temperature	Specified temp. range		±50			*		pA/°C
INPUT IMPEDANCE, DC			200			*		MΩ
INPUT CAPACITANCE			3			*		pF
VOLTAGE RANGE								
Common-Mode Voltage	Specified temp. range	$\pm(\|V_S\| - 5)$	$\pm(\|V_S\| - 3)$		*	*		V
Common-Mode Rejection	Specified temp. range	74	100		*	*		dB
GAIN								
Open-Loop Gain at 10Hz	1kΩ load		110			*		dB
	Specified temp. range, 8Ω load	96	108		*	*		dB
Gain-Bandwidth Product, 1MHz	8Ω load		4			*		MHz
Power Bandwidth	8Ω load	13	20		*	*		kHz
Phase Margin	Specified temp. range, 8Ω load		20			*		Degrees
OUTPUT								
Voltage Swing[1]	BM at 10A, SM at 15A	$\pm(\|V_S\| - 6)$			$\pm(\|V_S\| - 7)$			V
	Specified temp. range, $I_O = 80mA$	$\pm(\|V_S\| - 5)$			*			V
	$I_O = 5A$	$\pm(\|V_S\| - 5)$			*			V
Current, Peak		10			15			A
Settling Time to 0.1%	2V step		2			*		μs
Slew Rate		2.5	4		*	*		V/μs
Capacitive Load	Specified temp. range, G = 1			1.5			*	nF
	Specified temp. range, G > 10			SOA[2]			*	
POWER SUPPLY								
Voltage	Specified temp. range	±10	±40	±45	*	*	±50	V
Current, Quiescent			25	50		*	35	mA
THERMAL								
RESISTANCE								
AC Junction to Case[3]	$T_C = -55°C$ to $+125°C$, f > 60Hz		0.8	0.9		*	*	°C/W
DC Junction to Case	$T_C = -55°C$ to $+125°C$		1.25	1.4		*	*	°C/W
Junction to Air	$T_C = -55°C$ to $+125°C$		30			*		°C/W
TEMPERATURE RANGE, specified	T_C	−25		+85	−55		+125	°C

*Specification same as OPA512BM.

NOTES: (1) $+V_S$ and $-V_S$ denote the positive and negative supply voltage respectively. Total V_S is measured from $+V_S$ to $-V_S$. (2) SOA = Safe Operating Area. (3) Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$	100V
Output Current: source	15A
sink	see SOA
Power Dissipation, internal[1]	125W
Input Voltage: differential	$\pm(\lvert V_S\rvert - 3V)$
common-mode	$\pm V_S$
Temperature: pin solder, 10s	+300°C
junction[1]	+200°C
Temperature Range: storage[2]	−65°C to +150°C
operating (case)	−55°C to +125°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. (2) OPA512BM, −55°C to +100°C.

ORDERING INFORMATION

OPA512 X M

Basic Model Number

Performance Grade Code

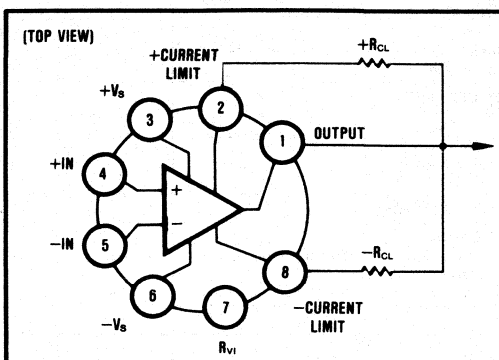
B = −25°C to +85°C

S = −55°C to +125°C

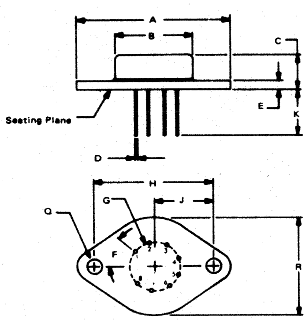
Package Code (TO-3)

M = TO-3

CONNECTION DIAGRAM



MECHANICAL



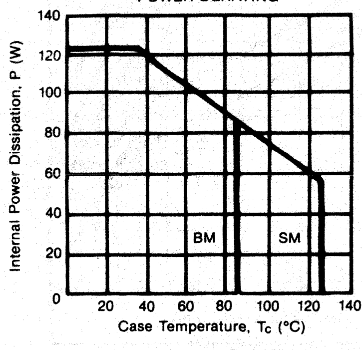
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.240	.290	6.10	7.37
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.583 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

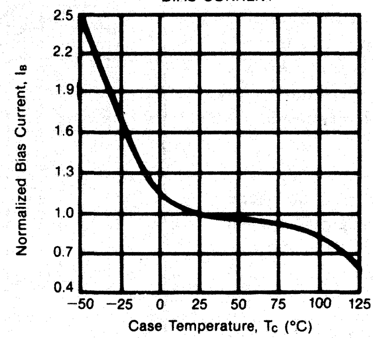
TYPICAL PERFORMANCE CURVES

$T_A = 25°C$, $V_S = ±40VDC$ unless otherwise noted.

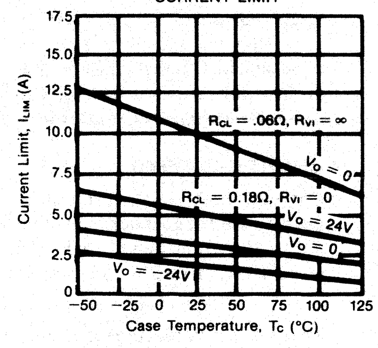
POWER DERATING



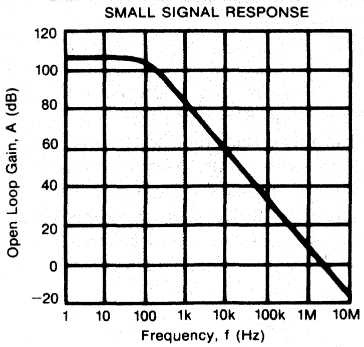
BIAS CURRENT



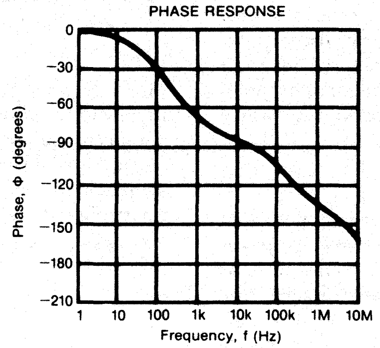
CURRENT LIMIT



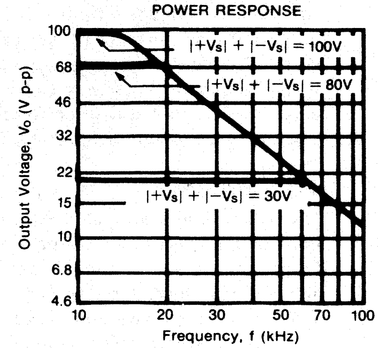
SMALL SIGNAL RESPONSE



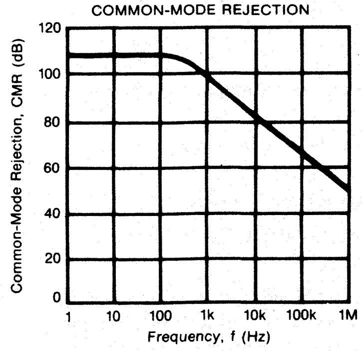
PHASE RESPONSE



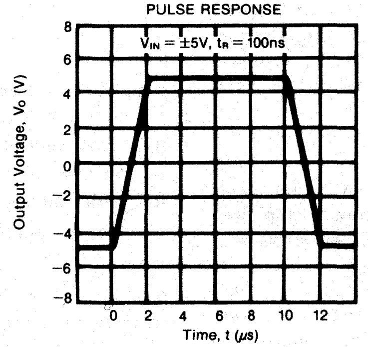
POWER RESPONSE



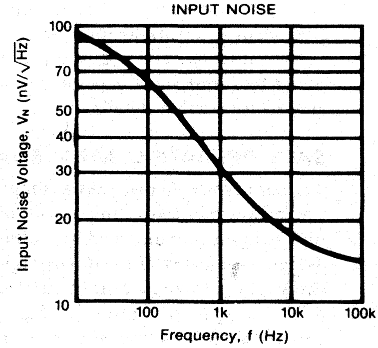
COMMON-MODE REJECTION



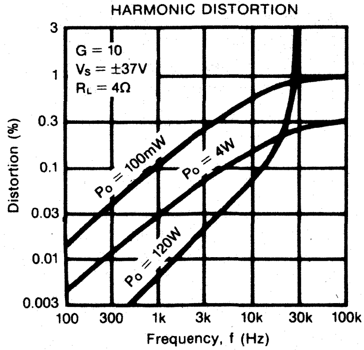
PULSE RESPONSE



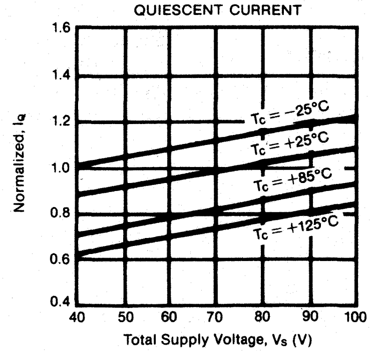
INPUT NOISE



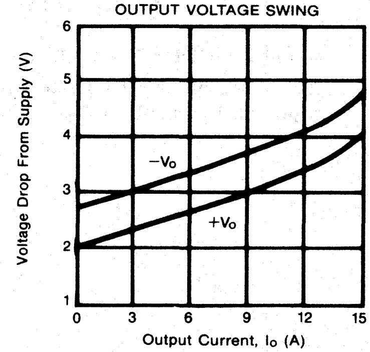
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



APPLICATIONS INFORMATION

POWER SUPPLIES

Specifications for the OPA512 are based on a nominal operating voltage of ±40V. A single power supply or unbalanced supplies may be used as long as the maximum total operating voltage (total of $+V_S$ and $-V_S$) is not greater than 90V (100V for "S" grade version).

CURRENT LIMITS

Current limit resistors must be provided for proper operation. Independent positive and negative current limit values may be selected by choice of R_{CL+} and R_{CL-} respectively. Resistor values are calculated by:

$$R_{CL} = 0.65/I_{LIM} \text{ (amps)} - 0.007$$

This is the nominal current limit value at room temperature. The maximum output current decreases at high temperature as shown in the typical performance curve. Most wire-wound resistors are satisfactory, but some highly inductive types may cause loop stability problems. Be sure to evaluate performance with the actual resistors to be used in production.

HEAT SINKING

Power amplifiers are rated by case temperature (not ambient temperature). The maximum allowable power dissipation is a function of the case temperature as shown in the power derating curve. Load characteristics, signal conditions, and power supply voltage determine the power dissipated by the amplifier. The case temperature will be determined by the heat sinking conditions. Sufficient heat sinking must be provided to keep the case temperature within safe bounds given the power dissipated and ambient temperature. See Applications Note AN-83 for further details.

SAFE OPERATING AREA (SOA)

The safe area plot provides a comprehensive summary of the power handling limitations of a power amplifier, including maximum current, voltage and power as well as the secondary breakdown region (see Figure 1). It shows the allowable output current as a function of the power supply to output voltage differential (voltage across the conducting power device). See Applications Note AN-123 for details on SOA.

VOLTAGE-CURRENT LIMITER CIRCUITRY

The voltage-current (V-I) limiter circuit provides a means to protect the amplifier from SOA damage such as a short circuit to ground, yet allows high output currents to flow under normal load conditions. Sensing both the output current and the output voltage, this limiter circuit increases the current limit value as the output voltage approaches the power supply voltage (where power dissipation is low). This type of limiting is achieved by connecting pin 7 through a programming resistor to ground. The V-I limiter circuit is governed by the equation:

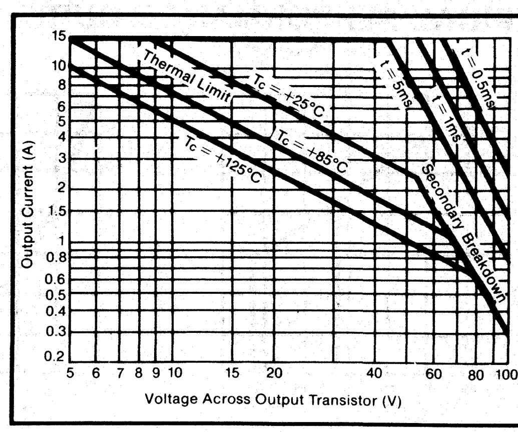


FIGURE 1. Safe Operating Area.

$$I_{LIMIT} = \frac{0.65 + \dfrac{0.28\ V_O}{20 + R_{VI}}}{R_{CL} + 0.007}$$

where:

I_{LIMIT} is the maximum current available at a given output voltage.

R_{VI} is the value (kΩ) of the resistor from pin 7 to ground.

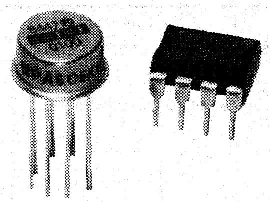
R_{CL} is the current limit resistor in ohms.

V_O is the instantaneous output voltage in volts.

Reactive or EMF generating loads may produce unusual (perhaps undesirable) waveforms with the V-I limit circuit driven into limit. Since current peaks in a reactive load do not align with the output voltage peaks, the output waveform will not appear as a simple voltage-limited waveform. Response of the load to the limiter, in fact, may produce a "backfire" reaction producing unusual output waveforms.

BURR-BROWN®

OPA606



Wide-Bandwidth *Difet*™ OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH, 13MHz typ
- HIGH SLEW RATE, 35V/μsec typ
- LOW BIAS CURRENT, 10pA max at $T_A = +25°C$
- LOW OFFSET VOLTAGE, 500μV max
- LOW DISTORTION, 0.0035% typ at 10kHz

APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- AUDIO AMPLIFIERS

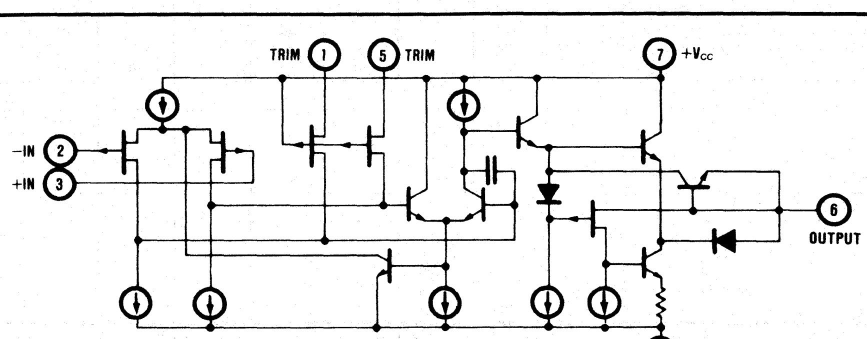
DESCRIPTION

The OPA606 is a wide-bandwidth monolithic dielectrically-isolated FET (*Difet*™) operational amplifier featuring a wider bandwidth and lower bias current than BIFET® LF156A amplifiers. Bias current is specified under warmed-up and operating conditions, not at a JUNCTION temperature of +25°C.

Laser-trimmed thin-film resistors offer improved offset voltage and noise performance.

The OPA606 is internally compensated for unity-gain stability.

Difet™ Burr-Brown Corp., Bifet® National Semiconductor Corp.



SIMPLIFIED CIRCUIT

International Airport Industrial Park · P.O. Box 11400 · Tucson, Arizona 85734 · Tel. (602) 746-1111 · Twx: 910-952-1111 · Cable: BBRCORP · Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm15VDC$ and $T_A = +25°C$ unless otherwise specified.

		OPA606KM/SM			OPA606LM			OPA606KP			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE											
Gain Bandwidth	Small signal	10	12.5		11	13		9	12		MHz
Full Power Response	20V p-p, $R_L = 2k\Omega$		515			550			470		kHz
Slew Rate	$V_O = \pm10V$, $R_L = 2k\Omega$	22	33		25	35		20	30		V/μsec
Settling Time[1]: 0.1%	Gain = −1, $R_L = 2k\Omega$		1.0			1.0			1.0		μsec
0.01%	10V step		2.1			2.1			2.1		μsec
Total Harmonic Distortion	G = +1, 20V p-p, $R_L = 2k\Omega$, f = 10kHz		0.0035			0.0035			0.0035		%
INPUT											
OFFSET VOLTAGE[2]											
Input Offset Voltage	$V_{CM} = 0VDC$		±180	±1.5mV		±100	±500		±300	±3mV	μV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±5			±3	±5		±10		μV/°C
Supply Rejection	$V_{CC} = \pm10V$ to $\pm18V$	82	100		90	104		80	90		dB
			±10	±79		±6	±32		±32	±100	μV/V
BIAS CURRENT[2]											
Input Bias Current	$V_{CM} = 0VDC$		±7	±15		±5	±10		±8	±25	pA
OFFSET CURRENT[2]											
Input Offset Current	$V_{CM} = 0VDC$		±0.6	±10		±0.4	±5		±1	±15	pA
NOISE											
Voltage, f_O = 10Hz	100% tested (L)		37			30	40		37		nV/√Hz
100Hz	100% tested (L)		21			20	28		21		nV/√Hz
1kHz	100% tested (L)		14			13	16		14		nV/√Hz
10kHz	(3)		12			11	13		12		nV/√Hz
20kHz	(3)		11			10.5	13		11		nV/√Hz
f_B = 10Hz to 10kHz	(3)		1.3			1.2	1.5		1.3		μV rms
Current, f_O = 0.1Hz thru 20kHz	(3)		1.5			1.3	2		1.7		fA/√Hz
IMPEDANCE											
Differential			$10^{13} \parallel 1$			$10^{13} \parallel 1$			$10^{13} \parallel 1$		Ω ∥ pF
Common-Mode			$10^{14} \parallel 3$			$10^{14} \parallel 3$			$10^{14} \parallel 3$		Ω ∥ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10.5	±11.5		±11	±11.6		±10.2	±11		V
Common-Mode Rejection	$V_{IN} = \pm10VDC$	80	95		85	96		78	90		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	95	115		100	118		90	110		dB
RATED OUTPUT											
Voltage Output	$R_L = 2k\Omega$	±11	±12.2		±12	±12.6		±11	±12		V
Current Output	$V_O = \pm10VDC$	±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		40			40			40		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	20		10	20		10	20		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	$I_O = 0mADC$		6.5	9.5		6.2	9		6.5	10	mA
TEMPERATURE RANGE											
Specification	Ambient temp. KM, KP, LM	0		+70	0		+70	0		+70	°C
	SM	−55		+125							°C
Operating	Ambient Temp.	−55		+125	−55		+125	−25		+85	°C
θ Junction-Ambient			200			200			155		°C/W

NOTES: (1) See settling time test circuit in Figure 2. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Sample tested—this parameter is guaranteed on L grade only.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

		OPA606KM/SM			OPA606LM			OPA606KP			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE											
Specification Range	Ambient temp. KM	0		+70	0		+70	0		+70	°C
	SM	−55		+125							°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC KM		±400	±2mV		±335	±750		±750	±3.5mV	µV
	SM		±680	±3mV							µV
Average Drift			±5			±3	±5		±10		µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	80	98		85	100		78	95		dB
			±13	±100		±10	±56		±18	±126	µV/V
BIAS CURRENT[1]											
Input Bias Current	V_{CM} = 0VDC KM		±158	±339		±113	±226		±181	±566	pA
	SM		±7.2	±15.4							nA
OFFSET CURRENT[1]											
Input Offset Current	V_{CM} = 0VDC KM		±14	±226		±9	±113		±23	±339	pA
	SM		±614	±10.2nA							pA
VOLTAGE RANGE											
Common-Mode Input Range		±10.4	±11.4		±10.9	±11.5		±10	±10.9		V
Common-Mode Rejection	V_{IN} = ±10VDC	78	92		82	95		75	88		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	90	106		95	112		88	104		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10.5	±12		±11.5	±12.4		±10.4	±11.8		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		6.6	10		6.4	9.5		6.6	10.5	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ORDERING INFORMATION

OPA606 X X

Basic model number

Performance grade
K, L = 0°C to +70°C
S = −55°C to +125°C

Package code
M = TO-99 metal can
P = 8-pin plastic DIP (K grade only)

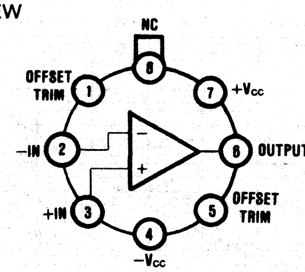
ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	M = −65°C to +150°C, P = −40°C to +85°C
Operating Temperature Range	M = −55°C to +125°C, P = −40°C to +85°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{JC} = 15°C/W or θ_{JA}. (2) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to the negative supply voltage. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

CONNECTION DIAGRAMS

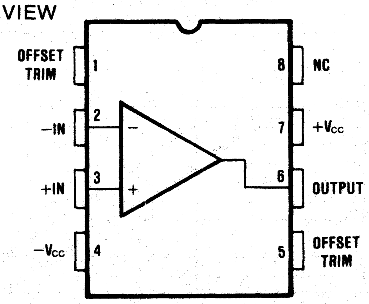
TOP VIEW TO-99



CASE IS CONNECTED TO V_{CC}

MECHANICAL

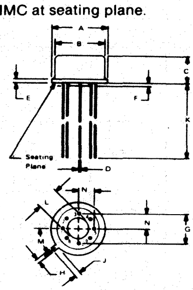
TOP VIEW DIP



MECHANICAL

"M" PACKAGE — TO-99 (Hermetic)

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.



Pin numbers shown for reference only. Numbers may not be marked on package.

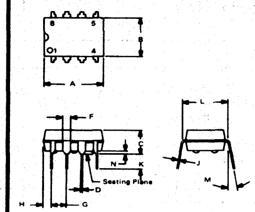
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	-	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

MECHANICAL

"P" PACKAGE — Plastic DIP

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.



Pin numbers shown for reference only. Numbers may not be marked on package.

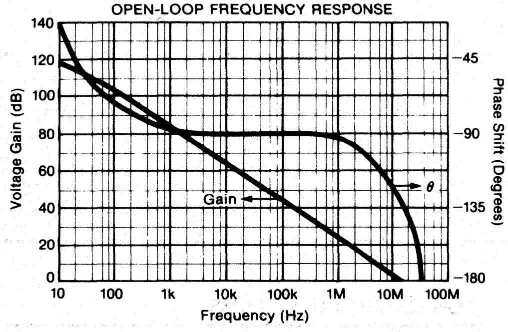
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.370	.400	9.40	10.16
B	.230	.290	5.84	7.37
C	.120	.200	3.05	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.050	0.76	1.27
J	.008	.015	0.20	0.38
K	.070	.135	1.78	3.43
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.010	.030	0.25	0.76

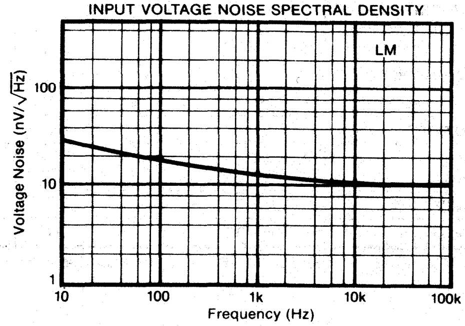
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = \pm15VDC$ unless otherwise noted.

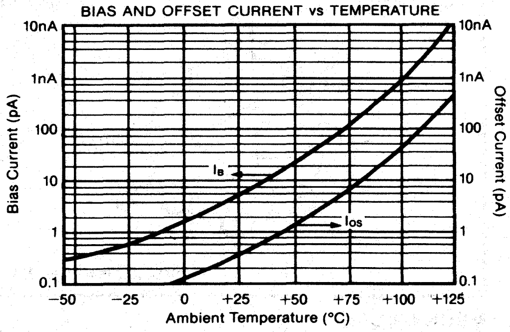
OPEN-LOOP FREQUENCY RESPONSE



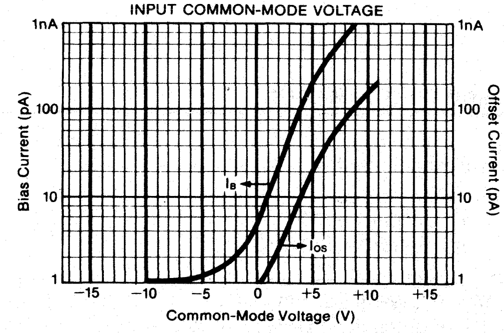
INPUT VOLTAGE NOISE SPECTRAL DENSITY



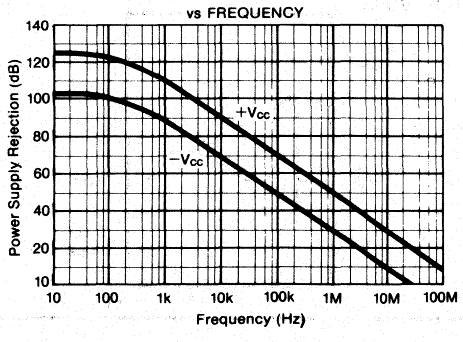
BIAS AND OFFSET CURRENT vs TEMPERATURE



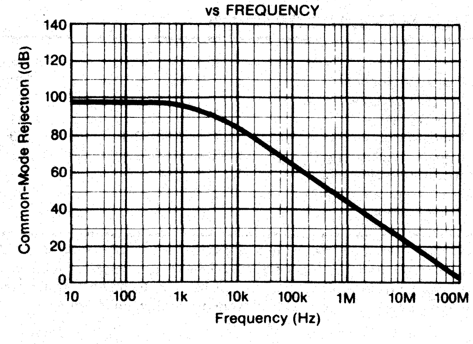
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



POWER SUPPLY REJECTION vs FREQUENCY



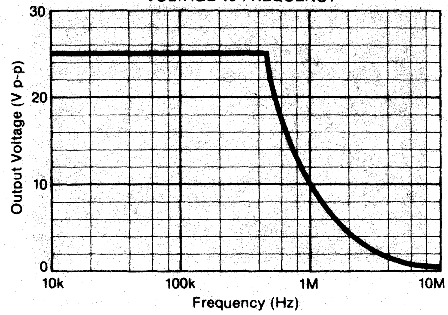
COMMON-MODE REJECTION vs FREQUENCY



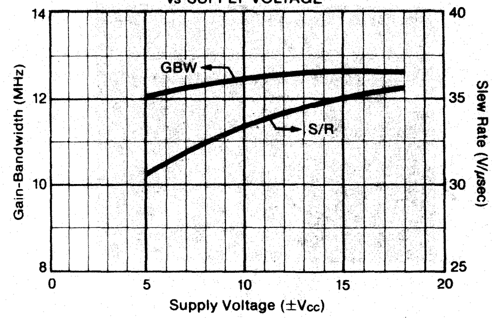
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_{CC} = ±15VDC$ unless otherwise noted.

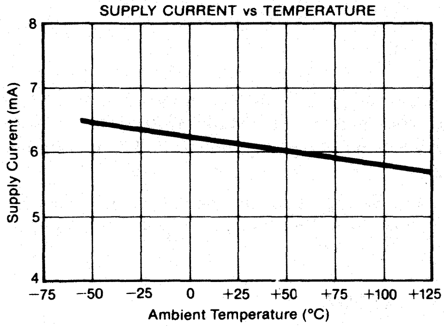
MAXIMUM UNDISTORTED OUTPUT
VOLTAGE vs FREQUENCY



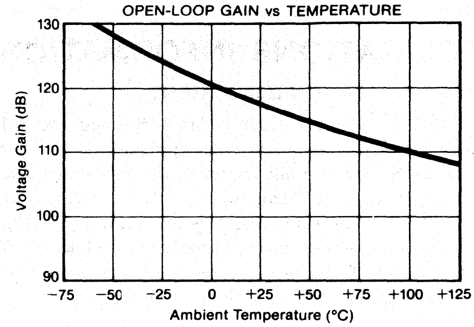
GAIN-BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE



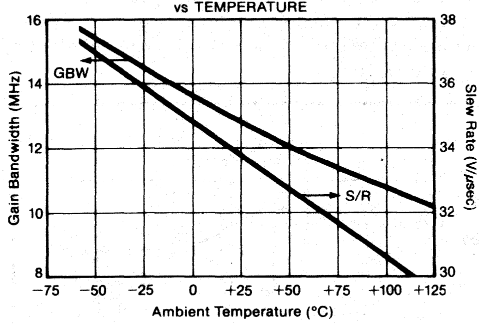
SUPPLY CURRENT vs TEMPERATURE



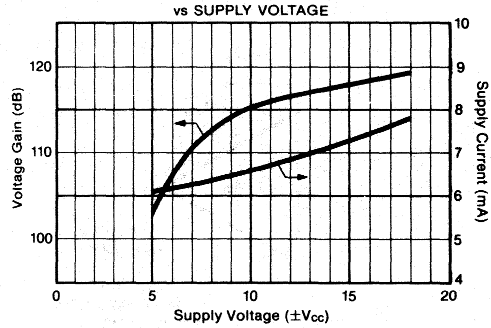
OPEN-LOOP GAIN vs TEMPERATURE



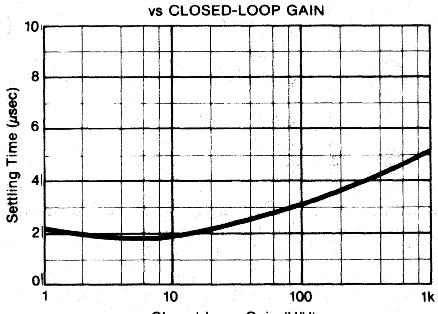
GAIN-BANDWIDTH AND SLEW RATE
vs TEMPERATURE



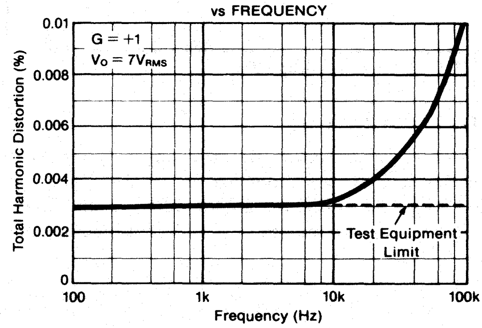
OPEN-LOOP GAIN AND SUPPLY CURRENT
vs SUPPLY VOLTAGE



SETTLING TIME
vs CLOSED-LOOP GAIN

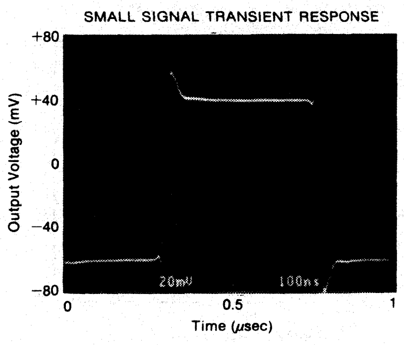


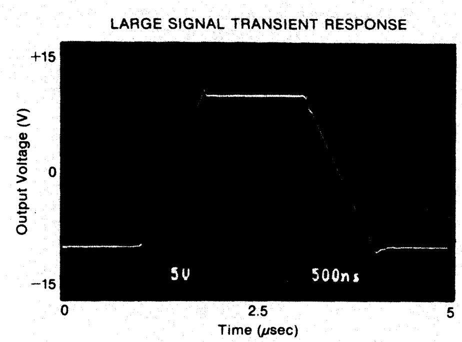
TOTAL HARMONIC DISTORTION
vs FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

$T_a = +25°C$, $V_{CC} = \pm15VDC$ unless otherwise noted.





APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA606 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.5μV/°C for each millivolt of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as LF156 and OP-16. The OPA606 can replace most other amplifiers by leaving the external null circuit unconnected.

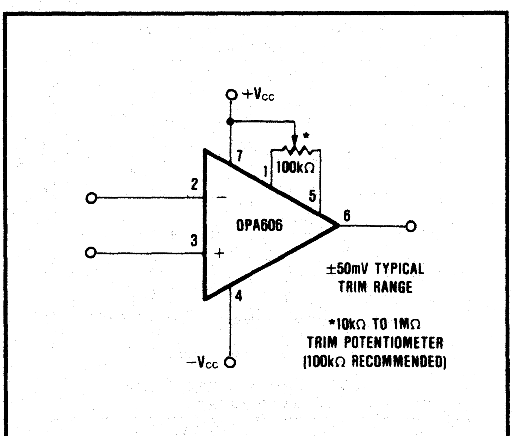


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

If the input voltage exceeds the amplifier's negative supply voltage, input current limiting must be used to prevent damage.

CIRCUIT LAYOUT

Wideband amplifiers require good circuit layout techniques and adequate power supply bypassing. Short, direct connections and good high frequency bypass capacitors (ceramic or tantalum) will help avoid noise pickup or oscillation.

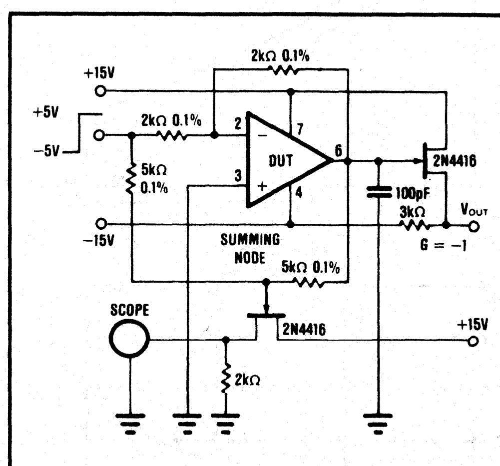


FIGURE 2. Settling Time Test Circuit.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA606. To avoid leakage problems, it is recommended that the signal input lead of the OPA606 be wired to a Teflon® standoff. If the OPA606 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout.

A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 3).

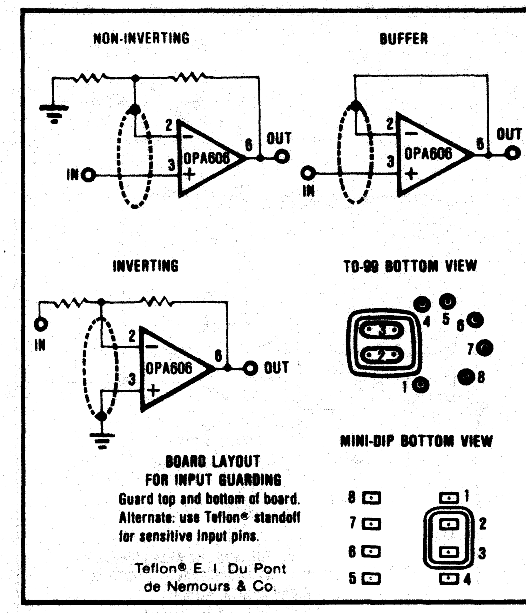


FIGURE 3. Connection of Input Guard.

APPLICATIONS CIRCUITS

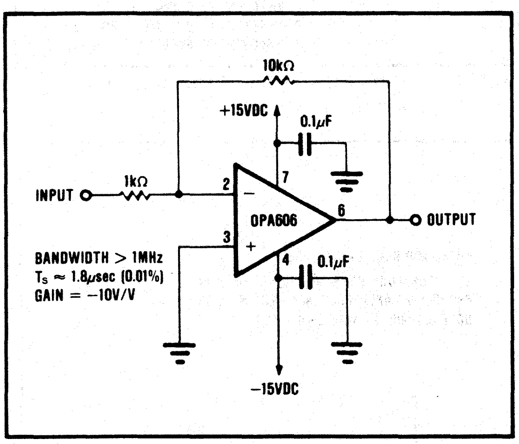


FIGURE 4. Inverting Amplifier.

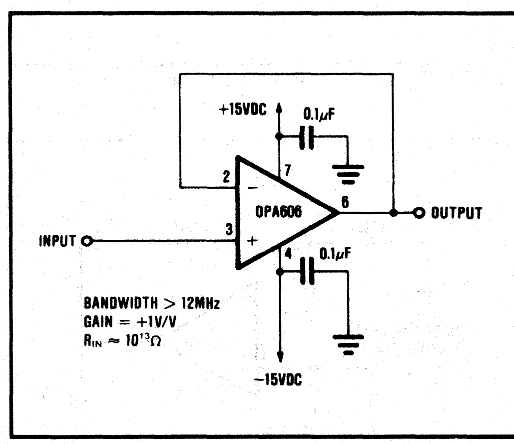


FIGURE 5. Noninverting Buffer.

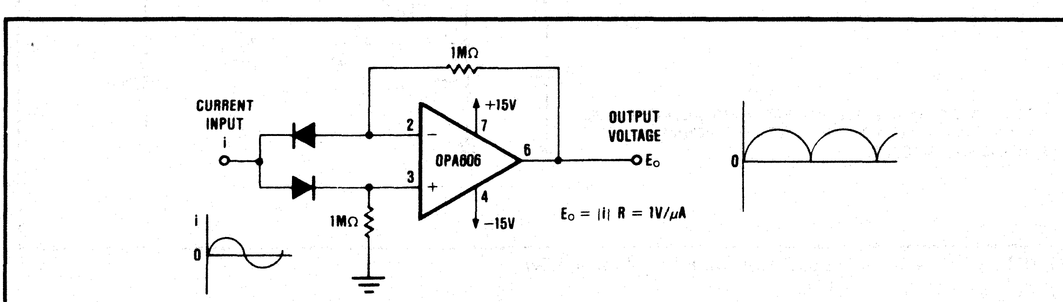


FIGURE 6. Absolute Value Current-to-Voltage Converter.

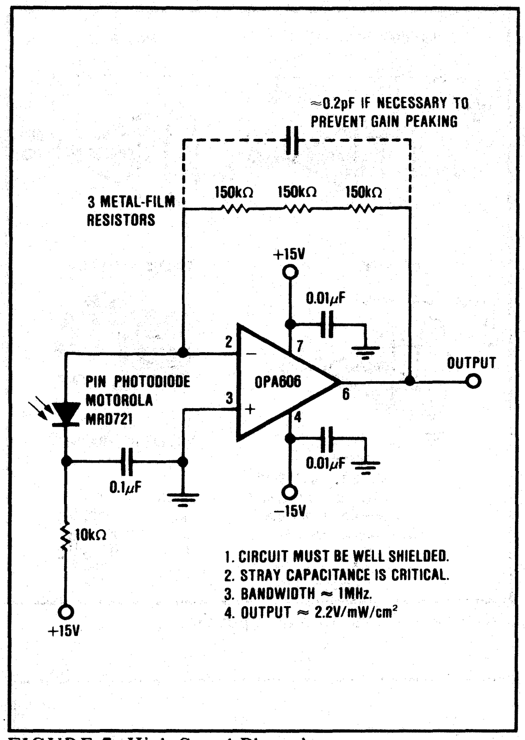


FIGURE 7. High-Speed Photodetector.

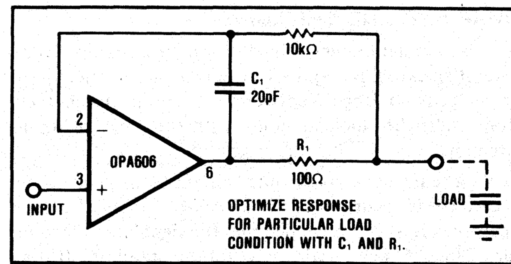


FIGURE 8. Isolating Load Capacitance from Buffer.

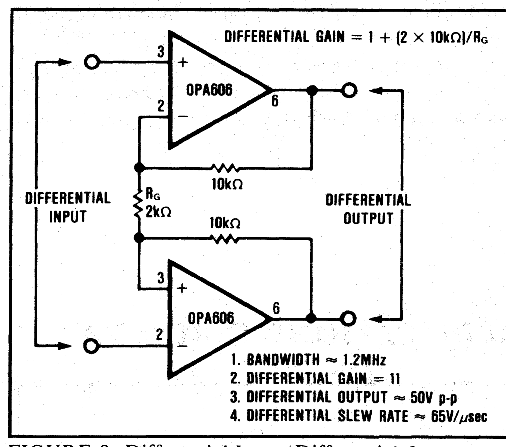


FIGURE 9. Differential Input/Differential Output Amplifier.

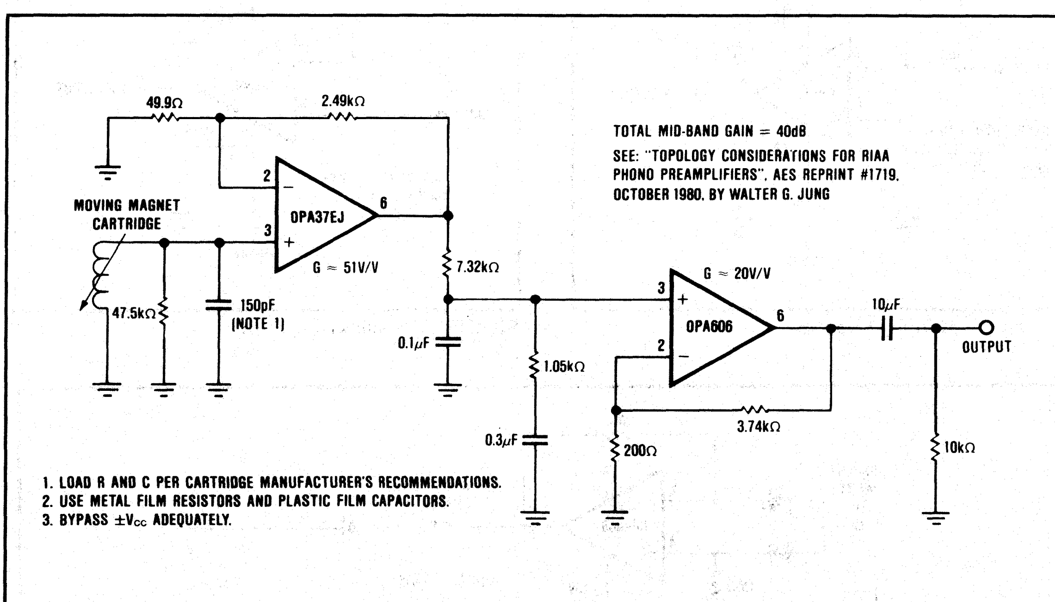
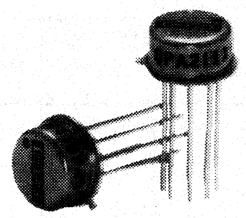


FIGURE 10. Low Noise/Low Distortion RIAA Preamplifier.

BURR-BROWN®

OPA2111



Dual Low Noise Precision *Difet*™ OPERATIONAL AMPLIFIER

FEATURES

- **LOW NOISE: 100% tested: 8nV/$\sqrt{\text{Hz}}$ max at 10kHz**
- **LOW BIAS CURRENT: 4pA max**
- **LOW OFFSET: 500μV max**
- **LOW DRIFT: 2.8μV/°C**
- **HIGH OPEN LOOP GAIN: 114dB min**
- **HIGH COMMON-MODE REJECTION: 96dB min**

APPLICATIONS

- **PRECISION INSTRUMENTATION**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**
- **PROFESSIONAL AUDIO EQUIPMENT**
- **MEDICAL EQUIPMENT**
- **DETECTOR ARRAYS**

DESCRIPTION

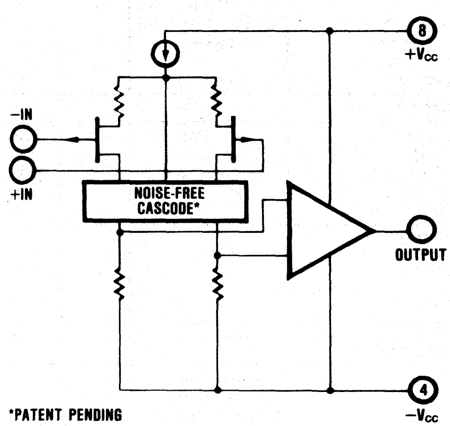
The OPA2111 is a high precision monolithic *Difet*™ (dielectrically-isolated FET) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patent pending). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard dual op-amp pin configuration allows upgrading of existing designs to higher performance levels.



*PATENT PENDING

OPA2111 SIMPLIFIED CIRCUIT (EACH AMPLIFIER)

BIFET® National Semiconductor Corp., *Difet*™ Burr-Brown Corp.

International Airport Industrial Park · P.O. Box 11400 · Tucson, Arizona 85734 · Tel. (602) 746-1111 · Twx: 910-952-1111 · Cable: BBRCORP · Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA2111AM MIN	OPA2111AM TYP	OPA2111AM MAX	OPA2111BM MIN	OPA2111BM TYP	OPA2111BM MAX	OPA2111SM MIN	OPA2111SM TYP	OPA2111SM MAX	UNITS
INPUT											
NOISE											
Voltage, f_o = 10Hz	100% tested		40	80		30	60		40	80	nV/√Hz
f_o = 100Hz	100% tested		15	40		11	30		15	40	nV/√Hz
f_o = 1kHz	100% tested		8	15		7	12		8	15	nV/√Hz
f_o = 10kHz	100% tested		6	8		6	8		6	8	nV/√Hz
f_B = 10Hz to 10kHz	100% tested		0.7	1.2		0.6	1.0		0.7	1.2	µV, rms
f_B = 0.1Hz to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3	µV, p-p
Current, f_B = 0.1Hz to 10Hz	(1)		15	24		12	19		15	24	fA, p-p
f_o = 0.1Hz thru 20kHz	(1)		0.8	1.3		0.6	1.0		0.8	1.0	fA/√Hz
OFFSET VOLTAGE(2)											
Input Offset Voltage	V_{CM} = 0VDC		±0.1	±0.75		±0.05	±0.5		±0.1	±0.75	mV
Average Drift	T_A = T_{MIN} to T_{MAX}		±2	±6		±0.5	±2.8		±2	±6	µV/°C
Match			1			0.5			2		µV/°C
Supply Rejection		90	110		96	110		90	110		dB
			±3	±31		±3	±16		±3	±31	µV/V
Channel Separation	100Hz, R_L = 2kΩ		136			136			136		dB
BIAS CURRENT(2)											
Initial Bias Current	V_{CM} = 0VDC		±2	±8		±1.2	±4		±2	±8	pA
Match			1			0.5			1		pA
OFFSET CURRENT(2)											
Input Offset Current	V_{CM} = 0VDC		±1.2	±6		±0.6	±3		±1.2	±6	pA
IMPEDANCE											
Differential			10^{13} ‖ 1			10^{13} ‖ 1			10^{13} ‖ 1		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			10^{14} ‖ 3			10^{14} ‖ 3		Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		96	110		90	110		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	110	125		114	125		110	125		dB
Match			3			2			3		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			2			2			2		MHz
Full Power Response	20V p-p, R_L = 2kΩ	16	32		16	32		16	32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	2		1	2		1	2		V/µsec
Settling Time, 0.1%	Gain = −1, R_L = 2kΩ		6			6			6		µsec
0.01%	10V step		10			10			10		µsec
Overload Recovery, 50% Overdrive(3)	Gain = −1		5			5			5		µsec
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10	±11		±10	±11		±10	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		5	7		5	7		5	7	mA
TEMPERATURE RANGE											
Specification	Ambient temp.	−25		+85	−25		+85	−55		+125	°C
Operating	Ambient temp.	−55		+125	−55		+125	−55		+125	°C
Storage	Ambient temp.	−65		+150	−65		+150	−65		+150	°C
θ Junction-Ambient			200			200			200		°C/W

NOTES: (1) Sample tested—parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm15VDC$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA2111AM			OPA2111BM			OPA2111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range	Ambient temp.	−25		+85	−25		+85	−55		+125	°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±0.22	±1.2		±0.08	±0.75		±0.3	±1.5	mV
Average Drift			±2	±6		±0.5	±2.8		±2	±6	μV/°C
Match			1			0.5			2		μV/°C
Supply Rejection		86	100		90	100		86	100		dB
			±10	±50		±10	±32		±10	±50	μV/V
BIAS CURRENT[1]											
Initial Bias Current	V_{CM} = 0VDC		±125	±1nA		±75	±500		±2.0nA	±16.3nA	pA
Match			60			30			1nA		pA
OFFSET CURRENT[1]											
Input Offset Current	V_{CM} = 0VDC		±75	±750		±38	±375		±1.3nA	±12nA	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	120		110	120		106	120		dB
Match			5			3			5		dB
RATED OUTPUT											
Voltage Output	$R_L = 2k\Omega$	±10	±11		±10	±11		±10	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		10	40		mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		5	8		5	8		5	8	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[2]	Continuous
Junction Temperature	+175°C

NOTES:

(1) Packages must be derated based on $\theta_{JC} = 150°C/W$ or $\theta_{JA} = 200°C/W$.

(2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

OPA2111 X M

Basic model number

Performance grade

A, B = −25°C to +85°C

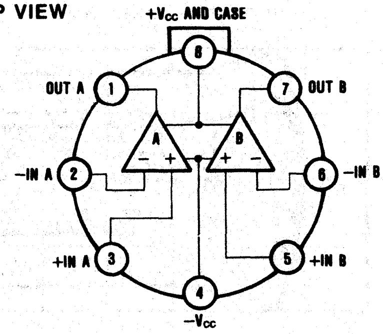
S = −55°C to +125°C

Package code

M = TO-99 metal can

CONNECTION DIAGRAM

TOP VIEW

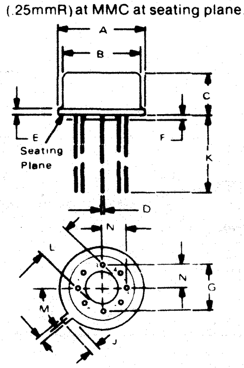


MECHANICAL "M" PACKAGE TO-99 (Hermetic)

NOTE:
Leads in true position within .010" (.25mmR) at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

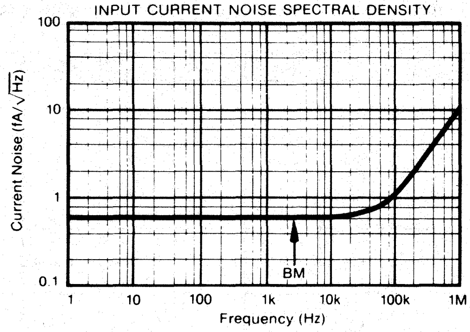


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8.51	9.40
B	305	335	7.75	8.51
C	165	185	4.19	4.70
D	016	021	0.41	0.53
E	010	040	0.25	1.02
F	010	040	0.25	1.02
G	200 BASIC		5.08 BASIC	
H	028	034	0.71	0.86
J	029	045	0.74	1.14
K	500		12.7	
L	110	160	2.79	4.06
M	45° BASIC		45° BASIC	
N	095	105	2.41	2.67

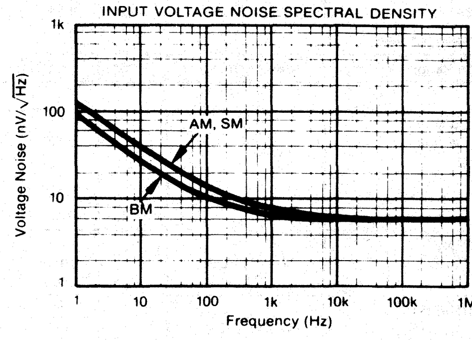
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = \pm15VDC$ unless otherwise noted.

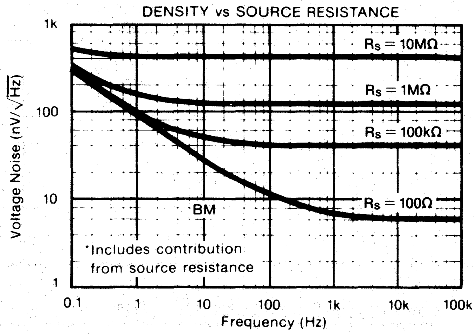
INPUT CURRENT NOISE SPECTRAL DENSITY



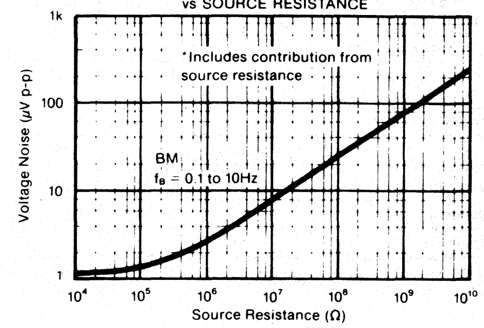
INPUT VOLTAGE NOISE SPECTRAL DENSITY



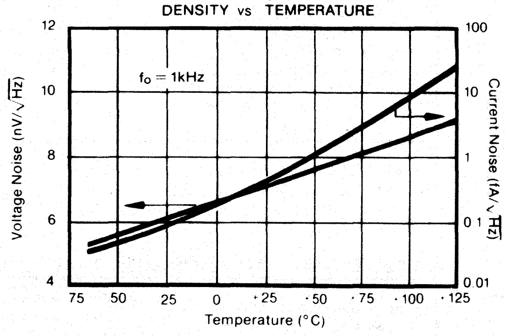
TOTAL* INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



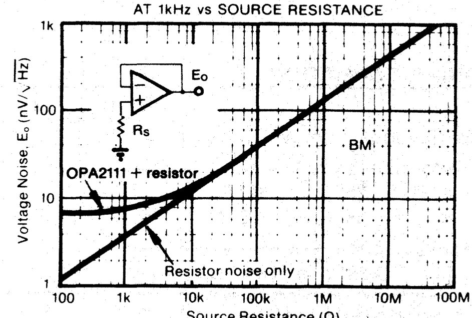
TOTAL* INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



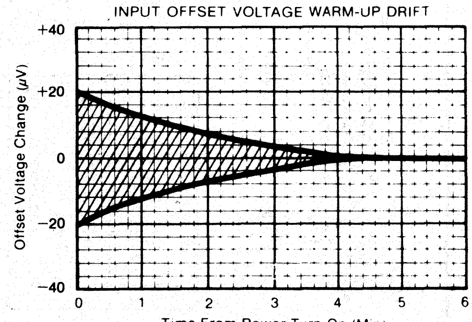
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



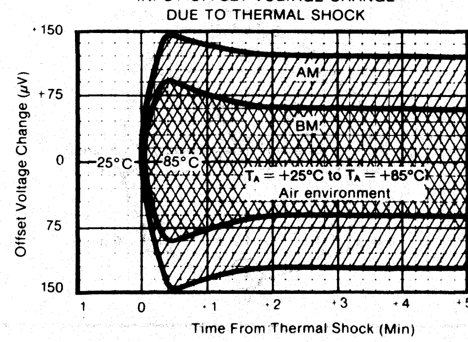
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



INPUT OFFSET VOLTAGE WARM-UP DRIFT



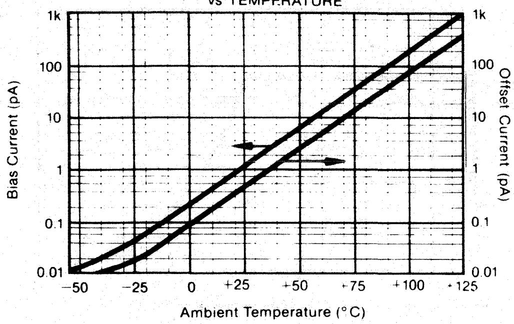
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



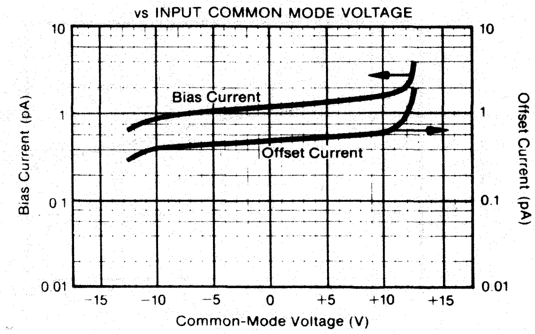
TYPICAL PERFORMANCE CURVES [CONT]

$T_A = +25°C$, $V_{CC} = \pm15VDC$ unless otherwise noted.

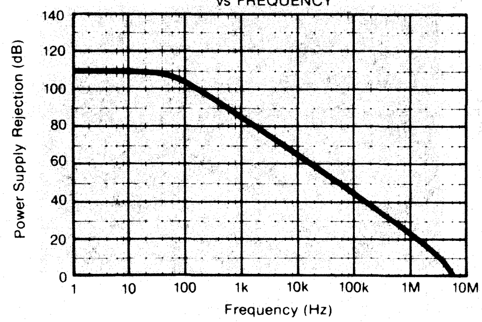
BIAS AND OFFSET CURRENT
vs TEMPERATURE



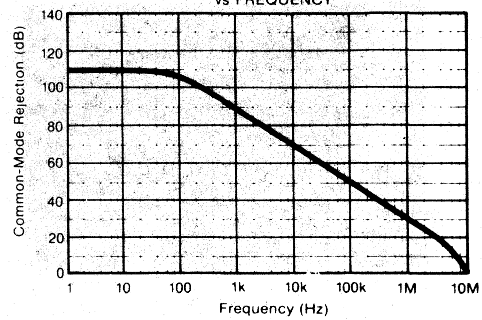
BIAS AND OFFSET CURRENT
vs INPUT COMMON MODE VOLTAGE



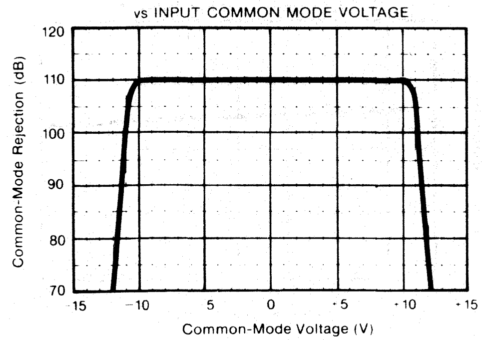
POWER SUPPLY REJECTION
vs FREQUENCY



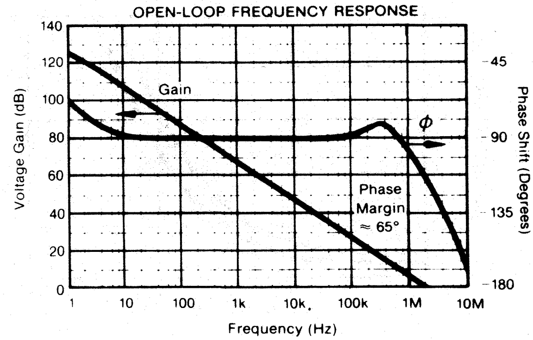
COMMON-MODE REJECTION
vs FREQUENCY



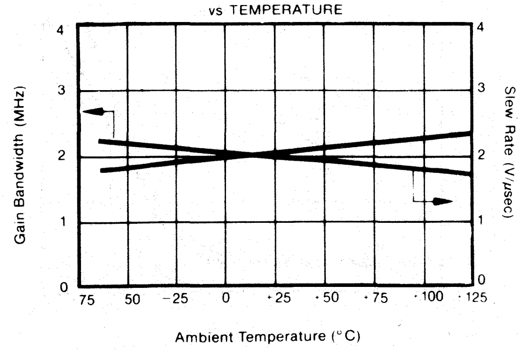
COMMON-MODE REJECTION
vs INPUT COMMON MODE VOLTAGE



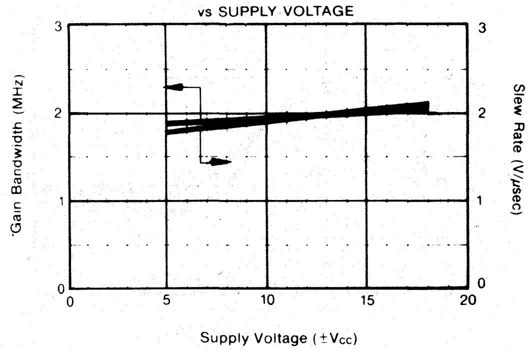
OPEN-LOOP FREQUENCY RESPONSE



GAIN-BANDWIDTH AND SLEW RATE
vs TEMPERATURE



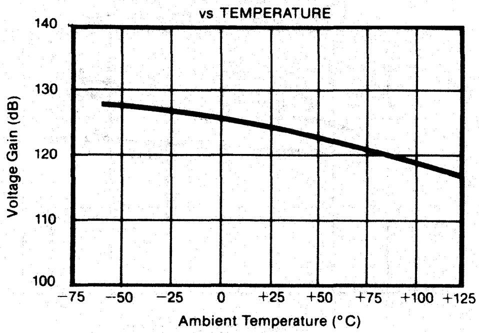
GAIN-BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE



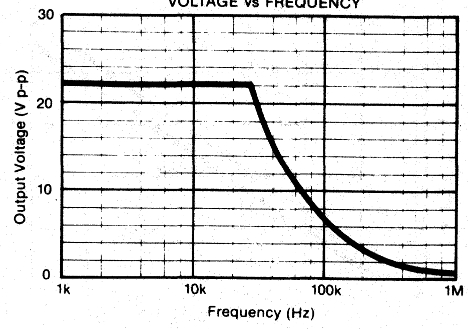
TYPICAL PERFORMANCE CURVES [CONT]

$T_A = +25°C$, $V_{CC} = \pm15VDC$ unless otherwise noted.

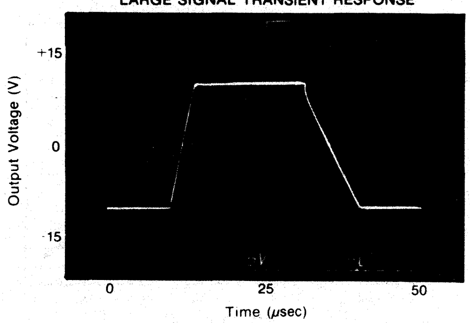
OPEN-LOOP GAIN vs TEMPERATURE



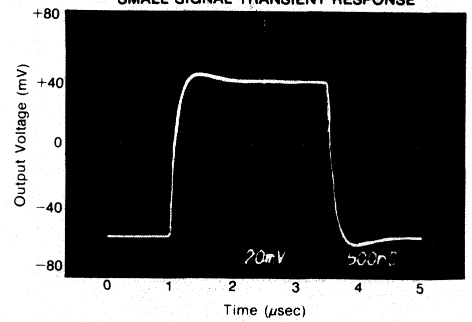
MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY



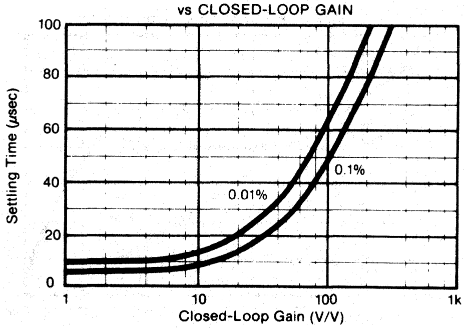
LARGE SIGNAL TRANSIENT RESPONSE



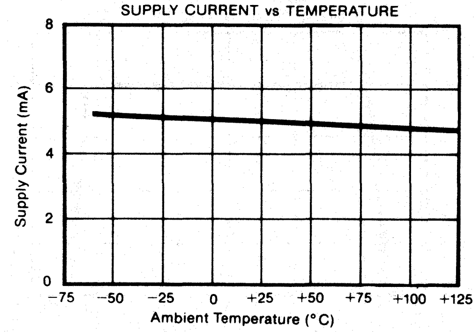
SMALL SIGNAL TRANSIENT RESPONSE



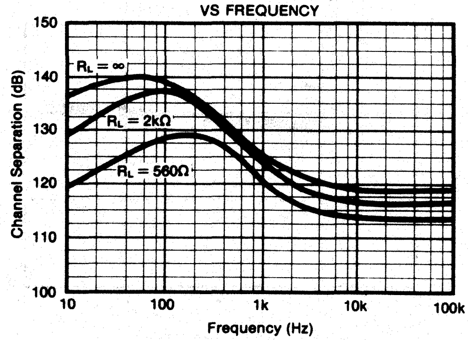
SETTLING TIME vs CLOSED-LOOP GAIN



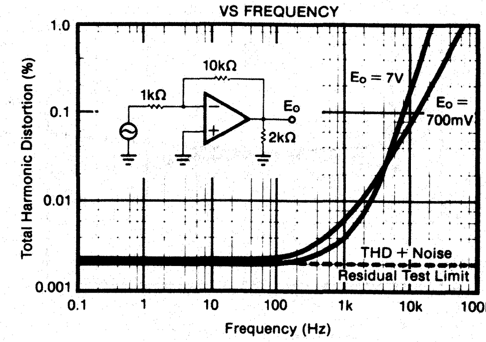
SUPPLY CURRENT vs TEMPERATURE



CHANNEL SEPARATION VS FREQUENCY



TOTAL HARMONIC DISTORTION VS FREQUENCY



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA2111 offset voltage is laser-trimmed and will require no further trim for most applications.

Offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

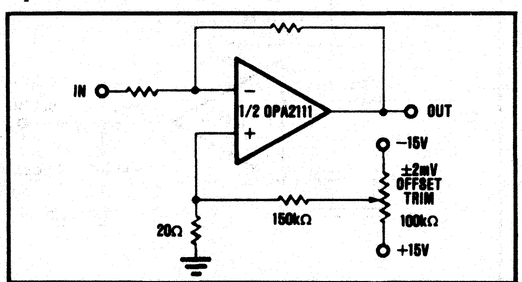


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET® amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA2111. Of course, the differential and common-mode voltage limits should be observed.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA2111. To avoid leakage problems, it is recommended that the signal input lead of the OPA2111 be wired to a Teflon standoff. If the OPA2111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 2).

NOISE: FET VERSUS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the low voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the OPA2111 will have lower total noise than an OP-27 (see Figure 3).

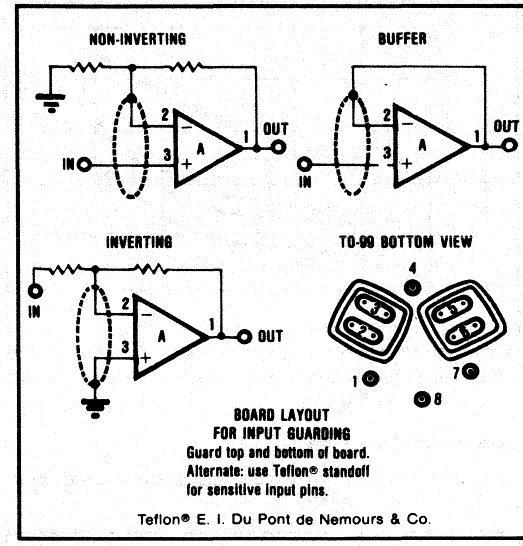


FIGURE 2. Connection of Input Guard.

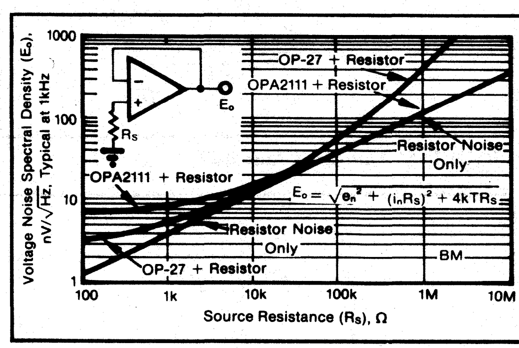


FIGURE 3. Voltage Noise Spectral Density Versus Source Resistance.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET® operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA2111 is not compromised by common-mode voltage.

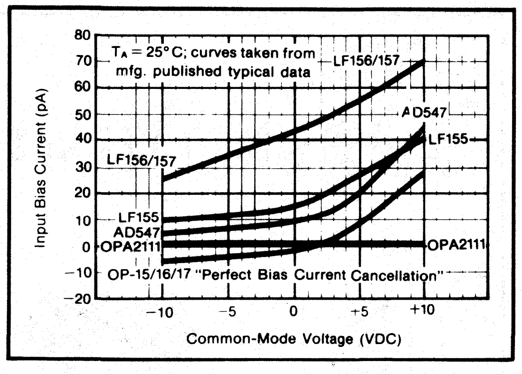


FIGURE 4. Input Bias Current Versus Common-Mode Voltage.

APPLICATIONS CIRCUITS

Figures 5 through 15 are circuit diagrams of various applications for the OPA2111.

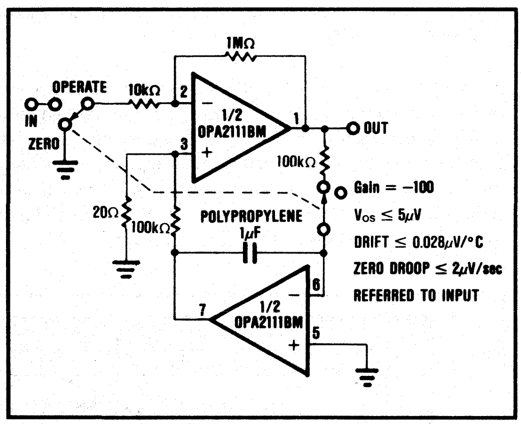


FIGURE 5. Auto-Zero Amplifier.

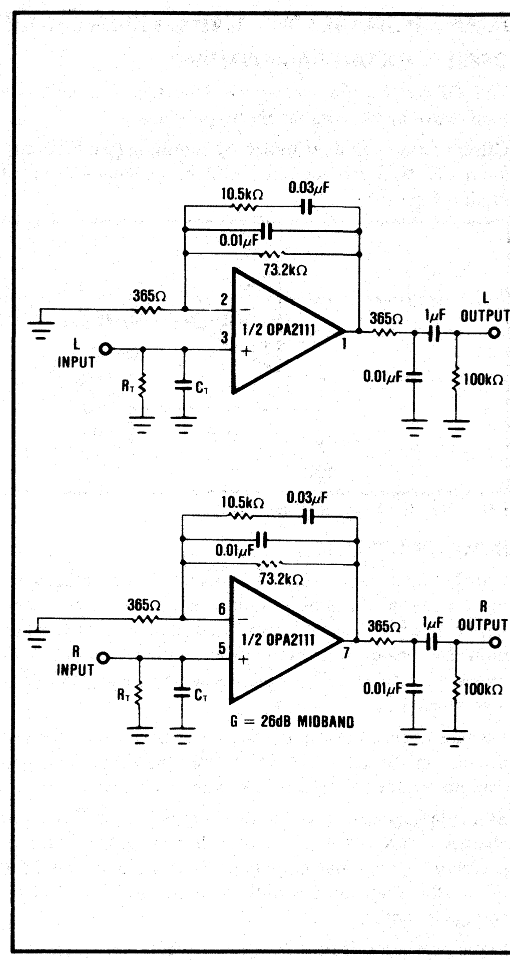


FIGURE 6. RIAA Equalized Stereo Preamplifier.

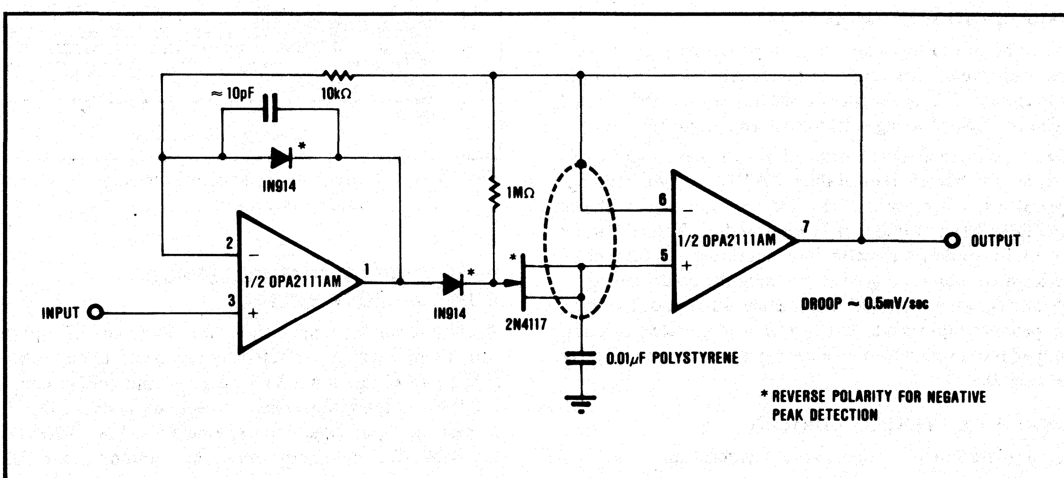


FIGURE 7. Low-Droop Positive Peak Detector.

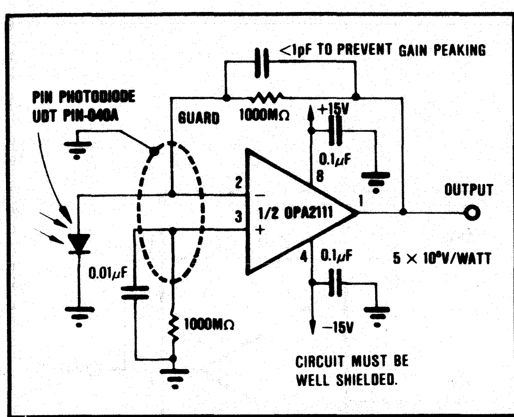


FIGURE 8. Sensitive Photodiode Amplifier.

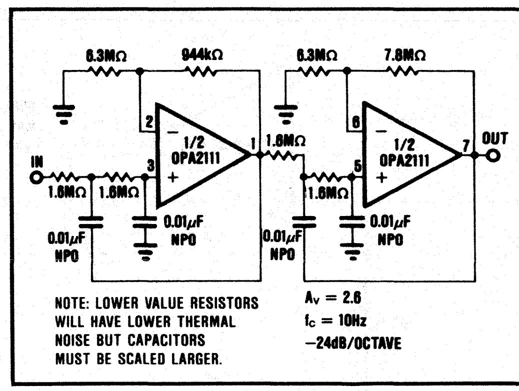


FIGURE 9. 10Hz Fourth-Order Butterworth Low-Pass Filter.

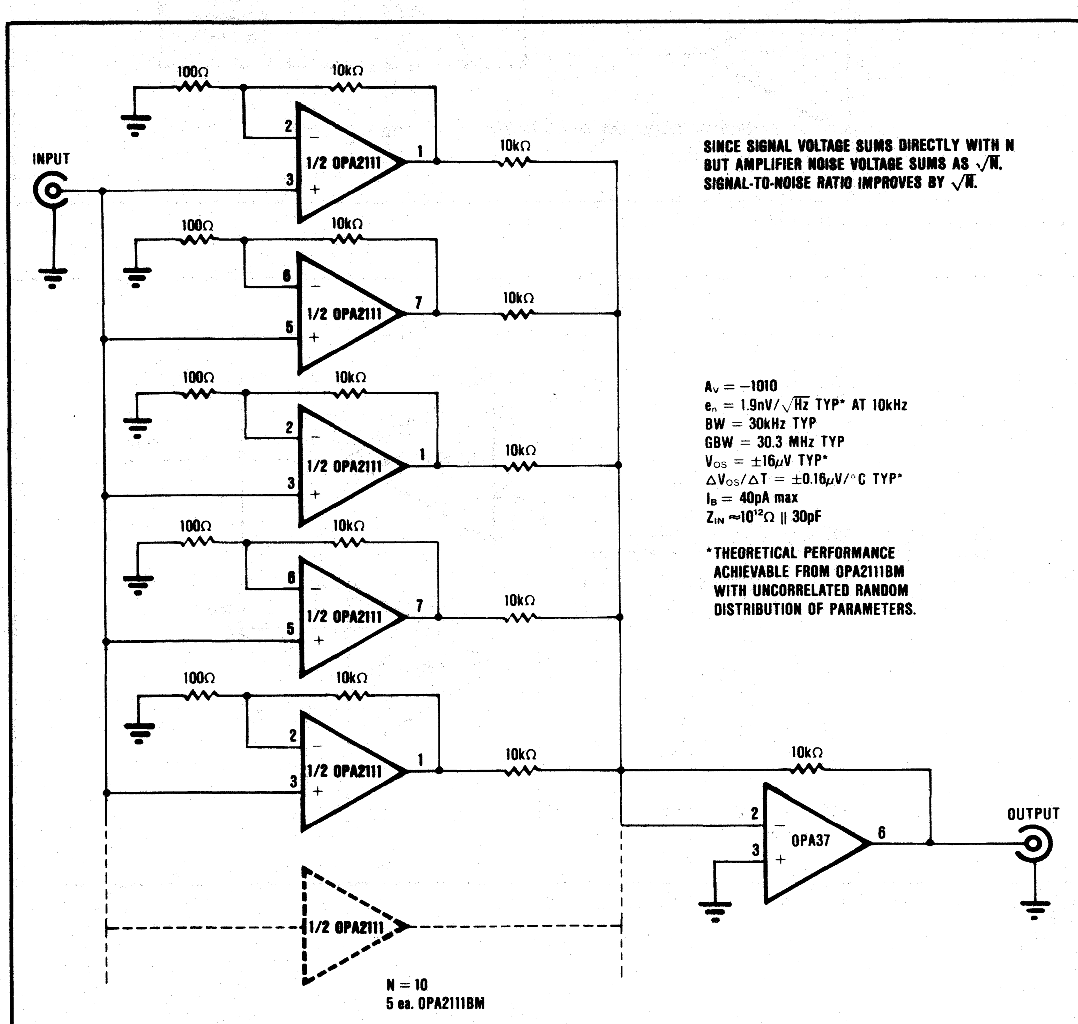


FIGURE 10. ‘N’ Stage Parallel-Input Amplifier.

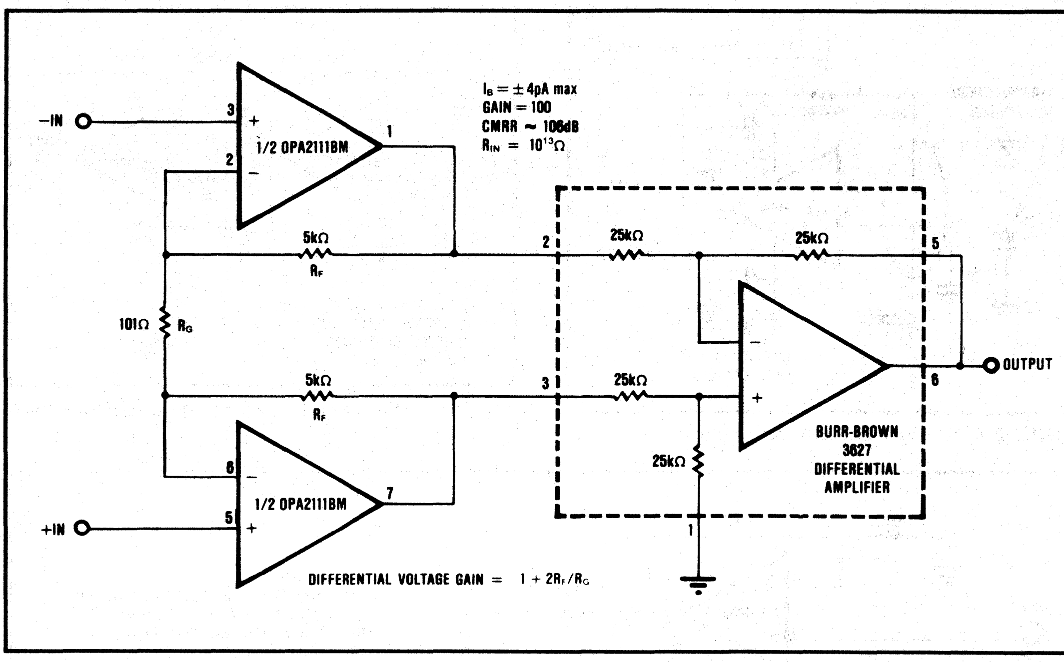


FIGURE 11. FET Input Instrumentation Amplifier.

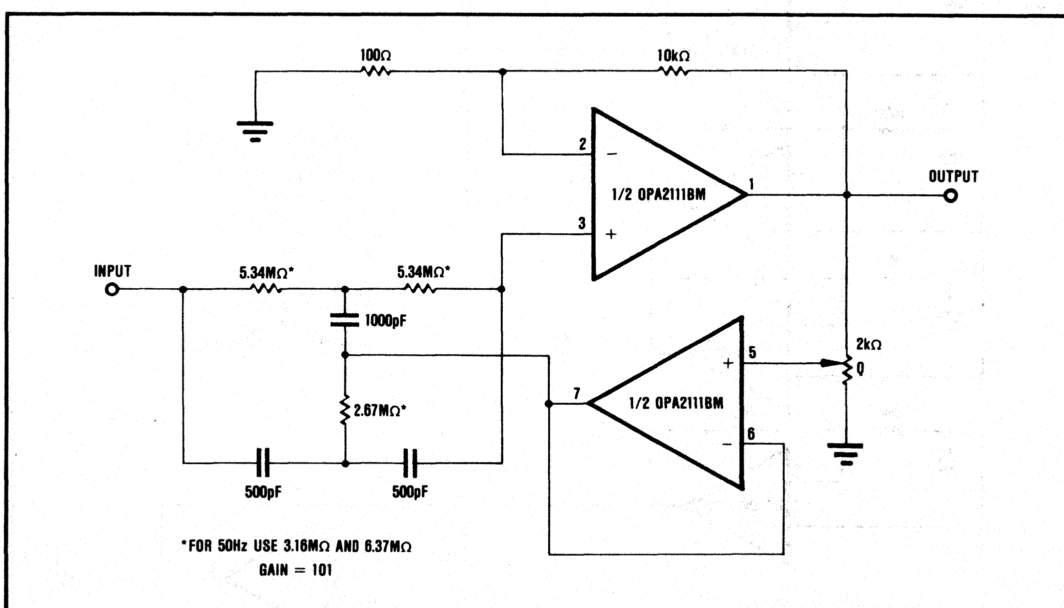
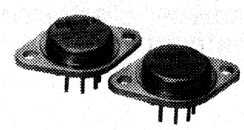


FIGURE 12. High-Impedance 60Hz Reject Filter with Gain.

BURR-BROWN®

OPA8785/883B SERIES

OPA8785VM/883B **OPA8785UM/883B**
OPA8785VM **OPA8785UM**



ADVANCE INFORMATION
Subject to Change

High Current, High Power Military OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE, ±10V to ±40V
- HIGH OUTPUT CURRENT, ±10A Peak
- HIGH OUTPUT POWER, 260W Peak
- LOW DC THERMAL IMPEDANCE: 2.2°C/W
- MIL-STD-883 SCREENING

DESCRIPTION

The OPA8785 is a high power operational amplifier. Its high current output stage delivers ±10A, yet the amplifier is unity-gain stable and it can be used in any operational amplifier configuration. The 260W peak output capability allows the OPA8785 to drive loads (such as motors) with a greater safety margin.

Safe operating area is fully specified and output current limiting is provided to protect both the amplifier and the load from excessive current.

This hybrid IC is housed in an 8-pin hermetic TO-3 package. The electrically-isolated package allows direct mounting to chassis or heat sink without an insulating washer or spacer which would increase thermal resistance.

Two electrical performance grades are available. The premium grade operates from −55°C to +125°C and is designed for military, aerospace, and demanding industrial applications. The U grade has specifications for operation from −25°C to +85°C and from −55°C to +125°C. Applications include test equipment, shipboard, and ground support equipment where operation is normally between −25°C and +85°C and full temperature range operation must be assured.

The OPA8785/883B Series is manufactured on a Hi-Rel manufacturing line with clean room conditions which meet the requirements of MIL-STD-883.

Two product assurance levels are available: Standard and /883B. The Standard product assurance level offers Hi-Rel manufacturing where many MIL-STD-883 screens are performed routinely. The /883B product assurance level, /883B suffix, offers Hi-Rel manufacturing, 100% screening per MIL-STD-883B method 5008 and 10% PDA. Quality assurance further processes /883B devices, by performing group A and B inspections on each inspection lot and group C and D inspections periodically and when specified on the customer's purchase order. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

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DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
HIGH CURRENT-HIGH POWER OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a high current-high power operational amplifier.

1.2 Part Number. The complete part number is as shown below.

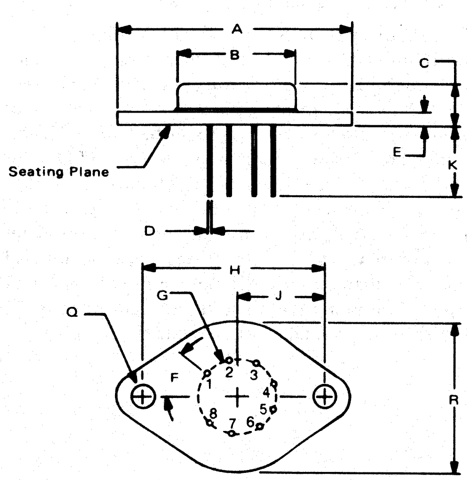
OPA8785	V	M	/883B
Basic model number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel product designator (see 1.2.1)

1.2.1 Device type. The device is a single operational amplifier. Two electrical performance grades are provided. The V grade offers performance specifications over the MIL temperature range (−55°C to +125°C) and the U grade which is specified over the industrial temperature range (−25°C to +85°C). Electrical specifications are shown in Table I and electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the class B product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels available as follows:

Hi-Rel Product Designator	Requirements
/883B	Standard model plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
(none)	Standard model including 100% electrical testing.

1.2.3 Case Outline. The case outline is an 8-pin TO-3 package and is depicted in Figure 1.



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.300	6.60	7.62
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

FIGURE 1. Case Outline (TO-3) Package Configuration.

1.2.4 Absolute maximum ratings.

Supply voltage V_{CC}	±40VDC
Differential input voltage	$\pm V_{CC} - 3$
DC internal power dissipation	80W 1/
AC Internal power dissipation (10kHz, 50% duty cycle)	160W 1/
Output short circuit duration	Continuous to ground
Storage temperature range	−65°C to +165°C
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_j = 200°C
Common-mode input voltage	$\pm V_{CC}$

1.2.5 Recommended operating conditions.

Supply voltage range	±28 or ±34VDC (see Table I)
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θJ-C
8-lead TO-3	Figure 1	80W with heat sink	2.2°C/W with heat sink

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510—Microcircuits, general specification for.

STANDARD
MILITARY
MIL-STD-883—Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

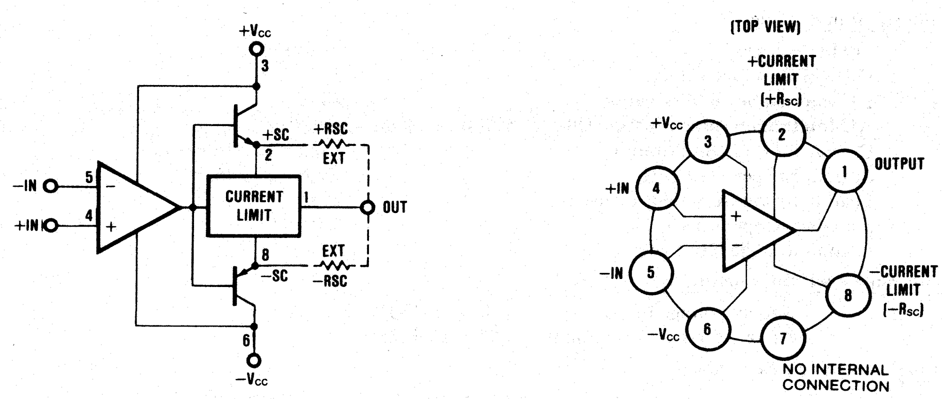
3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. The microcircuit dice are glassivated.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

1/ $T_A \leq +25°C$



(a) Circuit Diagram

(b) Terminal Connections

FIGURE 2. Circuit Diagram and Terminal Connections.

TABLE I. Electrical Performance Characteristics.

All characteristics at $-55°C \leq T_A \leq +125°C$ for OPA8785 "V" grade $V_{CC} = \pm34VDC$; OPA8785 "U" grade $V_{CC} = \pm28VDC$.

CHARACTERISTICS	SYMBOL	CONDITIONS	OPA8785VM/883B OPA8785VM MIN	TYP	MAX	OPA8785UM/883B OPA8785UM MIN	TYP	MAX	UNITS
RATED OUTPUT 1/ 2/									
Output Current	I_O	$R_L = 2\Omega$				±10			A
Continuous 3/		$R_L = 2.6\Omega$	±10						A
Output Voltage 3/	V_O	$I_O = 10A$ peak	±26			±20			V
DYNAMIC RESPONSE									
Bandwidth	BW	Unity Gain-Small Signal $T_A = +25°C$		1			*		MHz
Bandwidth	BW	Full Power $V_O = 40Vp\text{-}p$, $R_L = 8\Omega$,							
		$T_A = +25°C$	10			*			kHz
Slew Rate	SR	$R_L = 5\Omega$				1.5			V/μsec
		$R_L = 6.5\Omega$	1.5						V/μsec
INPUT OFFSET VOLTAGE									
Initial Offset	V_{IO}	$T_A = +25°C$			±5			±10	mV
Tempco	DV_{IO}	$[V_{IO}(T_A) - V_{IO}(+25°C)] \div \Delta T$							
		$-55 \leq T_A \leq +125°C$			±40				μV/°C
		$-25 \leq T_A \leq +85°C$						±65	μV/°C
Vs Supply Voltage	PSRR	$V_{CC} = \pm10$, $V_{CC} = \pm40$			±200				μV/V
		$V_{CC} = \pm10$, $V_{CC} = \pm36$					±200		μV/V
INPUT BIAS CURRENT									
Initial	I_{IB}	$T_A = +25°C$			+20			+40	nA
Tempco	I_{IB}	$-55 \leq T_A \leq +125°C$			±35				nA
		$-25 \leq T_A \leq +85°C$						±35	nA
Vs Supply				±0.02			±0.02		nA/V
INPUT DIFFERENCE CURRENT									
Initial	I_{OS}	$T_A = +25°C$			±3			±10	nA
Tempco	I_{OS}	$-55 \leq T_A \leq +125°C$			±7				nA
		$-25 \leq T_A \leq +85°C$						±7	nA
OPEN LOOP GAIN, DC	A_{VS}	$R_L = 6.5\Omega$	98						dB
		$R_L = 5\Omega$				94			dB
INPUT IMPEDANCE	Z_{ID}			10			*		MΩ
	Z_{ICM}			250			*		MΩ

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	SYMBOL	CONDITIONS	OPA8785VM/883B OPA8785VM MIN	TYP	MAX	OPA8785UM/883B OPA8785UM MIN	TYP	MAX	UNITS
INPUT NOISE									
Voltage Noise	e_n	f_n = 0.3Hz to 10Hz		3			*		μV, p-p
		f_n = 10Hz to 10kHz		5			*		μV, rms
Current Noise	i_n	f_n = 0.3Hz to 10Hz		20			*		pA, p-p
		f_n = 10Hz to 10kHz		4.5			*		pA, rms
INPUT VOLTAGE RANGE									
Common-mode 4/	V_{ICM}	Linear Operation	±(|V_{CC}| − 6)			*			V
Common-mode Rejection	CMRR	F = DC, V_{ICM} = ±(|V_{CC}|−6)	80			70			dB
POWER SUPPLY									
Rated Voltage	V_{CC}			±34			±28		V
Operating Voltage Range			±10		±40	*		±36	V
Current, Quiescent	I_Q				±10			*	mA
TEMPERATURE RANGE									
Specification			−55		+125	−25		+85	°C
Storage			−65		+150	*		*	°C

*Specification same as OPA8785 "V" grade.

NOTES:

1/ Package must be derated based on a junction-to-case thermal resistance of 2.2°C/W or a junction to ambient thermal resistance of 30°C/W.

2/ Safe Operating Area and Power Derating Curves must be observed.

3/ With ±R_{SC} = 0. Peak output current is typically greater than 10A if duty cycle and pulse width limitations are observed. Output current greater than 10A is not guaranteed.

4/ The absolute maximum voltage is 3V less than supply voltage.

3.4 Electrical test requirements. Electrical test requirements are shown in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.

TABLE II. Electrical Test Requirements.

MIL-STD-883 REQUIREMENTS (Hybrid Class)	MODELS OPA8785VM/883B	OPA8785VM	OPA8785UM/883B	OPA8785UM
Interim electrical parameters (preburn-in) (method 5008)	1	1	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7	1, 2U, 3U, 4, 5U, 6U, 7	1, 2U, 3U, 4, 5U, 6U, 7
Group A test requirements (method 5008)	1, 2, 3, 4, 5, 6, 7	—	1, 2U, 3U, 4, 5U, 6U, 7	—
Group C end point electrical parameters (method 5008)	Table IV limits and delta limits	—	—	—

*PDA applies to subgroup 1 for /MIL Hi-Rel designator (see 4.3c)

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS For: OPA8785 "V" grade V_{CC} = ±34VDC OPA8785 "U" grade V_{CC} = ±28VDC unless otherwise specified	LIMITS OPA8785VM/883 OPA8785VM MIN	MAX	OPA8785UM/883 OPA8785UM MIN	MAX	UNITS
1	V_{IO}	4001		−5	+5	−10	+10	mV
T_A = +25°C	I_{IB+}	4001		−20	+20	−40	+40	nA
	I_{IB-}	4001		−20	+20	−40	+40	nA
	I_{IO}	4001		−3	+3	−10	+10	nA
	+PSRR	4003	−V_{CC} = −34, +V_{CC} = +10 to + 40VDC	−200	+200			μV/V
	+PSRR	4003	−V_{CC} = −28VDC, +V_{CC} = +10 to +36VDC			−200	+200	μV/V
	−PSRR	4003	+V_{CC} = +34VDC, −V_{CC} = −10 to −40VDC	−200	+200			μV/V
	−PSRR	4003	+V_{CC} = +28VDC, −V_{CC} = −10 to −36VDC			−200	+200	μV/V
	CMRR	4003	V_{CM} = ±30V, f = DC	80				dB
	CMRR	4003	V_{CM} = ±22V, f = DC			70		dB
	I_{CC+}	4005	V_{CM} = 0, no load condition		+10		+10	mA
	I_{CC-}	4005	V_{CM} = 0, no load condition	−10		−10		mA

TABLE III. Group A Inspection (cont).

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS (For: OPA8785 "V" grade V_{CC} = ±34VDC; OPA8785 "U" grade V_{CC} = ±28VDC unless otherwise specified)	LIMITS OPA8785VM/883 OPA8785VM		LIMITS OPA8785UM/883 OPA8785UM		UNITS
				MIN	MAX	MIN	MAX	
2	DV_{IO}	4001	[V_{IO} (+125°C) − V_{IO} (+25°C)] ÷ 100	−40	+40			μV/°C
T_A = +125°C	I_{IB+}	4001		−35	+35			nA
	I_{IB-}	4001		−35	+35			nA
	I_{IO}	4001		−7	+7			nA
	+PSRR	4003	$-V_{CC}$ = −34VDC, $+V_{CC}$ = 10 to 40VDC		±200			μV/V
	−PSRR	4003	$+V_{CC}$ = +34VDC, $-V_{CC}$ = −10 to −40VDC		±200			μV/V
	CMRR	4003	V_{CM} = ±30V, f = DC	80				dB
	I_{CC+}	4005	V_{CM} = 0, no load condition		+10			mA
	I_{CC-}	4005	V_{CM} = 0, no load condition	−10				mA
2U	DV_{IO}	4001	[V_{IO} (+85°C) − V_{IO} (+25°C)] ÷ 60			−65	+65	μV/°C
T_A = +85°C	I_{IB+}	4001				−35	+35	nA
	I_{IB-}	4001				−35	+35	nA
	I_{IO}	4001				−7	+7	nA
	+PSRR	4003	$-V_{CC}$ = −28VDC, $+V_{CC}$ = 10 to 36VDC			−200	+200	μV/V
	−PSRR	4003	$+V_{CC}$ = +28VDC, $-V_{CC}$ = −10 to −36VDC			−200	+200	μV/V
	CMRR	4003	V_{CM} = ±22VDC, f = DC			70		dB
	I_{CC+}	4005	V_{CM} = 0, no load condition				+10	mA
	I_{CC-}	4005	V_{CM} = 0, no load condition			−10		mA
3	DV_{IO}	4001	[V_{IO} (+25°C) − V_{IO} (−55°C)] ÷ 80	−40	+40			μV/°C
T_A = −55°C	I_{IB+}	4001		−35	+35			nA
	I_{IB-}	4001		−35	+35			nA
	I_{IO}	4001		−7	+7			nA
	+PSRR	4003	$-V_{CC}$ = −34VDC, $+V_{CC}$ = 10 to +40VDC	−200	+200			μV/V
	−PSRR	4003	$+V_{CC}$ = +34VDC, $-V_{CC}$ = −10 to −40VDC	−200	+200			μV/V
	CMRR	4003	V_{CM} = ±30V, f = DC	80				dB
	I_{CC+}	4005	V_{CM} = 0, no load condition		+10			mA
	I_{CC-}	4005	V_{CM} = 0, no load condition	−10				mA
3U	DV_{IO}	4001	[V_{IO} (+25°C) − V_{IO} (−25°C)] ÷ 50			−65	+65	μV/°C
T_A = −25°C	I_{IB+}	4001				−35	+35	nA
	I_{IB-}	4001				−35	+35	nA
	I_{IO}	4001				−7	+7	nA
	+PSRR	4003	$-V_{CC}$ = −28VDC, $+V_{CC}$ = +10 to +36VDC			−200	+200	μV/V
	−PSRR	4003	$+V_{CC}$ = +28VDC, $-V_{CC}$ = −10 to −36VDC			−200	+200	μV/V
	CMRR	4003	V_{CM} = ±22VDC, f = DC			70		dB
	I_{CC+}	4005	V_{CM} = 0, no load condition				+10	mA
	I_{CC-}	4005	V_{CM} = 0, no load condition			−10		mA
4	V_{OP}	4004	I_O = 10A peak, 10kHz sine wave, 1sec duration	−26	+26	−20	+20	V
T_A = +25°C	I_{OP}	4004	R_L = 2.6Ω, 10kHz sine wave, 1sec duration	−10	+10			A
			R_L = 2.0Ω, 10kHz sine wave, 1sec duration			−10	+10	A
	A_{VS}	4004	R_L = 6.5Ω	98				dB
			R_L = 5Ω			94		dB
5	V_{OP}	4004	R_L = 10kΩ	−30	+30			V
T_A = +125°C			R_L = 10kΩ			±24	±24	V
	A_{VS}	4004	R_L = 10kΩ	98				dB
5U	V_{OP}	4004	R_L = 10kΩ			±24	±24	V
T_A = +85°C	A_{VS}	4004	R_L = 5.0Ω			94		dB
6	V_{OP}	4004	R_L = 10kΩ	−30	+30			V
T_A = −55°C	A_{VS}	4004	R_L = 10kΩ	98				dB
6U	V_{OP}	4004	R_L = 10kΩ			±24	±24	V
T_A = −25°C	A_{VS}	4004	R_L = 10kΩ			94		dB
7	SR	4002	R_L = 6.5Ω	1.5				V/μsec
T_A = +25°C			R_L = 5.0Ω			1.5		V/μsec

TABLE IV. Group C End Point Electrical Parameters.

(For OPA8785 V grade V_{CC} = ±34VDC, T_A = +25°C)

TEST	LIMIT	DELTA
V_{IO}	±5mV	±10%
$\pm I_{CC}$	±10mA	±10%

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum:

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin
f. Electrostatic sensitivity identifier (Δ)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /883B product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the /883B product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for /883B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, constant acceleration (condition A), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

For the /883B product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /883B product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening for the /883B Hi-Rel product designation is in accordance with MIL-STD-883, method 5008, class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.
b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 3 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum
c. Percent defective allowable (PDA). The PDA, for /883B product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no

1/ A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in are used to determine the percent defective for each manufacturing lot, and the lot is accepted or rejected based on the PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

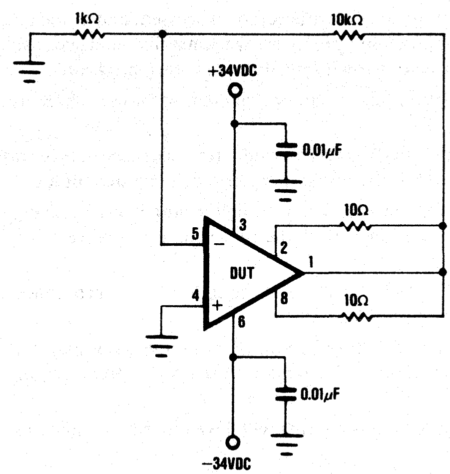


FIGURE 3. Test Circuit—Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, class B, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, class B are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008, class B. A report of the most recent group C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 (class B).

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 (class B), and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 3 herein
   (3) $T_A = +125°C$ minimum
   (4) Test condition is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 (class B) and as follows:

a. End point electrical parameters are specified in Table IV herein.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

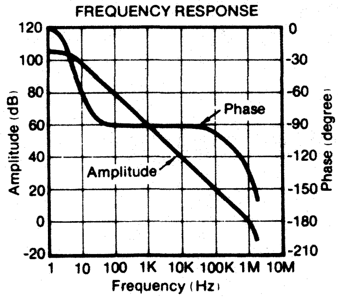
6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group I as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. CAUTION—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

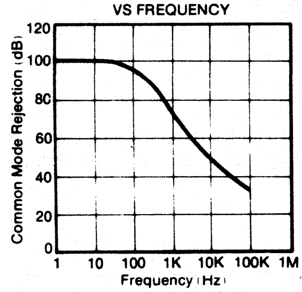
7. ELECTRICAL PERFORMANCE CURVES

(Typical at +25° case and ±Vcc = 28VDC unless otherwise noted.)

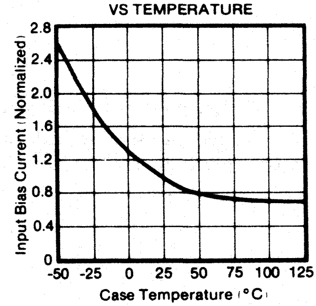
OPEN-LOOP
FREQUENCY RESPONSE



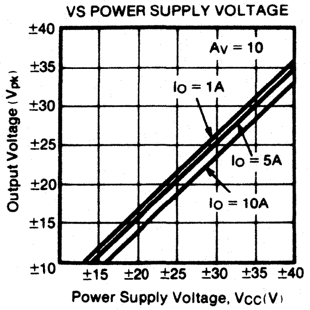
COMMON MODE REJECTION
VS FREQUENCY



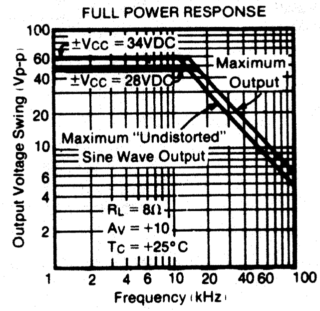
INPUT BIAS CURRENT
VS TEMPERATURE



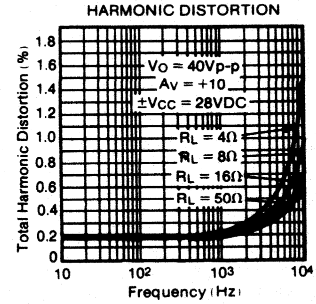
OUTPUT VOLTAGE SWING
VS POWER SUPPLY VOLTAGE

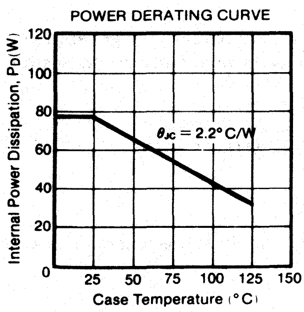


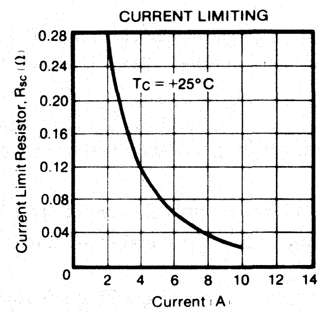
FULL POWER RESPONSE

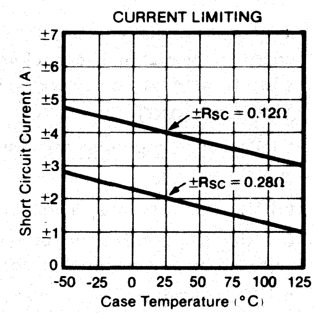


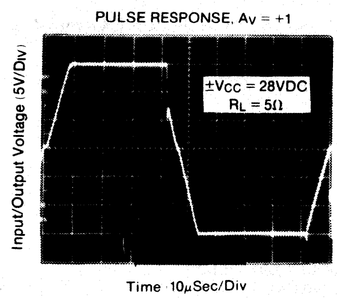
HARMONIC DISTORTION

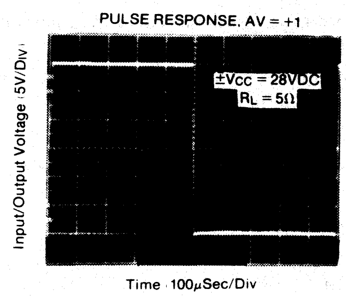












8. APPLICATION INFORMATION

8.1 Grounding. Because of the high output current capability of the OPA8785 Series, the user is cautioned to observe proper grounding techniques. Figure 4 illustrates a recommended technique.

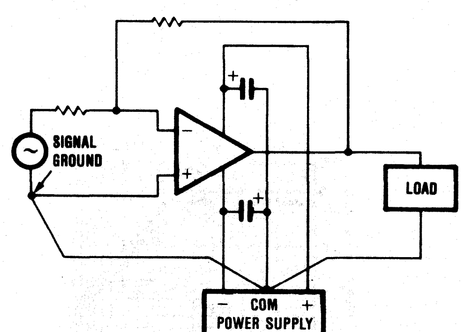


FIGURE 4. Proper Power Supply Connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

8.2 Supply bypassing. The OPA8785 power supplies should be bypassed with 50μF tantalum capacitors connected as close as possible to pins 3 and 6. These bypass capacitors should be connected to the load ground rather than the signal ground.

8.3 Current limits. The OPA8785 amplifier is designed so that both positive and negative load current limits can be set independently with external resistors $+R_{SC}$ and $-R_{SC}$ respectively. The approximate value of these resistors is given by the equation:

$$R_{SC} = [(0.65 \div I_{LIMIT}) - 0.0437] \text{ ohms}$$

I_{LIMIT} is the desired maximum current in amperes. The power dissipation of the current limit resistor is:

$$P_{max} = R_{SC} (I_{LIMIT})^2 \text{ watts}$$

R_{SC} is in ohms and I_{LIMIT} is in amperes.

Current limit resistors carry the full amplifier output current so lead lengths should be minimized. Highly inductive resistors can cause loop instability. Variation in limit with case temperature is shown in the Typical Performance Curves, paragraph 7.

The amplifier should be used with as low a current limit as possible for its particular application. This will minimize the change of damaging the amplifier under abnormal load conditions and will increase reliability by limiting internal power dissipation.

The current limits may be used to generate other functions such as constant current supplies and torque or stall current limits for servomotor applications.

8.4 Heat sinking. The OPA8785 requires a heat sink to limit output transistor junction temperature (T_J) to an absolute maximum of +200°C. The steady-state thermal circuit is illustrated in Figure 5.

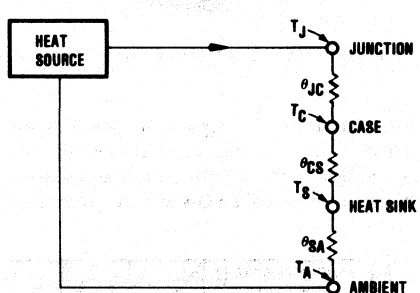


FIGURE 5. Simplified Steady-State Heat Flow Model.

Junction temperature (T_J) is found from the equation:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

where P_D = average amplifier power dissipation (W)
θ_{JC} = junction to case thermal resistance (°C/W)
θ_{CS} = case to sink thermal resistance (°C/W)
θ_{SA} = sink to ambient thermal resistance (°C/W)
T_A = ambient temperature (°C)

For most heat sink calculations the quiescent power dissipation is very low (<1 watt) and can be disregarded with only a small error.

The maximum size heat sink can be found as follows:

Example: Find the maximum thermal resistance (smallest heat sink) that can be used for an OPA8785 with $\pm V_{CC}$ = 28VDC. Output voltage is +10VDC across a 10Ω resistor and ambient temperature is +50°C:

$$\theta_{SA} = [(T_J - T_A) \div PD] - \theta_{CS} - \theta_{JC}$$

As large a heat sink as possible should be used. θ_{CS} depends on the flatness of the heat sink, the thermal compound used, and the roughness of the mating surfaces. Typical values are between 0.1°C/W and 0.3°C/W for a TO-3 package properly mounted on a heat sink.

The OPA8785 mounting flange is electrically-isolated and can be mounted directly to a heat sink without insulating washers or spacers.

The output transistor thermal resistance (θ_{JC}) is a function of the output current pulse width, pulse shape, and duty cycle. Long duration pulses allow the junction temperature to approach its steady state value while shorter pulses cause a lower peak junction temperature due to the junction's thermal time constant. Heat is conducted away from the junction rapidly so that as the duty cycle decreases, junction temperature decreases.

Steady state θ_{JC} is rated at 2.2°C/W maximum. In applications where the amplifier's output current alternates between output transistors—for example, an AC amplifier—the transistor θ_{JC} will depend on frequency as shown in Figure 6.

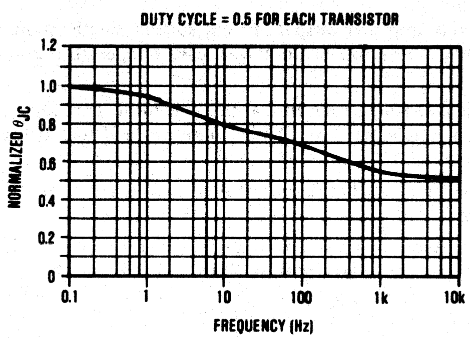


FIGURE 6. Effective θ_{JC} for Applications Where Output Current Alternates Between Output Transistors.

8.5 Safe operating area (SOA). In addition to the limits imposed by power dissipation, the amplifier's output transistors are also limited by a second breakdown region. This occurs because of increased emitter current density due to current crowding at higher operating voltages. Both the dissipation and second breakdown limits depends on time and temperature. Figure 7 shows each output transistor's SOA at a case temperature of +25°C.

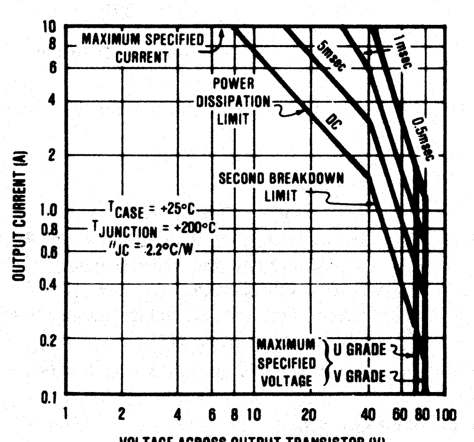


FIGURE 7. Transistor Safe Operating Area at +25° C Case Temperature.

Limits for short pulse widths are substantially greater than for steady state (DC). At a case temperature of +125°C the SOA limits are reduced (see Figure 8). The SOA shown in these curves is based on a conservative linear derating of both the power dissipation and the second breakdown region.

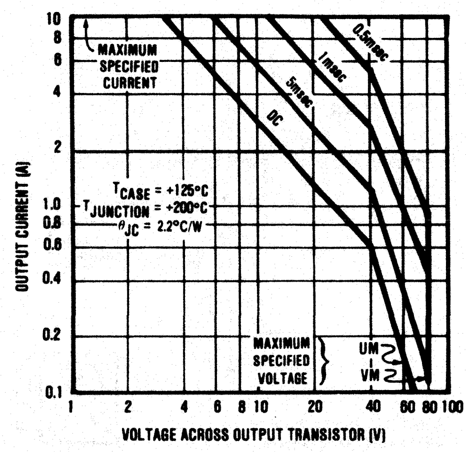


FIGURE 8. Transistor Safe Operating Area at +125°C Case Temperature.

Resistive loads are easy to analyze by simply plotting load lines on the SOA curve. If the curve representing the load line stays within the OPA8785 output transistor's SOA curve and all other parameters are observed, such as case temperature, etc., the amplifier will be safe. The load line can swing through the larger SOA limits if their time duration constraints are strictly observed.

Reactive loads present a more complex problem since the output voltage and current are not in phase. This results in the reactive load line becoming elliptical (when plotted on linear axes) which requires a larger SOA for safe operation.

Although detailed analysis is beyond the scope of this data sheet, the load line can be viewed on an oscilloscope as shown in Figure 9. The X-Y display is driven by the voltage across the load and by the current into the load. This setup can also display voltage and current stress across the OPA8785 output transistors as shown in Figure 10. This data can then be compared to the SOA limits.

The amplifier is designed to operate with electromotive force generating loads such as servomotors, relays, and actuators. Careful attention must be paid to both the load characteristics and the amplifier's SOA to ensure safe operation.

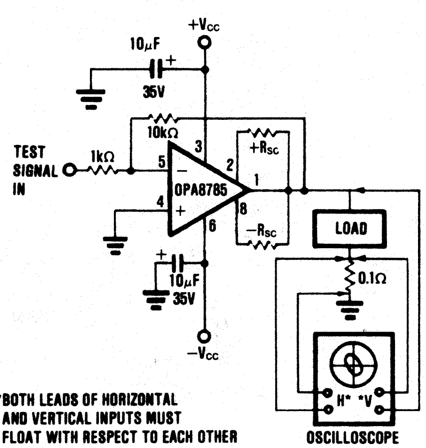


FIGURE 9. Loadline Display.

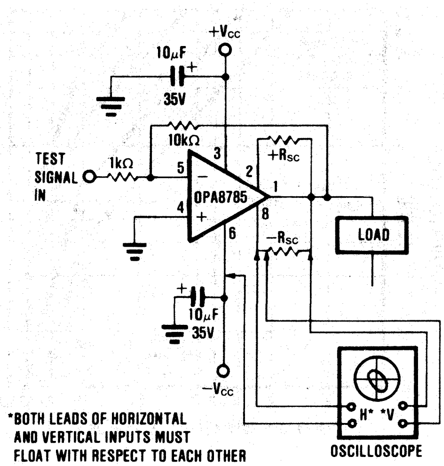


FIGURE 10. Output Transistor Safe Operating Area Stress Display.

Figure 11 shows the OPA8785 configured as a DC permanent magnet motor driver. The armature current (1A) and motor voltage (V_m) are monitored by an oscilloscope in the X-Y mode. Slewing the motor with a 4Hz sine wave results in the motor power ellipse of Figure 12. The input level has been adjusted to give ±20V, peak across the motor. An examination of the power ellipse indicates that the instantaneous power delivered to the motor exceeds the amplifier's output transistors safe operating area at a case temperature of +25°C. The point at which the motor shows 0V at −6.9A is a problem. The voltage across the output is 28V − 0V = 28V. Checking the SOA curve shows that the amplifier can safely withstand this condition for slightly under 5msec. At 4Hz this transient swing outside the DC SOA region is exceeded for much longer than 5msec. Continued operation under these conditions will result in device failure. Peak junction temperatures should not exceed +200°C. Perhaps a motor with a higher impedance winding should be considered for this application. Current limiting and lower supply voltage can also reduce dissipation.

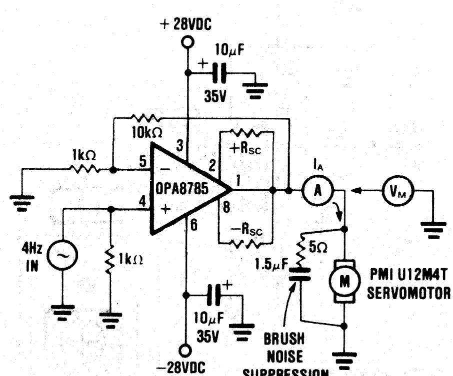


FIGURE 11. Servomotor Amplifier.

Motors used in servo applications often require a surprisingly large current to accelerate quickly. Worst-case conditions occur when the motor is operating at full speed and is suddenly slammed into reverse ("plugging"). This condition is illustrated in Figure 13 when a DC servomotor is driven by a bipolar square wave. As the motor reverses direction a large surge current flows, causing very-high peak power dissipation in the amplifier. After several time constants (determined by the inertia moment) the current drops to a lower steady-state value. Loading the motor increases the motor average power and amplifier dissipation. SOA curves should be checked for safe operation under these surge conditions.

The OPA8785 current limits may be set to clip the high surge currents to a safe level. This is shown in Figure 14. Note that the current limit does limit the servomotor peak acceleration.

Inductive loads should be investigated for high peak transients generated by a collapsing magnetic field. Resistive damping can reduce this problem and although the amplifier has a substrate as part of the Darlington output transistor structure, external diodes are recommended for heavy clamping.

Fast diodes such as those normally used as rectifiers in switching power supplies are suitable.

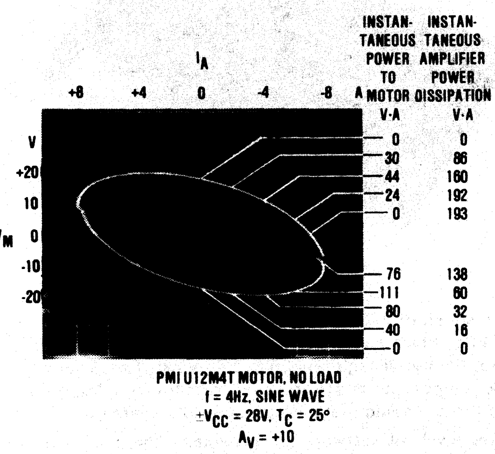


FIGURE 12. DC Servomotor Load Line.

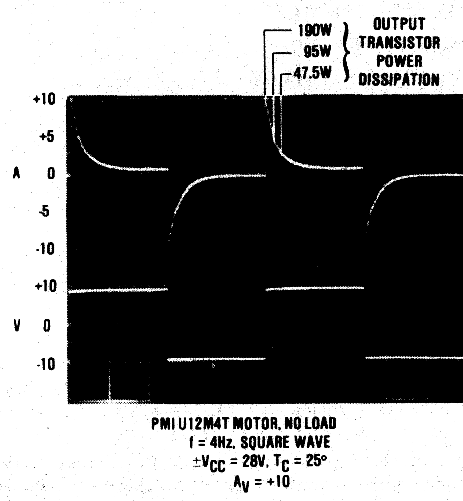


FIGURE 13. Servomotor Drive—"Plugging"

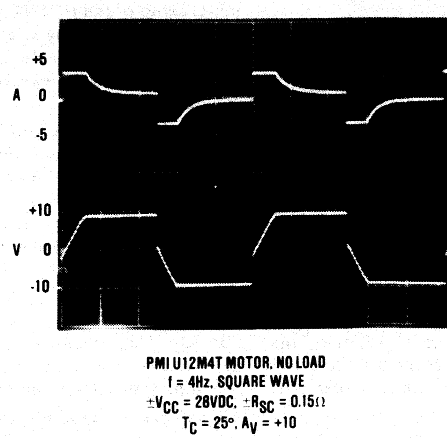


FIGURE 14. Servomotor Drive With Current Limit.

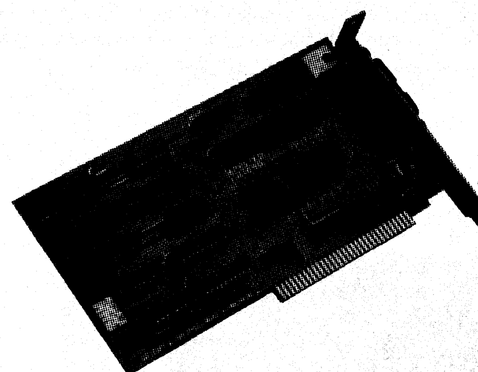
BURR-BROWN®

PC4311

IBM-PC IEEE-488 INTERFACE

FEATURES

- MENU DRIVEN SOFTWARE
- EXTENSIVE DOCUMENTATION
- MIL SPEC SOCKETS
- TMS9914A BASED
- LED STATUS DISPLAY
- FULL GPIB COMPATIBILITY
- SWITCH SELECTABLE ADDRESSING
- SUPPORTS INTERRUPTS
- DMA CAPABILITY



DESCRIPTION

The PC4311 is an IEEE-488 (GPIB) interface to the IBM-PC or any strict PC compatible microcomputer. It is based on the Texas Instruments TMS9914A, and can be programmed as a Talker, Listener, *or* Controller.

With a PC4311 installed in your IBM-PC, communication with and control of a wide range of "intelligent" equipment is possible. Equipment such as voltmeters, oscilloscopes, signal generators, and programmable power supplies can be easily interconnected.

A comprehensive software package, which includes a PC-DOS or MS-DOS compatible diskette containing source and executable code, is provided with each PC4311. Together, the hardware and software allow you to quickly utilize the flexibility of the IEEE-488 standard, and optimize your system's performance.

Supporting programmed I/O, interrupt driven and DMA transfers, the PC4311 architecture occupies 16 consecutive I/O addresses of the host system. The base address, which is switch selectable, can be set to begin on any unreserved boundary as described in the technical specifications. IRQ level and DMA channel selection are jumper options. The 16 locations are divided into eight Read and eight Write registers. To increase the flexibility of the board, one of the Write registers has been designated to configure the board as either a Talker/Listener or as a controller, under software control.

Eight LEDs provide visible information about the state of the GPIB management and control lines. This feature is particularly useful for initial checkout of the bus.

The standard GPIB cable is connected directly to the PC4311, which eliminates the need for a transition cable. Also, the use of high reliability IC sockets for all replaceable components cuts the time required for troubleshooting and repair, should that be necessary, to a minimum.

Three levels of software are provided. The menu driven program is intended for first time users and GPIB/PC4311 familiarization. MENU guides the programmer through the initial setup of the PC4311, passes data from the keyboard to the PC4311 and any selected GPIB device, and displays data received from the device. An extensive "help" section provides feedback for explanation of commands and error conditions.

The Level II software consists of two sets of linkable subroutines. One set of subroutines may be used for applications wherein the GPIB code must be a part of a larger program. The second set of subroutines is specifically designed to interface with Basic. Calls can be made from Basic to execute IEEE-488 functions.

Level III software is an installable device driver. The user modifies the CONFIG.SYS file to install the device driver at system load time. This device driver handles string transfers. This level of software provides the final link to the user most comfortable with the PC-DOS or MS-DOS operating system environment.

All software products include both source and executable code on the diskette, which is *not* copy protected. Printed copies of the assembled programs are included in the technical manual.

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SPECIFICATIONS

SYSTEM CLOCK RATE, max.
5.0 MHz

OPERATING RANGE
0° to +50° C

I/O ADDRESSING
Any 16 consecutive I/O addresses on the IBM PC Bus, jumper selectable to the 16 port boundaries beginning at base address 250H, 260H, 330H, 340H, 350H or 360H.

I/O PORT DESCRIPTION

Address	*Read*	*Write*
Base +0:	Interrupt Status 0	Interrupt Mask 0
Base +1:	Interrupt Status 1	Interrupt Mask 1
Base +2:	Address Status	
Base +3:	Bus Status	Auxiliary Command
Base +4:	Address Switch 1	Address Register
Base +5:		Serial Poll
Base +6:	Command Pass Through	Parallel Poll
Base +7:	Data In	Data Out
Base +8:		D0=1 Talk/Listen Only D0=0 Controller

HARDWARE COMPATIBILITY
IBM PC/XT/AT and strict compatibles

SOFTWARE COMPATIBILITY
PC-DOS, MS-DOS operating systems;
Source and executable code 8088 compatible

VOLTAGE REQUIREMENTS
+5 VDC @ 500 mA max.

TRANSFER RATE, max.
Dependent upon software and slowest device on GPIB Bus

INTERRUPT OPTIONS
Jumper selectable interrupt levels IRQ2-IRQ7

DMA OPTIONS
Jumper selectable DMA levels 1–3

CONNECTOR TYPE
24 Pin GPIB Connector

VISUAL INDICATORS
LED array for GPIB control lines

PHYSICAL DIMENSIONS
3.9″ X 7.2″

IC-TYPE
TMS9914A or equivalent

GPIB BUS DESCRIPTION

Pin	Signal	Description
1	DIO1	DATA1
2	DIO2	DATA2
3	DIO3	DATA3
4	DIO4	DATA4
5	EOI	END OR IDENTIFY
6	DAV	DATA VALID
7	NRFD	NOT READY FOR DATA
8	NDAC	NOT DATA ACCEPTED
9	IFC	INTERFACE CLEAR
10	SRQ	SERVICE REQUEST
11	ATN	ATTENTION
12	SHIELD	SHIELD GROUND
13	DIO5	DATA5
14	DIO6	DATA6
15	DIO7	DATA7
16	DIO8	DATA8
17	REN	REMOTE ENABLE
18	GND6	GROUND FOR PIN6
19	GND7	GROUND FOR PIN7
20	GND8	GROUND FOR PIN8
21	GND9	GROUND FOR PIN9
22	GND10	GROUND FOR PIN10
23	GND11	GROUND FOR PIN11
24	GNDLOGIC	LOGIC GROUND

SOFTWARE DESCRIPTION

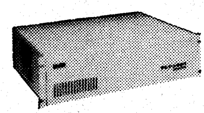
Example of a Basic Interface:

```
10  IOADDR%=&H25Ø        *IBM-PC I/O Address
20  GPADDR%=&HA          *PC4311 IEEE-488 Address
30  CNTL%=%HØ            *PC4311 is the Controller
40  DEVADDR%=&H14        *IEEE-488 device
50  DEF SEG=Ø
60  INIT=PEEK(&H4FØ)+(256*PEEK(&H4F1))
      *Get Offset
70  SUBSEG=PEEK(&H4F2)+(256*PEEK(&H4F3))
      *Get Segment
80  DEF SEG=SUBSEG
90  CALL INIT(IOADDR%,GPADDR%,CNTL%,
      AMTWRT%,AMTRD%,ERRNUM%)
100 REM PC4311 NOW INITIALIZED
110 SUBWRT=INIT+AMRWRT%
120 SUBRD=INIT+AMTRD%
130 WRTSTR$="ZF3R4"
140 CALL SUBWRT (DEVADDR%,WRTSTR$,
      ERRNUM%)
150 REM WRTSTR$ WAS WRITTEN TO IEEE-488
      DEVICE
160 STOP
```

All products are shipped with a complete documentation package which includes comprehensive operating instructions, user option tables, parts placement diagrams, and software examples.

BURR-BROWN®

PCI-3002 SERIES
PCI-3003 SERIES

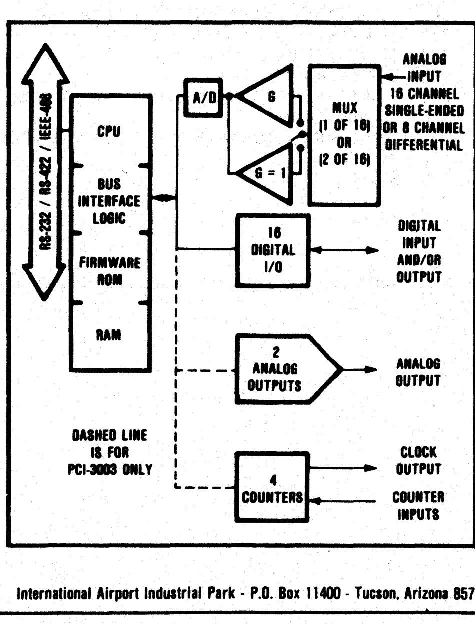


ADVANCE INFORMATION
Subject to Change

MID-SIZED, DATA ACQUISITION, TEST, MEASUREMENT AND CONTROL SYSTEMS

FEATURES

- 16 CHANNELS ANALOG INPUT (SINGLE-ENDED), 8 CHANNELS (DIFFERENTIAL)
- 2 CHANNELS ANALOG VOLTAGE OUTPUT
- 12-BIT RESOLUTION, ±0.1% ACCURACY
- 16 POINTS, DIGITAL INPUT/OUTPUT
- 4 CHANNELS, 16-BIT EVENT COUNTERS
- CLOCK OUTPUT
- BUILT-IN SIGNAL TERMINATION PANEL
- COMMUNICATIONS WITH MOST HOST COMPUTERS VIA RS-232, RS-422 OR IEEE-488 PORTS
- COMPATIBLE WITH OTHER PCI-3000 SYSTEMS PRODUCTS



DESCRIPTION

The PCI-3002 and PCI-3003 Series are Data Acquisition, Test, Measurement and Control Systems, designed for mid-sized applications. These master enclosures contain a built-in microprocessor, power supply, combination input/output board, and an integral signal termination panel. The microprocessor provides intelligence for task scheduling, data bus translation and data storage. Convenient screw terminals on the termination panel make connections to "real-world" signals easy.

The PCI-3003 hardware supports Analog inputs, Analog outputs, Digital I/O and Digital Counters. The PCI-3002 contains hardware for Analog inputs and Digital I/O, only.

Communications between these products and their host computer (or terminal) can be via RS-232, RS-422 or IEEE-488 ports. The RS-422 protocol supports multi-dropped (networked) connections between the host and up to 31 PCI-3000 series master enclosures. IEEE-488 allows the interconnection of several standard laboratory instruments along with the one or more PCI-3000 systems.

The PCI-3002/3 and the other PCI-3000 series of systems provide a powerful, adaptable, expandable and cost effective solution for data acquisition, test, measurement and control applications. Systems ranging from just a few channels to over 31000 are easily configured using a single host computer.

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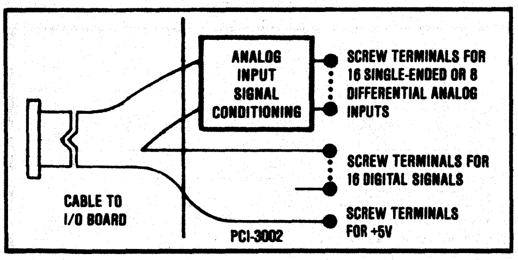
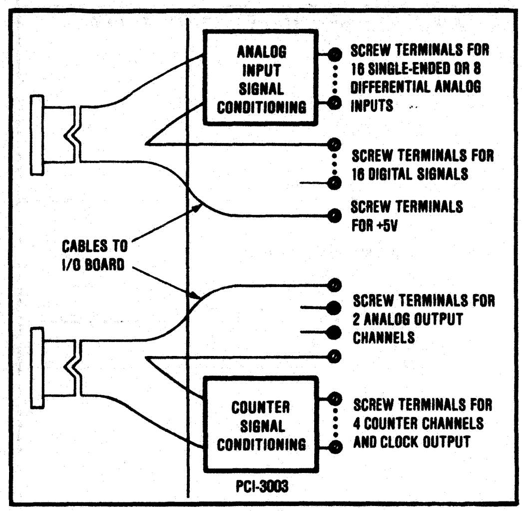
SPECIFICATIONS

(For all models unless otherwise noted.)

POWER REQUIREMENTS	
Line voltage	PCI-3002-1/3003-1 105VAC to 132VAC PCI-3002-2/3003-2 207VAC to 260VAC PCI-3002-3/3003-3 87VAC to 110VAC
Frequency	48Hz to 420Hz
Power	60W
TEMPERATURE RANGE	0°C to 50°C
DIMENSIONS (nominal)	W - 17 3/4", D - 14 1/4", H - 5 1/4". Standard 19-inch rack-mount ears installed.
COMMUNICATIONS	Two asynchronous serial channels, 300-9600 baud. RS-232-C on both channels. RS-422 signals on channel A (2-wire, half duplex, up to 4000 feet). IEEE-488 (optional), controlled by host.
LANGUAGE/CODE	Accepts high level commands in either ASCII or Binary format
USER MEMORY	8k bytes of user RAM installed. Expandable to 32k bytes, RAM or EPROM.
ANALOG INPUTS	±10mV to ±10V direct inputs (higher with attenuation added to termination panel). Convertible to current input.
A/D Input Range	Standard: 0 to 10V Jumpered: ±2.5V, ±5V, ±10V, 0 to 5V
Output Format	Standard: Binary positive (0 to +4095) Jumpered: Two's complement (−2048 to 2047)
Channels	16 single-ended 8 differential
Resolution	12 bits
Accuracy	±0.1% of full scale
Speed	2000 readings/sec (into internal memory), up to 30 readings/sec returned to host, at 9600 baud
INPUT AMPLIFIERS	Software-selected, instrumentation amplifiers
Amp #1	Fixed (G=1)
Amp #2	Variable via resistor selection (G=1 to 1k). G=1 + (40k/R). Supplied with G=201 (standard)
Maximum Input	±15V (without damage)
CMRR	90dB at 60Hz (1k source imbalance)
I_{bias}	10nA
THERMOCOUPLE INPUTS	Direct inputs for types J, K, T and S
Accuracy	±0.7°C (including software linearization)
ANALOG OUTPUTS	PCI-3003 only
Channels	Two
D/A Output	Standard: ±10V Jumpered: ±2.5V, ±5V, 0 to 10V, 0 to 5V
Input Format	Standard: Two's complement (−2048 to 2047) Jumpered: Binary positive (0 to +4095)
Resolution	12 bits
Accuracy	±0.1% of full scale
Write Time	33msec, at 9600 baud
DIGITAL INPUTS/OUTPUTS	
Number of Bits	16
Organization	Two 8-bit bytes
Input/Output	Each byte selected by jumper
Logic Levels	Standard TTL
Output Current	24mA sink, 15mA source
Speed	Read or set bits, bytes or word at the rate of 30 per second (at 9600 baud)
Optoisolation	Compatible with external optoisolated termination panel
DIGITAL COUNTERS	PCI-3003 only
Function	Count Events
Number	Four
Resolution	16 bits
Pulse Width	60nsec, minimum
Input Frequency	8MHz, maximum
Logic Levels	Standard TTL
CLOCK OUTPUT	PCI-3003 only
Output Frequency	8Mz/(MxN) 2MHz maximum, 0.002Hz minimum
Dividers	Two 16-bit counters (M, N)
Waveform	Squarewave
Output levels	Standard TTL
TERMINATION PANEL	Internal to enclosure
Functions	Field signal connection points for analog inputs, digital I/O's, +5V and cold junction compensation PCI-3003 only: Analog outputs, counters and clock.
Signal Conditioning	User space for passive conditioning, ie: Terminations, filtering, surge protection, attenuation, etc.
Screw Terminals	Clamp type - Accept wires from 24AWG to 14AWG
ACCESSORIES	
Software Support	PCI-4901-1, BASIC callable routines. PCI-3919-1, BASIC program examples, plus PCI-3000 Tutorial.
Communications	PCI-3901-1, IEEE-488 communications port.
Memory	RAM or EPROM conforming to BYTE-WIDE format.

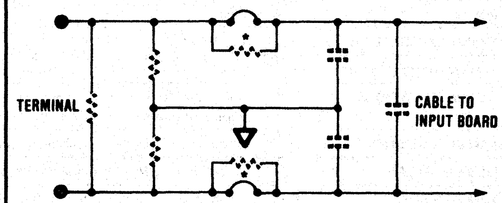
TERMINATION PANEL





ANALOG INPUT

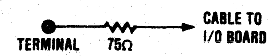
Schematic showing 2 terminals (1 of 8).
These are either 2 single-ended channels or 1 differential pair.



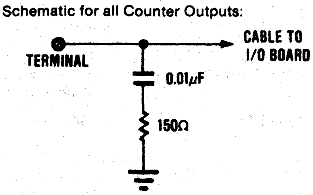
NOTE: Dashed lines indicate where components may be installed.
*This resistor location shipped with jumper installed.

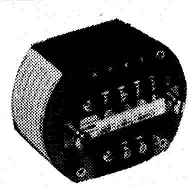
COUNTERS

Schematic for all Counter Inputs and Enables:



Schematic for all Counter Outputs:





PCI-3940 SERIES

High Accuracy INDUSTRIAL TWO-WIRE TRANSMITTERS

The PCI-3940 series is a family of industrial two-wire transmitters intended for remote signal conditioning and acquisition. Models are tailored for a wide range of input signals including DC, RTDs and thermocouples. All units have switches that provide field selection of input and output ranges. Four to 20mA or 10 to 50mA output current is user selectable. Current output is desirable because it has reduced sensitivity to wire length and noise pick-up. The three basic models are available in both isolated (-2 models) and non-isolated versions (-1 models).

The 600V input isolation rating allows for power line fault protection and ground loop elimination in most industrial, factory and laboratory applications. DC signal levels from 1mV to 10V as well as 100Ω RTDs and J, K, T thermocouples are accommodated. Internal cold junction compensation and linearization are also provided. Direct screw terminal connections along with several mounting configurations make installation quick and easy. Refer to the PCI-3940 series product data sheet for additional information.

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PCI-4304 SERIES

PCI-4304-1 Complete Logic Analyzer System
(Contains 1 each: PCI-4304-2, PCI-4905-2, PCI-4906-1)
PCI-4304-2 Plug-In Analyzer PC Board Only
PCI-4905-2 Analyzer Software plus Instrument Pod
PCI-4906-1 Package of 45 Input-lead Probe Clips

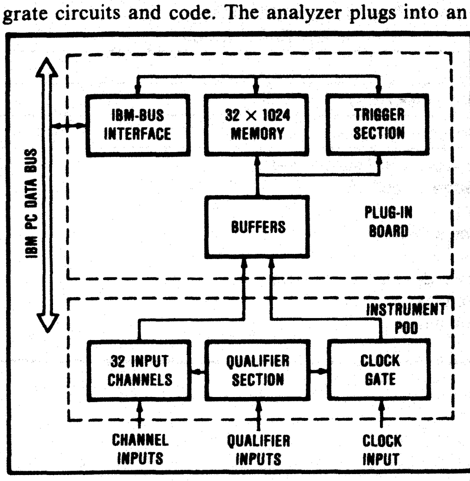
LOGIC STATE ANALYZER PLUG-IN BOARD AND ACCESSORIES for IBM Personal Computer

FEATURES

- MENU-DRIVEN SOFTWARE FOR STATE AND TIMING ANALYSIS
- LOW COST
- PC PROVIDES STORAGE OF DATA ON DISK, PRINTING, AND DISPLAY
- 32 CHANNELS × 1024 WORDS INPUT
- 3 QUALIFIER PAIRS
- INPUT RATE = 13MHz maximum
- SEQUENTIAL TRIGGERS ALLOW DATA-CAPTURE WINDOWS

DESCRIPTION

The PCI-4304 is a low-cost digital logic analyzer for state and timing analysis. It can be used to trace software flow, for hardware analysis, and to integrate circuits and code. The analyzer plugs into an IBM PC, XT, Compaq, or compatible personal computer. The PC provides the analyzer with black and white or color display capabilities, floppy or hard disk data storage, hard-copy printing, and communications networking capabilities. The PCI-4304 can be integrated alone or with other personal computer instrumentation products to create automated test systems, event recorders, integrated laboratory instrumentation systems, etc.



The PCI-4304 has 32 input channels, three qualifier pairs, a 1024-word memory, and it operates up to 13MHz. The clock signal is derived from the circuit under test for synchronous-state analysis, or from an external clock for timing analysis. Since the most useful information in a digital system occurs at the system's clock transition, the PCI-4304 features zero hold-time; that is, the data present at a clock transition is stored.

Inputs to the analyzer board are preprocessed by a convenient instrument pod. The pod connects to the analyzer board through flat ribbon cables. All signal inputs from the pod are easily connected to test clips, integrated circuit DIP clips, or to 0.025 square-post terminal test points.

Measurement parameters are selected quickly using interactive software menus. Up to eight 32-bit trigger words can be used to sequentially start or stop a data trace or to form data-capture windows. Trigger delay and choice of clock edge are also easily selected. The sophisticated triggering structure of the PCI-4304 permits a wide variety of data-capture alternatives. Data can be displayed graphically using the timing analysis mode or in binary, decimal, hexadecimal, octal or ASCII using the state analysis mode. Both data and setups can be stored or recalled from the personal computer disk. In addition, captured data can be compared with previously recorded data. Variations between two sequences

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are displayed highlighted in color, or in changes of screen intensities, so differences can be rapidly seen. A personal-computer printer can permanently record a timing diagram or tabular state analysis information.

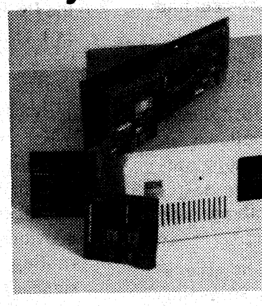
The PCI-4304-1 is a complete logic state analyzer kit that contains the plug-in PC board, instrument pod, software disk, user manual, and a package of input-lead probe clips. The plug-in board, pod-plus-software, and clips are available separately.

SPECIFICATIONS

PCI-4304-1	
IBM BUS INTERFACE	
Number of Addresses Used	16k memory addresses
Base Address Selection: Number of switches	4
Selectable range	1 of 9 64k spaces
Power Requirements: Voltage used	+5VDC
Maximum current	3A
HARDWARE SPECIFICATIONS	
MEMORY	1024 × 32-bit words
TRIGGERING	
Eight Trigger Words	32 bits each
Delay	Up to 511 clock cycles
Data Taken	On rising or falling clock pulse edge
TIMING INFORMATION	
Data Setup Time	20nsec
Data Hold Time	0nsec
Qualifier Setup Time	20nsec
Qualifier Hold Time	0nsec
INPUTS	
Data Path Width	32 bits
Load	One low-power Schottky
Low Input	+0.4VDC
High Input	+2.4VDC
Threshold	1.5V (TTL)
Maximum Input Range	−0.5VDC to +5.5VDC
CLOCK	
User Supplied	By circuit under test (or other external source)
Signals	To 13MHz maximum
Minimum Pulse Width	20nsec
MECHANICAL	
Plug-in PC Board	Designed to fit IBM PC and hardware-compatible expansion slots
Instrument Pod	Approximate dimensions: 4 × 8.5 × 1.3 inches 10.2 × 21.6 × 3.3 cm
SOFTWARE SPECIFICATIONS	
IBM PC MEMORY REQUIRED	256k minimum; 1 disk drive
SOFTWARE STRUCTURE	Interactive menus
SOFTWARE ABILITIES	Set up trigger words and sequences Clock pulse edge selection Delay selection Start data trace selection Display data Compare known data to current data Store data to a disk Read data from a disk Print data

PCI-20000

INTELLIGENT INSTRUMENTATION for Industry and Laboratory



INTRODUCTION

The PCI-20000 is an intelligent instrumentation front end, designed to turn the personal computer (PC) into a powerful system for data acquisition, test, measurement and control. The system resides on a printed circuit board that plugs into an available expansion slot within the host PC. The internal PCI-20000 architecture is designed to interface with most microcomputers. Compatibility with a specific PC is achieved with bus translation circuitry located on the plug-in board. Direct connection is made to the PC's internal computer bus allowing high speed data acquisition and control.

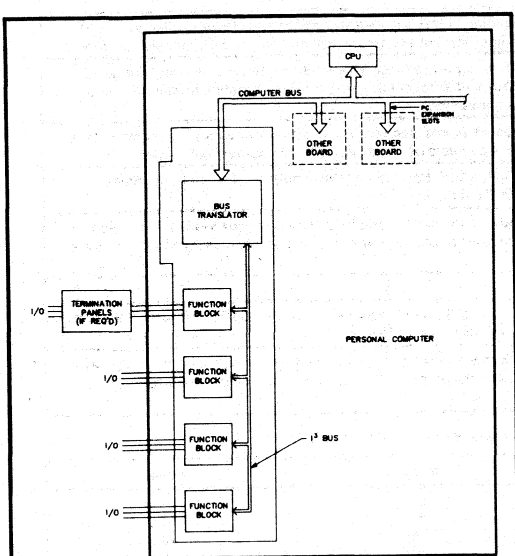


FIGURE 1. Personal Computer-Based Data Acquisition and Control System—Block Diagram.

Figure 1 is a block diagram showing the system configuration. The unique design of the PCI-20000 allows the input/output configuration to be optimized for a particular application. The key concepts embodied within the PCI-20000 system include its modular construction, its proprietary "Intelligent Instrumentation Interface Bus" (I^3 Bus - patent pending) and its memory mapped address structure.

Mechanically, the PCI-20000 system consists of two types of printed circuit boards. The main boards are known as "Carriers." The other boards are "Instrument Modules" which connect, piggyback style, to the carrier. It is the carrier that plugs into one of the PC's expansion slots.

The family of carriers now contains two types. These first models are designed for the IBM series of PC's as well as the COMPAQ, AT&T and other IBM compatible personal computers.

Each carrier provides mounting space for up to three modules. The carrier also includes the Intelligent Instrumentation Interface Bus (I^3 Bus), and the PC bus interface and logic circuits. In addition to the above features the second carrier also provides 32 fully buffered digital input/output points.

A wide variety of instrument modules for analog and digital applications are available. Because of the versatility of the I^3 bus, the family of modules will grow. In addition, the modules can be treated as building block components that will find wide application in the design of systems of other manufacturers.

Signal termination panels within the system complement it, by providing convenient screw terminal connections between the internal electronics and the external field signals. Appropriate cables are available to link the termination panels to the instrument modules. Rack and table top enclosures are also available.

Several applications software support packages are available for the PCI-20000 system. Some of the packages contain a family of routines that can be called by high level commands. Versions to support BASIC, C and ASSEMBLY languages are now available. Complete instrumentation, laboratory and control packages can also be provided. These diskettes give the user easy access to the extensive data acquisition, test, measurement and control features of the system.

The classic deficiencies found in other single board data acquisition systems are largely eliminated in this design.

1. A wide variety of I/O types are supported, as follows: analog input (voltage, current, thermocouple, etc...), simultaneous multiple channel readings, analog output, digital input, digital output, counter input, frequency measurement, pulse generation along with high speed triggering and alarm monitoring.
2. Relatively large numbers of channels can be accommodated. Up to 128 digital I/O points or 80 analog inputs or 6 analog outputs or 12 counter/timer ports can be configured on a single carrier, using the instrument modules available. In addition, multiple carriers can be used simultaneously.
3. By selecting the appropriate mix of modules, the capability of the system can be tailored to a particular application. Thus, function and cost can be optimized. Modules can be added, changed or rearranged at any time to satisfy new measurement or control requirements.
4. Probable conflicts in available address space within the PC have been eliminated by the choice of memory vs I/O mapping. Only two kilobytes are decoded on the I/O side of the IBM PC, while 100's of kilobytes are potentially available in RAM address space. Switches on the carrier allow placing the unit anywhere in the PC's memory map.
5. In addition to the memory and digital I/O connections provided by a standard computer bus, the internal Intelligent Instrumentation Interface (I^3) bus also provides for analog, synchronization and trigger signal routing. This facility allows the chaining of analog signals from one module to another as well as the triggering or synchronizing of events on a particular module by another module.

Figure 2 is a summary of the PCI-20000 system specifications.

HOST COMPUTER COMPATIBILITY	Suitable for the IBM PC/XT/AT family of PC's, COMPAQ, AT&T or other hardware compatible personal computers.
MECHANICAL	Electrically, a CARRIER takes one expansion slot in the host. Mechanically, part or all of the adjacent slot may be occupied depending upon the installed module configuration. TERMINATION PANELS reside outside the host, optionally, in rack or table mount enclosures.
ANALOG INPUTS Single-ended or differential, voltage or current	±10mV to ±10V direct inputs (higher with attenuation on termination panel). 12-bit resolution, ±0.04% accuracy, ±0.04% linearity. PGA, G =1, 10, 100, 1000. CMV = ±10V, CMR = 106dB. Speed, up to 80K readings/sec. Up to 16 channels per module, and up to 80 channels per carrier using the 32-channel expansion modules.
ANALOG OUTPUTS	±10V and 4-20mA outputs. 12-bit resolution, ±1/2LSB linearity, monotonic, 8V/µsec slew rate. ±10 V output, 16-bit resolution, ±0.003% FSR linearity. 1 or 2 channels per module, up to 6 channels per carrier.
DIGITAL Input & Output	TTL compatible, 24mA current sink, 15mA current source. Read/set bits, bytes or words. High voltage isolation (4000V AC/DC) and 3A (AC/DC) switch capability using the opto-isolation termination panels. 32 points per module, up to 128 points per carrier.
COUNTERS	TTL compatible. Up to 8MHz inputs. Count events, accumulate, measure frequency. 16-bit resolution. 8MHz time-base with 0.008% accuracy. 4 counters per module, up to 12 counters per carrier.
PULSE OUTPUTS	TTL compatible. Finite or continuous outputs. Pulse or squarewave outputs. Output frequencies of 0.002Hz to 2MHz. 125ns resolution. 0.008% accuracy.
TERMINATION PANELS	Provides a screw terminal interface between the system and field signals. Types available: Analog I/O, Thermocouple Input, Digital I/O and Opto-isolation. Rack and table top enclosures for 1 to 4 panels are available.
TEMPERATURE RANGE	0 to 50°C, Ambient.
POWER REQUIREMENTS	+5V @ 600mA Quiescent carrier (1C-2) current, add individual modules POWER for total. 2.9A Max current, fully loaded. DC to DC converter efficiency = 50%.
SOFTWARE	Applications software packages provide machine language routines that can be called from high level languages to control most functions. Complete programs for instrumentation and control functions are also available.

SPEED SUMMARY

All data is expressed in readings/sec, and includes the time to read or write to RAM.

PARAMETER	CONDITIONS	IBM-PC	IBM-AT
ANALOG INPUT	PCI-20014S-1 Software		
	Normal Analog Read mode	130	337
	Thermocouple Read mode	75	234
	Block mode, 2M Module	7K	10K
	19M Module	45K	65K
ANALOG OUTPUT	PCI-20014S-1 Software	129	338
DIGITAL I/O	PCI-20014S-1 Software	126	326
	Assembly code, with sync	45K	90K
COUNTER	PCI-20014S-1 Software	126	331
	Assembly code, sync and reset	24K	48K

FIGURE 2. PCI-20000 General System Specifications.

Conditions: IBM PC, using most appropriate PCI-20000 hardware.

CONFIGURING A PCI-20000 SYSTEM

This section is an aid in configuring a system for a given application. The first step involves listing the specific input/output requirements for each application. With this information, the following guide will provide the needed PCI-20000 system specifications.

The PCI-20000 is intended for small and medium sized tasks, where the host computer can be located near the application. The maximum channel capacity for this system is shown in Figure 2. Note that more than one carrier can often be used to increase the system's capacity. Carriers can either be installed within the host computer or in expansion enclosures. More detailed information about each component appears in later sections of this brochure.

For large scale, distributed or remote applications, the PCI-3000 system is suggested. This type of system can be expanded to almost 32,000 channels and can be located at any distance from the host computer. Please refer to the Burr-Brown product data book or contact your local representative for the appropriate PCI-3000 literature.

Fundamental to configuring a system is the selection of a carrier. The difference between the two available carriers is the inclusion of 32 digital I/O points on the PCI-20001C-2. This carrier provides a significant level of digital capability, at very low cost, without occupying an instrument module location.

Figure 3 graphically shows all of the components that comprise the PCI-20000 system. Also indicated are the associated options and accessories. Compatibility of each group of components is indicated by the interconnecting lines. Note that there are compatible components having part numbers in the 1100, 3000 and 20000 series.

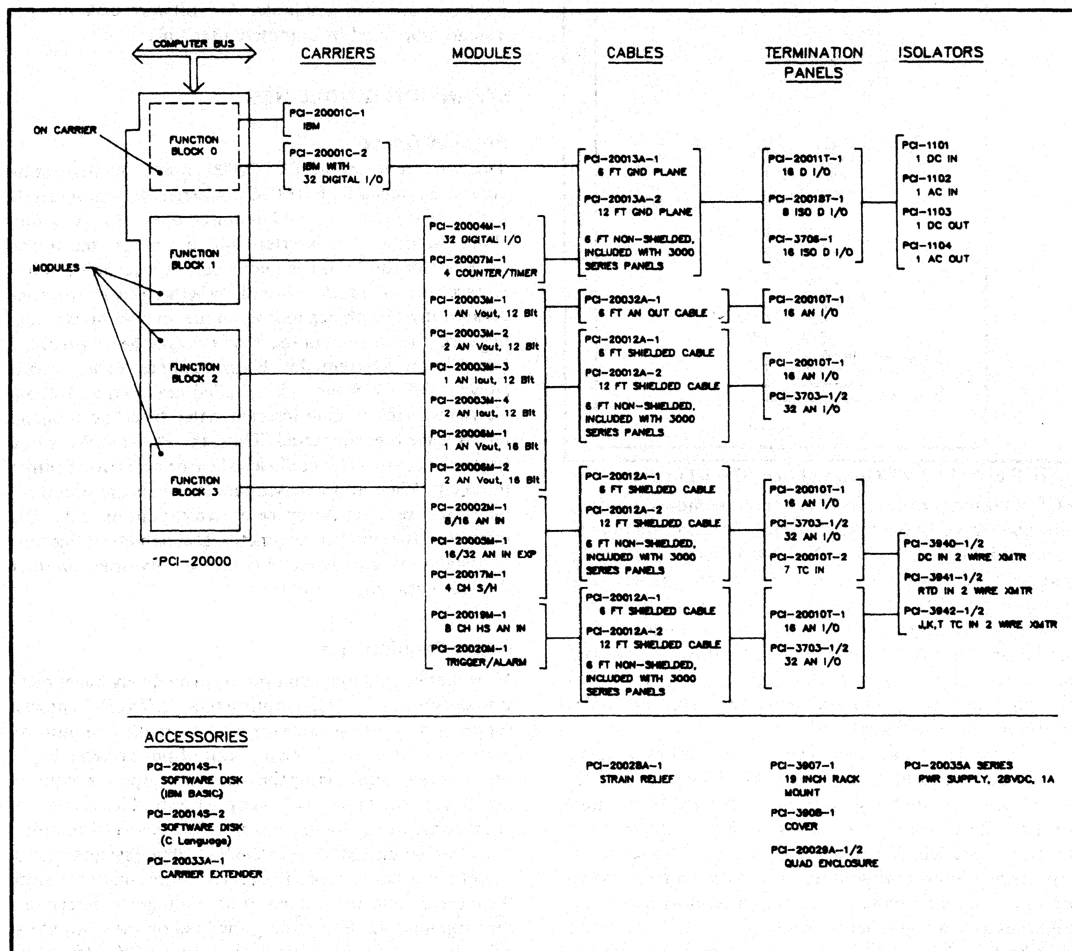


FIGURE 3. PCI-20000 — System Component Configuration Guide.

Some analog input modules can be configured for either single-ended or differential use. Be sure to account for the proper number of channels (differential yields half as many) when selecting the number of modules required. The I^3 bus structure shown in Figure 4 suggests how the analog chain can connect the output of one module to the input of another. This feature provides channel multiplexing capability with the analog expansion module.

Digital function blocks can be software configured for either input or output use, in groups of eight points (byte size). Thus, a 32-point module can be used for 8 inputs and 24 outputs or 16 inputs and 16 outputs or 32 outputs, etc...

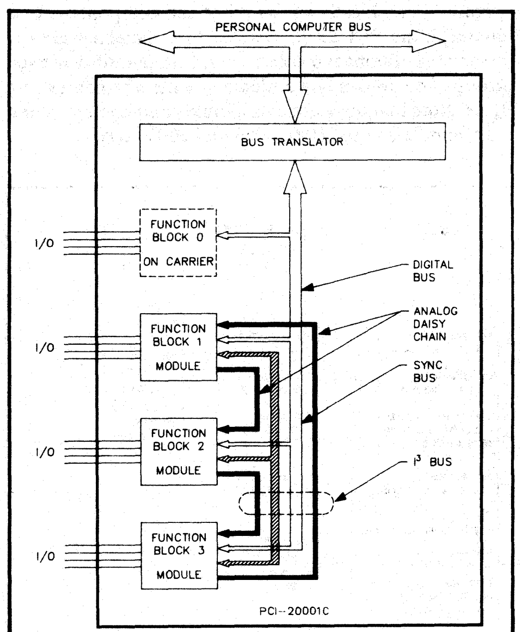


FIGURE 4. PCI-20000 Simplified Block Diagram.

PCI-3000 series of termination panels include 6 foot long non-shielded ribbon cables to make connections to the various I/O boards. The PCI-20000 series provides a choice of shielded cables to connect the panels. The possible benefits of shielded or ground-plane cables should be considered. Use of these types of cables often results in improved signal to noise ratio and reduced electrical interference. Within the analog or digital groups, shielded or ground-plane and non-shielded cables are physically interchangeable.

All termination panels have provisions for user defined, passive signal conditioning. The PCI-3703 series of panels is optionally available with or without straight through jumpers. The other panels come with straight through jumpers installed. When several cables are required to exit the personal computer, it is often convenient to make use of any unused, expansion board mounting locations. An accessory strain relief connector is available to secure the ribbon cables and help protect internal components (PCI-20028A-1).

The 1100 series, optical couplers, are for digital use only. Each coupler supports one signal. The four different types of couplers can be mixed on a single termination board with one restriction; remember, that digital function blocks can only be set for input or output use in groups of 8 points.

Remote sensing of analog signals can be accomplished with the PCI-3940 series of two-wire transmitters. DC, RTD and Thermocouple input models are available in both isolated and non-isolated versions. These units are field programmable for a wide range of input levels and types.

DOCUMENTATION AND SOFTWARE SUPPORT

The PCI-20000 system is fully supported by written documentation in the form of a user's manual. The manual provides detailed instructions for the installation, setup and programming of all hardware components. In addition, a family of Applications Software Support Packages are also available. All software diskettes are also accompanied by complete user's manuals.

EXPANSION GUIDELINES

Physical Space

The minimum useful PCI-20000 system configuration consists of only a PCI-20001C-2 Carrier. This provides 32 points of digital I/O, and requires one expansion slot. When Modules are inserted into a Carrier, the added thickness of the Modules may result in mechanical interference with an adjacent board. Whether this interference actually does result depends upon the number of Modules installed, the location of the Modules and the length of the board in the adjacent slot. If for example, a short board (Async, IEEE-488, etc...) is installed next to a PCI-20000 Carrier with one module inserted in the "front" position, no interference is encountered. Thus, the PCI-20000 is still a single slot device. This could also be true with two Modules installed. When all three Module locations are occupied, the system requires the space of two expansion slots. It is interesting to note that the functional capability of this type of installation greatly exceeds that of any other product that occupies only two slots.

Power Requirements

Most modern personal computers provide several expansion slots for user selected option boards. The PC's power supply is designed to provide a "reasonable" amount of current to these slots. The amount of power available is determined by subtracting the base systems power requirements from the total power supply rating. Please consult your computer's documentation for this information. Each Carrier and Module in the PCI-20000 system has its power requirements specified. It is a simple matter to sum the individual terms (current times voltage) to determine the total load. In determining the load on the computers +5 volt supply, it is necessary to apply a 50% efficiency factor to the DC/DC converter that generates the ±15 volt supply on the carrier. Because of the hundreds of possible PCI-20000 configurations and the different computer power supply ratings, it is not practical to generate a compatibility table. In general, however, adequate power is available for all boards that will physically fit in a given PC.

PCI-20000 specifications

Carriers

PCI-20001C-1 Carrier Card
- Plugs into IBM PC, XT, AT, Compaq expansion slots
- Holds up to 3 instrument modules
- Provides address decoding for memory-mapped modules

PCI-20001C-2 Carrier Card
- Same as PCI-20001C-1 but also includes 32 points digital I/O

Instrument Modules

PCI-20002M-1 Data Acquisition Module
- 16-channel single-ended analog input (8-channels differential input)
- 12-bit accuracy and resolution A/D converter
- Programmable gain of 1, 10, 100, 1000
- Computer control of gain, channel selection and initialization of conversion
- Single-channel conversion time = 40μsec

PCI-20003M Series Analog Output Modules
- 12-bit resolution digital-to-analog converters
- Scalable outputs
  - Voltage converters: 0–10V FS, ±5V FS, ±10V FS
- PCI-20003M-1: 1-channel voltage-output
  - -2: 2-channels voltage-output

PCI-20004M-1 Digital Input/Output Module
- 32 points, 4 groups, 8-bit bytes
- TTL compatible, fully buffered

PCI-20005M-1 Analog Input Expansion Module
- (expands input channels available for PCI-20002M-1)
- Provides 32 additional single-ended analog input channels or 16 additional differential channels
- Input Voltage Range: ±10V
- Input Capacitance
  - Channel "ON": 30pF
  - Channel "OFF": 5pF
- "OFF" Input isolation: 65dB

PCI-20006 Series Analog Output Modules
- 16-bit digital-to-analog converters
  - Linearity 0.003% FSR
  - Slew Rate 10V/μsec
  - Settling Time 8μsec
  - Differential Linearity 0.006% FSR
- PCI-20006M-1: 1-channel voltage-output
  - -2: 2-channels voltage-output

PCI-20007M-1 Counter, Timer, Pulse-Generator Module
- Provides a stable time base for controlling data acquisition, frequency measurement, frequency generation, or event counting using a self-contained 8MHz clock
- 1 channel provides clock
- 4 channels can be used for:
  - Event counting
  - Frequency generation
  - Frequency measurement
  - Square-wave generation
- Choice of Hardware-Retriggered Strobe or Software-Triggered Strobe

PCI-20017M-1 Sample/Hold Module (4 channels)
- Simultaneous sample/hold with programmable gain
- Eliminates time-skew among channels
- Gains of 1, 10, 100, 1000
- Gain Error 0.1% at G = 1
- Linearity Error 0.03% at G = 1
- Slew Rate 0.2V/μsec (G = 1 to 100)
- Frequency Response (small signal) 100kHz (G = 1)
- Acquisition Time (to 0.01%) = 6μsec
- Aperture Delay (over temperature) = 275nsec max

PCI-20019M-1 Analog Input Module
- 8 channel, high-speed, data acquisition, single-ended, high-level analog input
- 12-bit resolution
- Data Rate of 50kHz throughput to memory (software controlled)
- Software control of multiplexer
- Total conversion time 11.5μsec max
- Jitter 200nsec max
- Automatic input scan if desired

PCI-20020M-1 Trigger/Alarm Module
- 1-channel digital signal output indicates one of:
  - Input below programmed threshold
  - Input above programmed threshold
  - Input between programmed limits
  - Input outside of programmed limits
- Threshold Voltages: Resolution of 8 bits
  - Linearity of 0.5LSB
- Hysteresis of 25mV, 10%
- Input Range 10V (15V without damage)
- Response Time (input to sync output) = 3.5μsec max

PCI-20031M-1 Fast Expander-Sequencer Module
- Expands input channels available for PCI-20002M-1 and/or PCI-20019M-1
- Provides 32 single-ended (16 differential), high-speed, analog input channels
- Provides automatic scan of a random list of analog channels at a high throughput rate
- Advances channels on command up to 128 entries
- Advances channels on sync signals until a "last channel" flag identifies the end of a scan list

Termination Panels

PCI-20010T-1 16/8 Channel Analog Termination Panel
- Space for 16 single-ended or 8 differential analog inputs
- Provision for 4–20mA transmitters
- Provision for thermocouples
- Provision for user-supplied signal conditioning:

PCI-20011T-1 16-Channel Digital Termination Panel
- Space for 16 digital inputs or outputs
- Easy-to-use high density screw terminals
- Provision for user-supplied signal conditioning

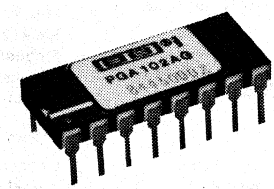
PCI-20018T-1 8-Channel Isolated Digital Termination Panel
- Accept standard Crydom or OPTO-22 modules
- AC or DC inputs or outputs—same options as isolated digital termination panels for PCI-3000 System

Software Support

PCI-20014S-1 BASIC Language Interface
PCI-20014S-2 "C" Language Interface
PCI-20014S-3 Turbo Pascal Language Interface
PCI-20014S-4 ASYST Scientific Software Interface
(used with ASYST I and/or ASYST II available from Macmillan Software Company)
PCI-20014S-5 IBM PC Combination Software Support Package
(includes PCI-20014S-1, PCI-20014S-2, PCI-20014S-3, and PCI-20014S-4)

BURR-BROWN®

PGA102



Digitally-Controlled Programmable-Gain/Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- DIGITALLY-PROGRAMMABLE GAINS, X1, X10, X100
- LOW GAIN ERROR, 0.01%, max
- LOW GAIN DRIFT, 5ppm/°C, max
- LOW NONLINEARITY, 0.003%, max, 14-BIT
- FAST SETTLING, 2.8μsec, 0.01%, typ
- THREE INDEPENDENT INPUT CHANNELS WITH SEPARATE GAIN ADJUSTMENT
- LOW COST
- SMALL 16-PIN DIP PACKAGE

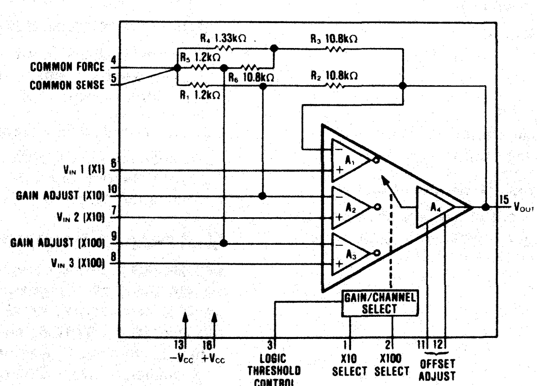
APPLICATIONS

- DATA ACQUISITION AMPLIFIER
- AUTORANGING AMPLIFIER UNDER COMPUTER CONTROL
- SUPER-ACCURACY, LOW COST, FIXED GAIN BLOCK
- TEST EQUIPMENT GAIN CONTROL
- PORTABLE INSTRUMENT GAIN SELECTION
- DATA LOGGING RANGING CONTROL
- 3-CHANNEL MULTIPLEXER

DESCRIPTION

The PGA102 is a precision digitally-programmable gain block. Its monolithic design permits low cost and high reliability. The user can select one of three gains (1, 10, 100), two of which are independently adjustable. The logic section has high input impedance and functions without a separate supply. Precision laser-trimmed offset and gains permit use without external adjustments. High performance thin-film resistors with excellent temperature tracking assure low gain drift and excellent stability.

The fast 2.8μsec settling makes the PGA102 ideal for rapid channel scanning in data acquisition systems. Also the high accuracy is very beneficial in test equipment and instrumentation applications where programmable or fixed gain is required.



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SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC unless otherwise specified.

PARAMETER	CONDITIONS	PGA102AG MIN	PGA102AG TYP	PGA102AG MAX	PGA102BG/SG MIN	PGA102BG/SG TYP	PGA102BG/SG MAX	UNITS
GAIN								
Inaccuracy[1]	R_L = 2kΩ, G = 1		±0.007	±0.02		±0.003	±0.01	%
	G = 10		±0.015	±0.03		±0.01	±0.02	%
	G = 100		±0.02	±0.05		±0.015	±0.025	%
vs Temperature	G = 1		±0.4	±5		*	*	ppm/°C
	G = 10		±2	±7		*	*	ppm/°C
	G = 100		±7	±20		*	*	ppm/°C
Nonlinearity	R_L = 2kΩ, G = 1		±0.001	±0.003		*	*	% of FS
	G = 10		±0.002	±0.005		*	*	% of FS
	G = 100		±0.003	±0.01		*	*	% of FS
RATED OUTPUT								
Voltage	R_L = 2kΩ	±10	±12.5		*	*		V
Current	V_{OUT} = 10V	±5	±10		*	*		mA
Short Circuit Current		±10	±25		*	*		mA
Output Resistance			0.01			*		Ω
Load Capacitance	For stable operation		2000			*		pF
INPUT OFFSET VOLTAGE								
Initial[2]	G = 1		±200	±500		±100	±250	μV
	G = 10		±70	±200		±50	±100	μV
	G = 100		±70	±200		±50	±100	μV
vs Temperature	G = 1		±5	±20		*	*	μV/°C
	G = 10		±1	±7		*	*	μV/°C
	G = 100		±0.5	±3		*	*	μV/°C
vs Supply Voltage	$\pm5 < V_{CC} < \pm18V$							
	G = 1		±30	±70		*	*	μV/V
	G = 10		±8	±30		*	*	μV/V
	G = 100		±8	±30		*	*	μV/V
INPUT BIAS CURRENT								
Initial	T_A = +25°C		±20	±50		*	*	nA
Over Temperature	T_{Amin} to T_{Amax}		±25	±60		*	*	nA
ANALOG INPUT CHARACTERISTICS								
Voltage Range	Linear operation	±10	±12		*	*		V
Resistance			7×10^8			*		Ω
Capacitance			4			*		pF
INPUT NOISE								
Voltage Noise	f_B = 0.1Hz to 10Hz,							
	G = 1		4.5			*		μV p-p
	G = 10		1.5			*		μV p-p
	G = 100		0.6			*		μV p-p
Voltage Noise Density	f_O = 1Hz, G = 1		490			*		$nV/\sqrt{Hz}$
	G = 10		178			*		$nV/\sqrt{Hz}$
	G = 100		83			*		$nV/\sqrt{Hz}$
	f_O = 10Hz, G = 1		155			*		$nV/\sqrt{Hz}$
	G = 10		56			*		$nV/\sqrt{Hz}$
	G = 100		20			*		$nV/\sqrt{Hz}$
	f_O = 100Hz, G = 1		93			*		$nV/\sqrt{Hz}$
	G = 10		31			*		$nV/\sqrt{Hz}$
	G = 100		18			*		$nV/\sqrt{Hz}$
	f_O = 1kHz, G = 1		79			*		$nV/\sqrt{Hz}$
	G = 10		31			*		$nV/\sqrt{Hz}$
	G = 100		18			*		$nV/\sqrt{Hz}$
Current Noise	f_B = 0.1Hz to 10Hz		76			*		pA p-p
Current Noise Density	f_O = 1Hz		8.8			*		$pA/\sqrt{Hz}$
	f_O = 10Hz		2.8			*		$pA/\sqrt{Hz}$
	f_O = 100Hz		0.99			*		$pA/\sqrt{Hz}$
	f_O = 1kHz		0.43			*		$pA/\sqrt{Hz}$

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	PGA102AG MIN	PGA102AG TYP	PGA102AG MAX	PGA102BG/SG MIN	PGA102BG/SG TYP	PGA102BG/SG MAX	UNITS
DYNAMIC RESPONSE								
±3dB Bandwidth	Small signal, G = 1		1500			*		kHz
	G = 10		750			*		kHz
	G = 100		250			*		kHz
Full Power Bandwidth	$V_{OUT} = \pm10V$, $R_L = 2k\Omega$		160			*		kHz
Slew Rate	$V_{OUT} = \pm10V$ step, $R_L = 2k\Omega$	6	9		*	*		V/μsec
Settling Time (0.1%)	V_{OUT} = 10V step, G = 1		1.6			*		μsec
	G = 10		2.2			*		μsec
	G = 100		5.2			*		μsec
Settling Time (0.01%)	V_{OUT} = 10V step, G = 1		2.8			*		μsec
	G = 10		2.8			*		μsec
	G = 100		8.2			*		μsec
Overload Recovery Time, 0.1%	50% overdrive, G = 1 (see Performance Curve)		2.5			*		μsec
CROSSTALK								
DC	±10V to both Off channels		−155			*		dB
60Hz	±10V to both Off channels		−144			*		dB
DIGITAL INPUT CHARACTERISTICS								
Input "Low" Threshold	V_{IL}(3) on pin 1 or 2			VLTC + 0.8			*	V
Input "Low" Current				1			*	μA
Input "High" Threshold	V_{IH}(3) on pin 1 or 2	VLTC + 2			*			V
Input "High" Current			0.1	1		*	*	μA
Logic Threshold Control	VLTC on pin 3	$-V_{CC}$		$V_{CC} - 4$	*		*	V
Switching Time(4)	Between channels		1			*		μsec
POWER SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range		±5		±18	*		*	VDC
Quiescent Current	V_{OUT} = 0V		±2.4	±3.3		*	*	mA
	No external load, $V_{OUT} = \pm10V$			±5.3			*	mA
TEMPERATURE RANGE								
Specification	T_{Amin} to T_{Amax}							
AG and BG grades		−25		+85	*		*	°C
SG grade		−55		+125	*		*	°C
Operating		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C
Thermal Resistance	θ_{JA}		100			*		°C/W

*Same specification as AG grade.

NOTES: (1) Gain inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero for gains of 10 and 100. (2) Offset voltage can be adjusted for any one channel. Adjustment affects temperature drift by approximately ±0.3μV/°C for each 100μV of offset adjusted. (3) Voltage on the logic threshold control pin, VLTC, adjusts the threshold for "Low" and "High" logic levels. (4) Total time to settle equals switching time plus settling time of the newly selected gain.

ABSOLUTE MAXIMUM RATINGS

Power Supply .... ±18V
Input Voltage Range, Analog .... $\pm V_{CC}$
Input Voltage Range, Digital .... (V_{PIN3} − 5.6V) to $+V_{CC}$
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (soldering 10 seconds) .... +300°C
Output Short-Circuit Duration .... Continuous to Common
Junction Temperature .... +175°C

PIN CONFIGURATION

X10 SELECT	1	16	$+V_{CC}$
X100 SELECT	2	15	V_{OUT}
LOGIC THRESHOLD CONTROL	3	14	NC*
COMMON FORCE	4	13	$-V_{CC}$
COMMON SENSE	5	12	OFFSET ADJUST
V_{IN1} (X1)	6	11	OFFSET ADJUST
V_{IN2} (X10)	7	10	GAIN ADJUST (X10)
V_{IN3} (X100)	8	9	GAIN ADJUST (X100)

*NO INTERNAL CONNECTION

ORDERING INFORMATION

PGA102 X G

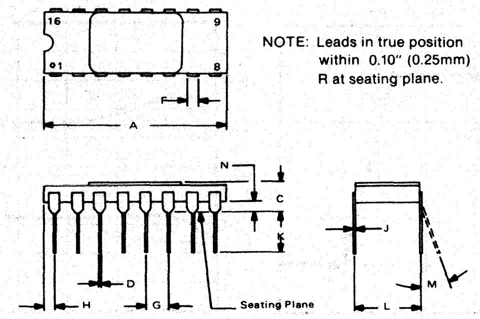
Basic Model Number — PGA102

Performance Grade Code — X
A, B: −25°C to +85°C
S: −55°C to +125°C

Package Code — G
G: 16-pin hermetic DIP

PGA102AG, PGA102BG, PGA102SG

MECHANICAL



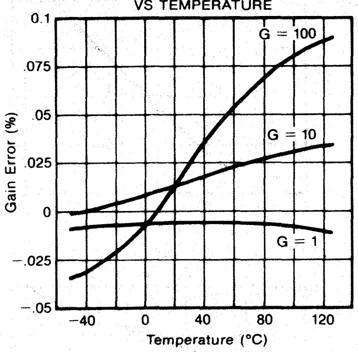
NOTE: Leads in true position within 0.10" (0.25mm) R at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

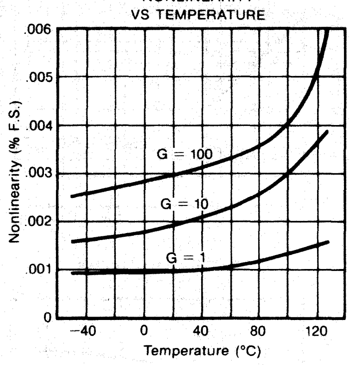
TYPICAL PERFORMANCE CURVES

$T_A = 25°C$, $\pm V_{CC} = 15VDC$ unless otherwise noted.

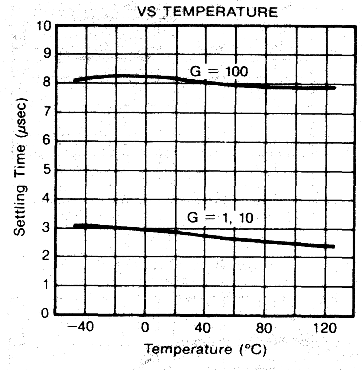
GAIN ERROR VS TEMPERATURE



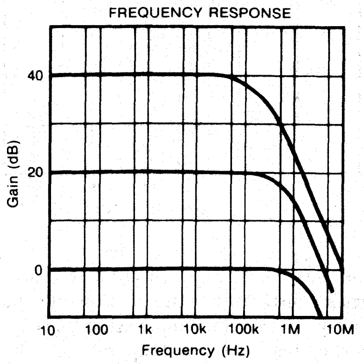
NONLINEARITY VS TEMPERATURE



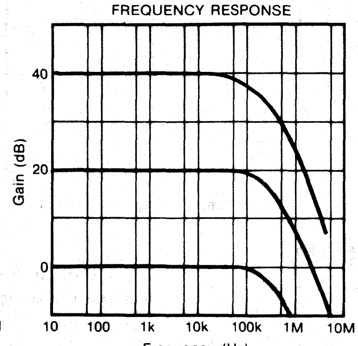
SETTLING TIME VS TEMPERATURE



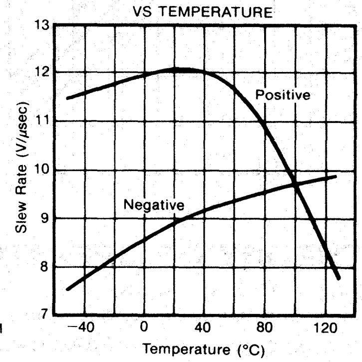
SMALL SIGNAL FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



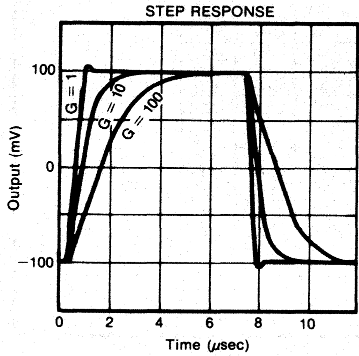
SLEW RATE VS TEMPERATURE



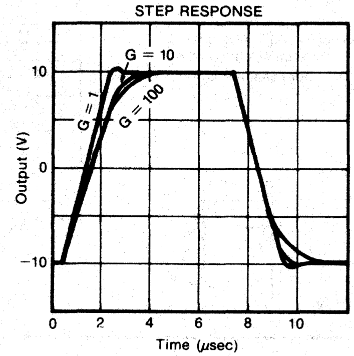
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = 25°C$, $\pm V_{CC} = 15VDC$ unless otherwise noted.

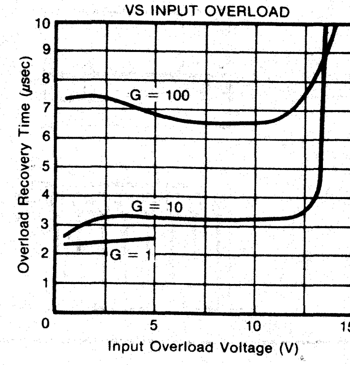
SMALL SIGNAL STEP RESPONSE



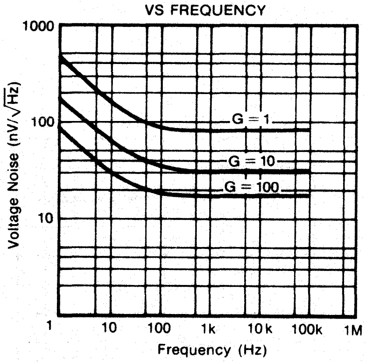
LARGE SIGNAL STEP RESPONSE



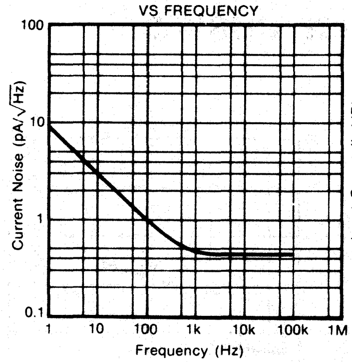
OVERLOAD RECOVERY VS INPUT OVERLOAD



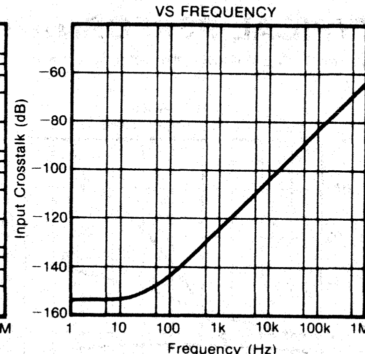
INPUT VOLTAGE NOISE VS FREQUENCY



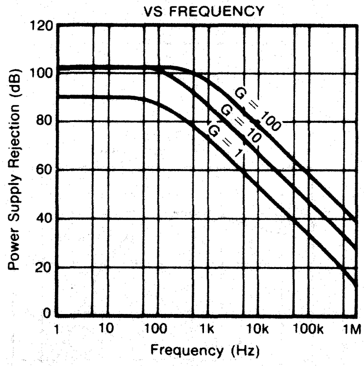
INPUT CURRENT NOISE VS FREQUENCY



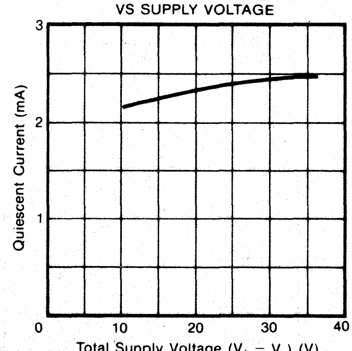
INPUT CROSSTALK VS FREQUENCY



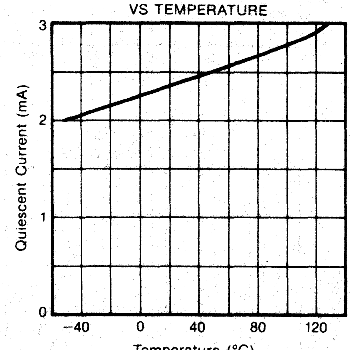
POWER SUPPLY REJECTION VS FREQUENCY



QUIESCENT CURRENT VS SUPPLY VOLTAGE



QUIESCENT CURRENT VS TEMPERATURE



THEORY OF OPERATION

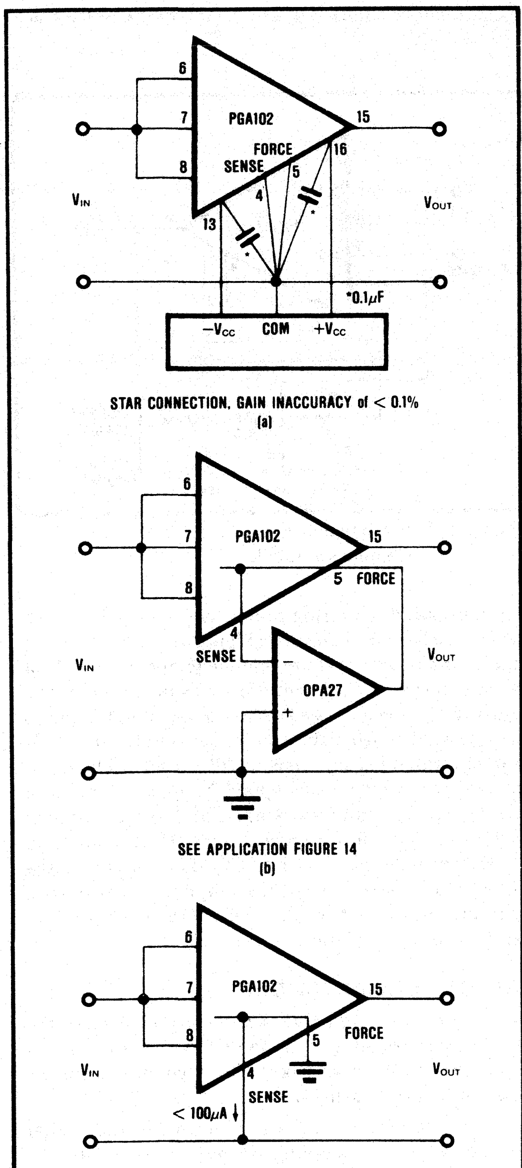
The PGA102 is a self-contained programmable-gain amplifier with digitally selectable gains of 1, 10, and 100.

A block diagram of the PGA102 is shown on the first page of this data sheet. The circuit contains three sections: (1) 3-channel switchable-input operational amplifier, (2) precision thin-film resistor network (R_1–R_6), and (3) gain/channel select digital circuit.

Under control of the channel select circuitry, only one input stage (A_1, A_2, or A_3) is active at any time. The selected input stage steers input signals (V_{IN1}, V_{IN2}, or V_{IN3}) to the output amplifier (A_4). At this time the unselected input stages are turned off by deactivation of their internal bias circuitry. Three different precision gains are produced by closing the feedback loop through the selected input stage. This unique feature of having each channel set to a specific gain allows the user more flexibility in applications. Low gain drift is achieved by the excellent tracking of the thin-film gain set resistors. The "trip point" on select pins 1 and 2 for changing channels, and hence gain, is set by the logic threshold control voltage on pin 3.

INSTALLATION AND OPERATING INSTRUCTIONS

Figure 1 shows proper power supply and signal connections. The supplies should be decoupled with 0.1μF capacitors as close to the package as possible. To avoid gain errors, connect ground as indicated, being sure to minimize ground resistance. The PGA102 has a separate ground force and ground sense which virtually eliminate gain errors due to resistance in the common line. The gain error results from any resistance added in series with the internal junction of R_1, R_4, and R_5. Internally, wire bond resistance of 0.2Ω can cause a 0.02% error for gain of 10 and 0.2% error for gain of 100. By minimizing the current in the sense line, specified performance is achievable.



STAR CONNECTION, GAIN INACCURACY of $< 0.1\%$
(a)

SEE APPLICATION FIGURE 14
(b)

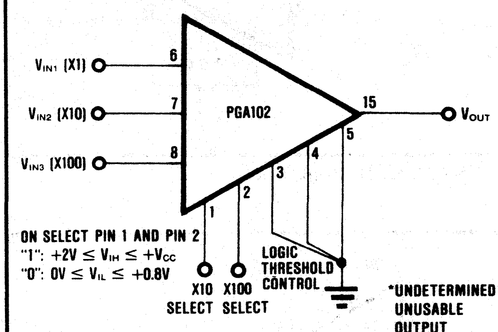
SEE APPLICATION FIGURES 9 AND 10
(c)

(b) AND (c) ELIMINATE GAIN ERRORS DUE TO RESISTANCE OF THE INTERNAL WIRE BOND (INACCURACY $< 0.05\%$).

FIGURE 1. Power Supply and Signal Connections.

GAIN/CHANNEL SELECTION

Gain is chosen by digitally manipulating the voltage level on the X10 and X100 select pins as shown in Figure 2. The table in Figure 2 shows how to select a specific channel which has a gain of 1, 10, or 100. In this circuit, the logic threshold control has been grounded to give compatibility with TTL levels. However, this threshold can be set anywhere between [$-V_{CC} + 4V$] and [$+V_{CC} - 2.6V$] for compatibility with other logic such as CMOS.



X10 SELECT	X100 SELECT	CHANNEL 1 GAIN SELECT
0	0	V_{IN1} (X1)
0	1	V_{IN2} (X10)
1	0	V_{IN3} (X100)
1	1	ILLEGAL*

FIGURE 2. Channel Selection for Ground-Referenced Logic Threshold (TTL-compatible).

In general, the logic state is determined by the voltage on pin 1 or pin 2 relative to the threshold control voltage on pin 3. The input high (V_{IH}) and low (V_{IL}) voltages to switch states are shown below:

Logic one, "1": $(V_{LTC} + 2V) < V_{IH} < +V_{CC}$

Logic zero, "0": $(V_{LTC} - 5.6) < V_{IL} < (V_{LTC} + 0.8V)$

An external decoder and latch on the select lines may be added for operation in computer-controlled analog input/output systems.

OPTIONAL OFFSET ADJUSTMENT

The input offset voltage is laser trimmed and will not require user adjustment for most applications. However, pins 11 and 12 may be used to adjust the offset of the active channel to zero as shown in Figure 3. This also affects the inactive channels (all offsets move as the potentiometer is adjusted). By compromising, the user can adjust for the average offset of all three channels using one potentiometer; or a compromise for just the X10 and X100 channels can be made, considering the unity gain channel's offset is insignificant for high-level inputs.

Figure 4 shows another approach to offset adjustment. An inexpensive CMOS switch (4016) may be used to independently connect the wipers of three potentiometers to $-V_{CC}$. Therefore, R_1, R_2, and R_3 adjust the offset of channels 1, 2, and 3 respectively.

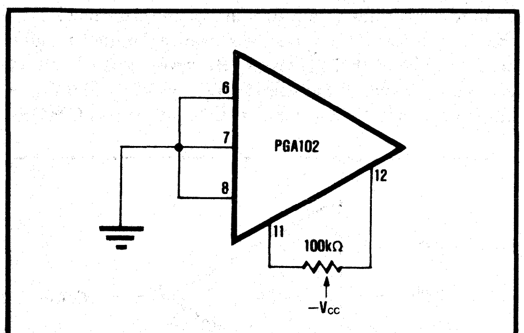


FIGURE 3. Offset Adjustment.

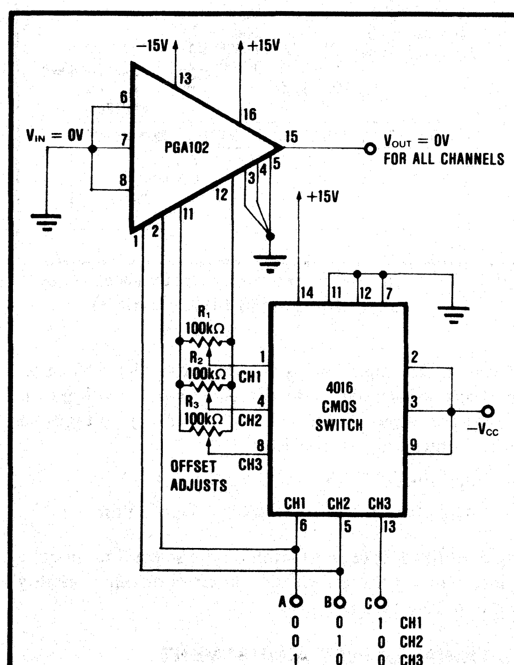


FIGURE 4. Independent Offset Adjustment of Channels 1, 2, and 3.

OPTIONAL GAIN ADJUSTMENT

The initial gain accuracy has been internally laser trimmed to high precision, but can be adjusted. Figure 5 shows independent fine-gain adjustment of channels 2 and 3. This involves either paralleling the internal input resistors for gain up or the internal feedback resistors for gain down. External resistors R_2, R_3, R_5, and R_6 are chosen to trade off range and resolution. Channel 1's gain cannot be adjusted due to the internal zero feedback resistance.

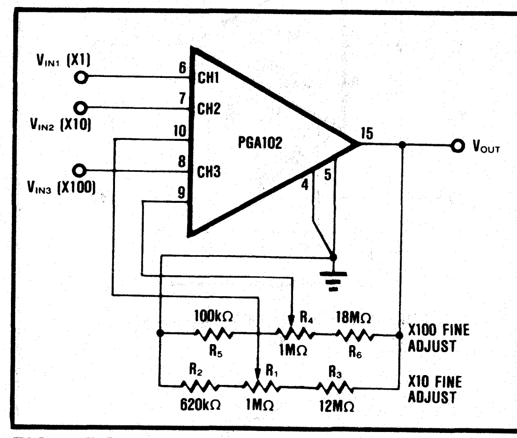


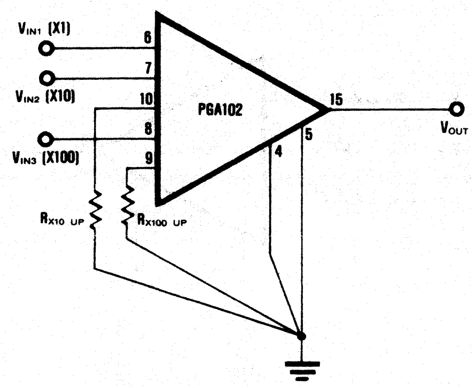
FIGURE 5. Independent Fine Gain Adjustment of Channels 2 and 3.

For applications requiring gains other than 1, 10, or 100, the PGA102 can be gained up (Figure 6) or down (Figure 7). It is important to realize that the temperature drift of the external gain adjustment resistors will affect the total gain drift. This becomes more predominant as the gain is changed further from the factory-set specification. For example, with small adjustments (20% or so), a 30ppm/°C external resistor will add 6ppm/°C to the 10ppm/°C internal resistor ratio tracking. For large adjustment (50% or so), the effect becomes larger. The best that can be achieved is 25ppm/°C (the TCR of one internal resistor) when the external resistor has 0ppm/°C. Also when adjusting the X10 channel, keep the gain above 5 to assure frequency stability.

LAYOUT CONSIDERATIONS

Proper attention to layout is necessary to achieve the specified performance of the PG102. Major goals are to reduce crosstalk, noise pickup, noise coupled from the power supply, and gain errors.

Be certain to separate the runs for analog and digital grounds to avoid coupling of digital transients. To reduce gain errors, connect analog grounds with a ground plane or a low resistance star configuration. Properly using the PGA102 ground force and sense (see Figure 1) assures the best performance, especially in high gains.

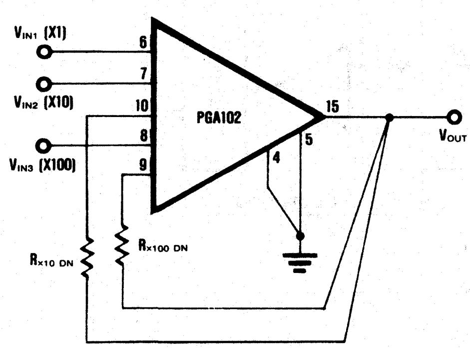


$$R_{x10\ UP} \approx \frac{10.8k\Omega}{G_{x10\ UP} - 10}$$

$$R_{x100\ UP} \approx \frac{108k\Omega}{G_{x100\ UP} - 100}$$

Example:
$R_{x10\ UP} \approx 1.08k\Omega$ and $R_{x100\ UP} \approx 1.08k\Omega$
Gives gains of 1, 20, 200

FIGURE 6. Gain Up Control.



$$R_{x10\ DN} \approx -\left(\frac{97.2k\Omega}{G_{x10\ DN} - 10} + 10.8k\Omega\right)$$

$$R_{x100\ DN} \approx 100\left(\frac{108k\Omega}{100 - G_{x100\ DN}} - 1.09k\Omega\right)$$

Example:
$R_{x10\ DN} \approx 8.64k\Omega$ and $R_{x100\ DN} \approx 107k\Omega$
Gives gains of 1, 5, 50

FIGURE 7. Gain Down Control.

CROSSTALK

Crosstalk expresses the signal feedthrough from an OFF channel that appears at the active input. It is expressed in dB, which translates to a percent of the input signal applied to the OFF channel. Crosstalk increases with increasing frequency (see Typical Performance Curve). Best performance is achieved by keeping input lines short and band limiting if possible.

SETTLING TIME

The PGA102 is designed for applications requiring fast settling. Settling time is the time required, after the onset of a step input signal, for the output voltage to settle and remain within a specified error band around the final value. It is very important because it limits maximum channel scanning or throughput rate in multiplexed systems. Since the error increases with source resistance, keep sources $< 10k\Omega$ for best results.

INPUT OVERLOAD RECOVERY

Another important parameter in data acquisition systems is overload recovery, especially when high gain is selected. The PGA102's fast recovery limits delays in capturing input signals in the presence of large transients. Best results are obtained by clamping input overvoltages to less than 13V (see Typical Performance Curve).

TYPICAL APPLICATIONS

The PGA102 is ideal for auto-gain-ranging systems with many multiplexed input channels that must be scanned quickly. Its high gain accuracy and low temperature drift permit application where computer error correction is not available. In other cases, the PGA102 provides an inexpensive precision fixed gain block requiring no precision external components. An external decoder and latch allow the user flexibility to configure the system as desired. Figures 8 through 15 show application circuits.

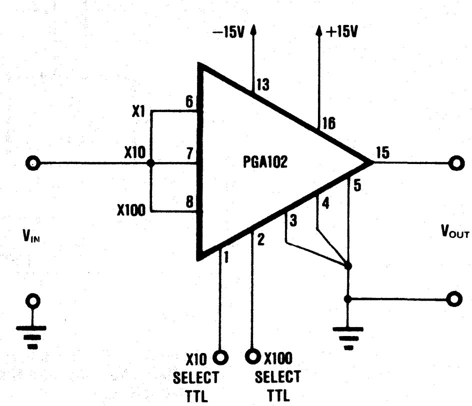


FIGURE 8. Fast Settling Programmable-Gain Amplifier (Gain = 1, 10, 100).

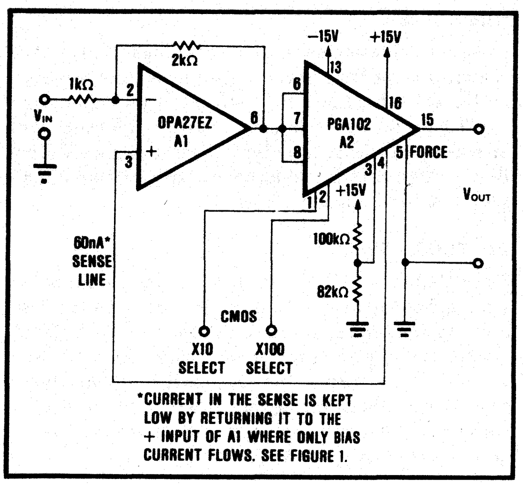


FIGURE 9. Fast-Settling Programmable-Gain Amplifier (Gain = 2, 20, 200).

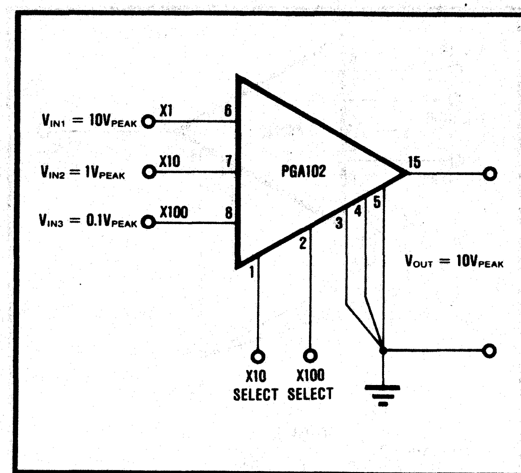


FIGURE 10. Three-Channel Separate Gain Amplifier.

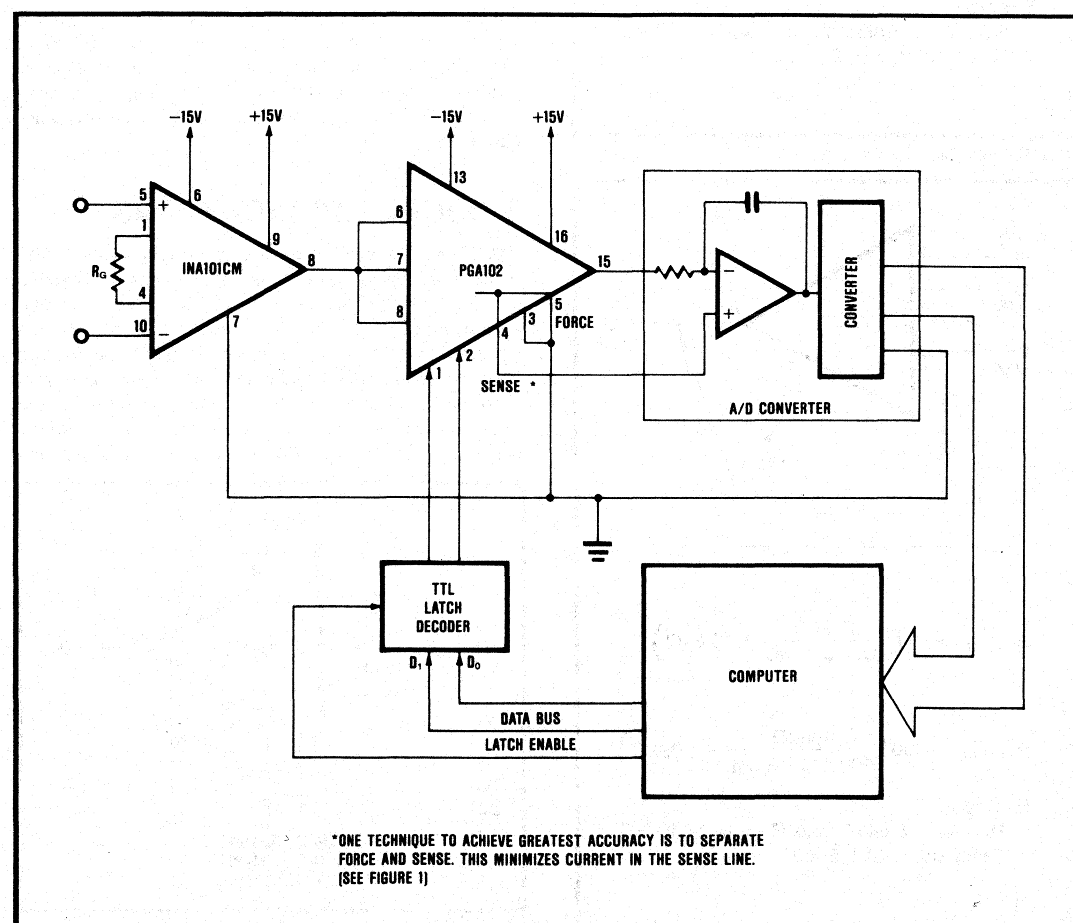


FIGURE 11. Auto-Gain Ranging Instrumentation Amplifier for Data Acquisition.

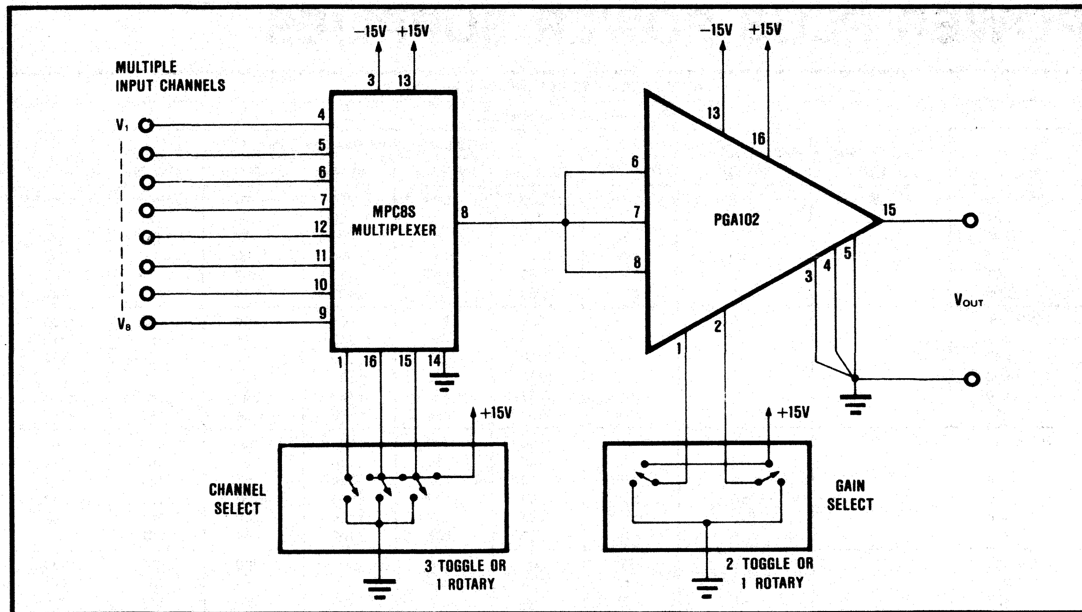


FIGURE 12. Manually Controlled Gain-Ranging Amplifier for Portable Test Equipment.

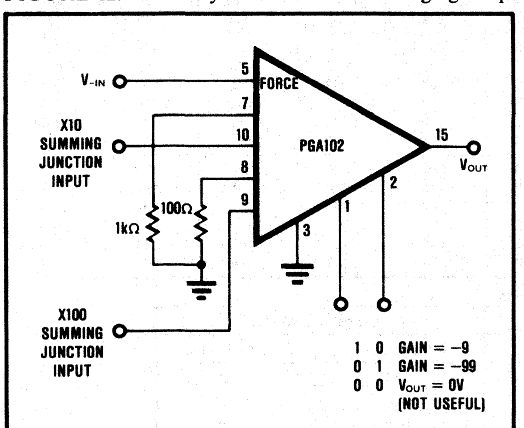


FIGURE 13. Inverting Programmable Amplifier. Summing Junctions Can Be Used for Offsetting.

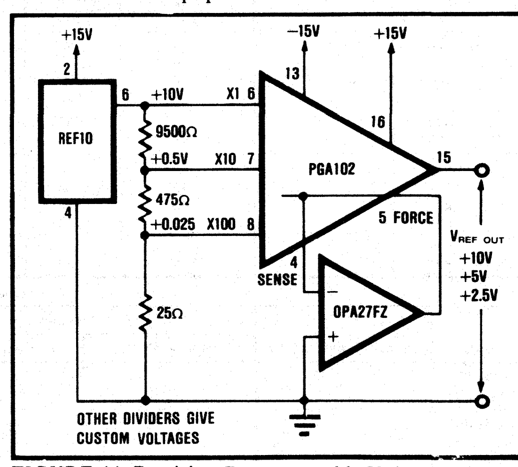


FIGURE 14. Precision Programmable Voltage Reference.

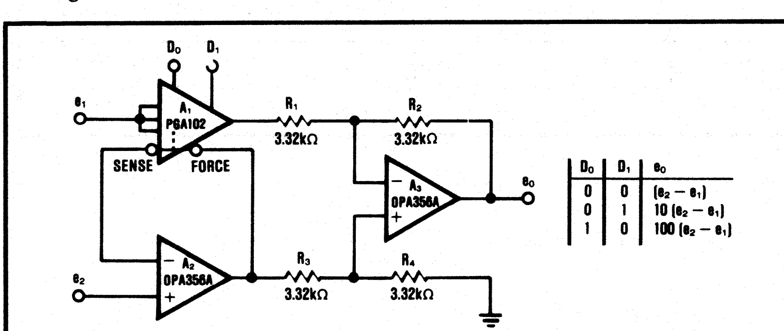


FIGURE 15. Fast Instrumentation Amplifier.

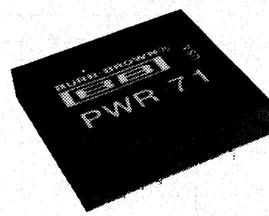
POWER PLUS POWER SUPPLIES

•POWER PLUS SERIES (all new products)									
Single or Dual Output									
Model	Input Voltage (VDC)	Output Voltage (VDC)	Output Current (mA) by Series Type						
			PWR 1xx	PWR 2xx	PWR 3xx	PWR 4xx	PWR 5xx	PWR 6xx	PWR 7xx
PWR x00	5	5	90	300	200	600	200	400	1000
x01		12	38	125	84	250	84	167	417
x02		15	30	100	67	200	67	134	334
x03		±5	±45	±150	±100	±300	±100	±200	±500
x04		±12	±19	±63	±42	±125	±42	±84	±209
x05		±15	±15	±50	±34	±100	±34	±67	±167
PWR x06	12	5	90	300	200	600	200	400	1000
x07		12	38	125	84	250	84	167	417
x08		15	30	100	67	200	67	134	334
x09		±5	±45	±150	±100	±300	±100	±200	±500
x10		±12	±19	±63	±42	±125	±42	±84	±209
x11		±15	±15	±50	±34	±100	±34	±67	±167
PWR x12	15	5	90	300	200	600	200	400	1000
x13		12	38	125	84	250	84	167	417
x14		15	30	100	67	200	67	134	334
x15		±5	±45	±150	±100	±300	±100	±200	±500
x16		±12	±19	±63	±42	±125	±42	±84	±209
x17		±15	±15	±50	±34	±100	±34	±67	±167
PWR x18	24	5	90	300	200	600	200	400	1000
x19		12	38	125	84	250	84	167	417
x20		15	30	100	67	200	67	134	334
x21		±5	±45	±150	±100	±300	±100	±200	±500
x22		±12	±19	±63	±42	±125	±42	±84	±209
x23		±15	±15	±50	±34	±100	±34	±67	±167
PWR x24	28	5	90	300	200	600	200	400	1000
x25		12	38	125	84	250	84	167	417
x26		15	30	100	67	200	67	134	334
x27		±5	±45	±150	±100	±300	±100	±200	±500
x28		±12	±19	±63	±42	±125	±42	±84	±209
x29		±15	±15	±50	±34	±100	±34	±67	±167
PWR x30	48	5	90	300	200	600	200	400	1000
x31		12	38	125	84	250	84	167	417
x32		15	30	100	67	200	67	134	334
x33		±5	±45	±150	±100	±300	±100	±200	±500
x34		±12	±19	±63	±42	±125	±42	±84	±209
x35		±15	±15	±50	±34	±100	±34	±67	±167

Triple Output					
Model	Input Voltage (VDC)	Output Channel 1		Output Channel 2	
		Voltage (VDC)	Current (mA)	Voltage (VDC)	Current (mA)
PWR 800 PWR 801	5	5	250	±12 ±15	±156 ±125
PWR 802 PWR 803	12	5	250	±12 ±15	±156 ±125
PWR 804 PWR 805	15	5	250	±12 ±15	±156 ±125
PWR 806 PWR 807	24	5	250	±12 ±15	±156 ±125
PWR 808 PWR 809	28	5	250	±12 ±15	±156 ±125
PWR 810 PWR 811	48	5	250	±12 ±15	±156 ±125

BURR-BROWN®

PWR71



ISOLATED DC/DC CONVERTER
Four Isolated Channels - Dual, Unregulated Outputs
3 WATTS RATED OUTPUT POWER

FEATURES

- TESTED IN COMPLIANCE WITH UL544
- OUTPUT POWER TO 3 WATTS
- HIGH ISOLATION VOLTAGE 1000V_{PEAK}
- SIX-SIDED SHIELDING
- INPUT AND OUTPUT FILTERING
- LOW PROFILE PACKAGE 0.4" HIGH

APPLICATIONS

- SPOT REGULATOR
- POWER FOR DATA ACQUISITION, OP AMPS, ETC.
- PROCESS CONTROL
- PORTABLE EQUIPMENT
- TEST EQUIPMENT

DESCRIPTION

The PWR71 is a four-channel, dual-output, unregulated DC/DC converter designed for general purpose power conversion applications where high efficiency is more important than load regulation.

The PWR71 has four isolated plus and minus output voltages approximately equal to the magnitude of the input voltage. It operates over an input voltage range of 10VDC to 18VDC. Rated output current for the PWR71 is 25mA per output or a total of 200mA for all outputs.

Isolation voltage between the input and any of the four output circuits is 1000V_{PK} continuous. This same isolation specification applies between any of the four dual outputs.

A continuous connection between an output and its common will not damage the PWR71. Short circuit protection is accomplished by using power MOSFETs in the PWR71 input circuitry.

Six-sided shielding suppresses electromagnetic radiation which could disturb sensitive analog measurements or interfere with system timing signals. Filtering the PWR71 input and outputs minimizes the effects of electrical noise on the source and loads of the converter.

Each PWR71 is tested in compliance with UL544, VDE750, and CSA C22.2 dielectric withstand specifications. In addition, barrier leakage current is 100% tested.

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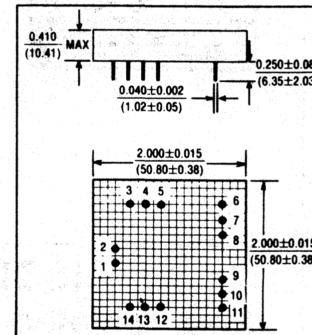
SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{IN}$ = 15VDC, and I_{OUT} = ±25mA unless otherwise noted.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
INPUT					
Rated Voltage			15		VDC
Voltage Range		10		18	VDC
Input Current	I_{LOAD} = 0		50		mA
	I_{LOAD} = Rated Load		280	375	mA
Ripple Current	I_{LOAD} = 0		30		mA, pk
	I_{LOAD} = Rated Load		80		mA, p-p
ISOLATION	Ratings apply input-to-output and channel-to-channel				
Rated Voltage	60 sec, 60 Hz, 3000 V_{PK}	1000			VDC
Resistance			10G		Ω
Capacitance			10		pF
Leakage Current	V_{ISO} = 240VAC, 60Hz			3	μA
OUTPUT					
Rated Voltage			±15		VDC
Voltage Range	I_{OUT} = No Load	±15		±18	VDC
	I_{OUT} = Rated Load	±14.25		±15.75	VDC
Rated Power		3			Watts
Rated Current	Each output	±25			mA
	Total of all outputs	200			mA
Current Range	Each output	0		+40	mA
	Total of all outputs	0		500	mA
Line Reguation	10VDC ≥ V_{IN} ≥ 18VDC		1.08		V/V
Load Regulation	0mA ≥ I_{LOAD} ≥ 25mA		35		mV/mA
Ripple Voltage	I_{LOAD} = 0		±10		mV, pk
	I_{LOAD} = Rated Load			±100	mV, pk
TEMPERATURE					
Specification		-25		+85	°C
Operating		-40		+100	°C
Storage		-55		+125	°C

MECHANICAL



NOTES:

All dimensions are in inches (millimeters).

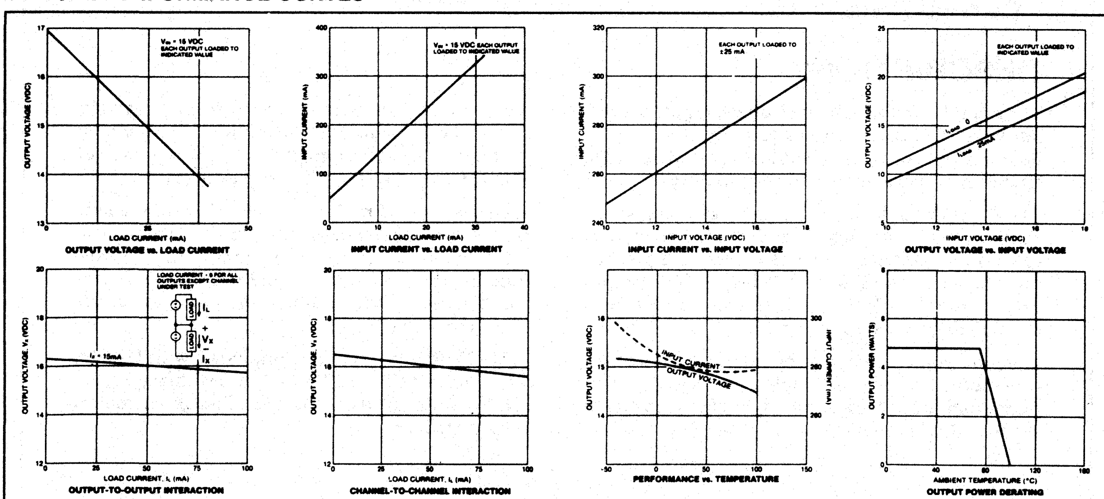
GRID: 0.100 inches (2.54 millimeters)

MATERIAL: Low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range and good electrical properties under high humidity environments. Lead material is brass with a hot solder dipped surface to allow ease of solderability.

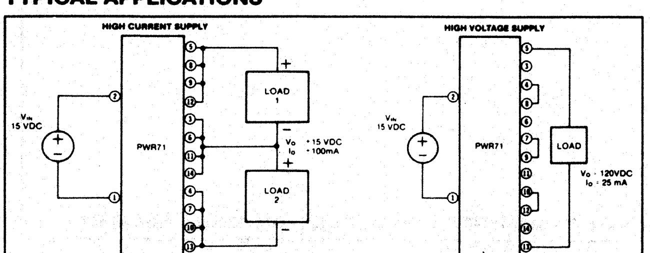
ABSOLUTE MAXIMUM RATINGS

Input Voltage	18VDC
Output Current	500 mA
Output Short-Circuit Duration	Continuous

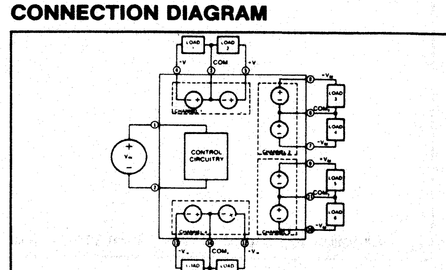
TYPICAL PERFORMANCE CURVES



TYPICAL APPLICATIONS

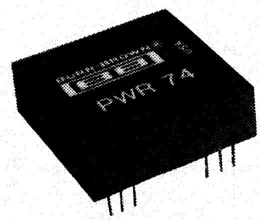


CONNECTION DIAGRAM



BURR-BROWN®

PWR74



ISOLATED DC/DC CONVERTER
Two Isolated Channels - Dual, Unregulated Outputs
OUTPUT POWER TO 3 WATTS

FEATURES

- TESTED IN COMPLIANCE WITH UL544
- OUTPUT POWER TO 3 WATTS
- HIGH ISOLATION VOLTAGE $1500V_{PEAK}$
- SIX-SIDED SHIELDING
- INPUT AND OUTPUT FILTERING
- LOW PROFILE PACKAGE 0.4" HIGH

APPLICATIONS

- SPOT REGULATOR
- POWER FOR DATA ACQUISITION, OP AMPS, ETC.
- PROCESS CONTROL
- PORTABLE EQUIPMENT
- TEST EQUIPMENT

DESCRIPTION

The PWR74 is a two-channel, dual-output DC/DC converter designed for general purpose power conversion applications where high efficiency is more important than load regulation.

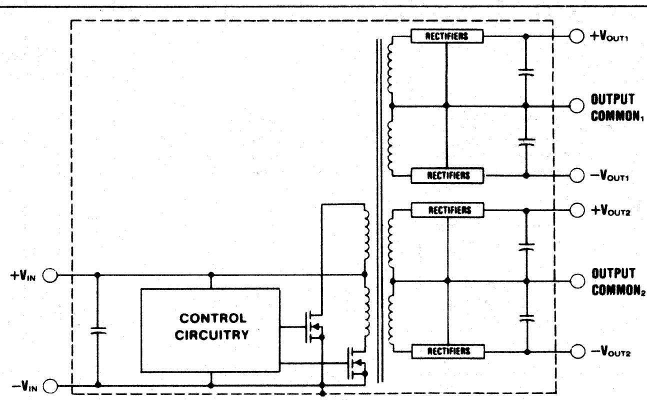
The PWR74 provides two isolated plus and minus output voltages approximately equal to the input voltage magnitude. It operates over an input voltage range of 10VDC to 20VDC. Isolation voltage is a minimum of 1500 V_{PK}.

Six-sided shielding suppresses electromagnetic radiation which could disturb sensitive analog measurements or interfere with system timing signals. Input filtering minimizes reflected ripple current. Output ripple voltage and switching transients are reduced by filtering the PWR74 outputs.

Momentarily connecting an output pin to its output common will not damage the PWR74. Short-circuit protection is accomplished by using power MOSFETs in the PWR74's input circuitry.

The PWR74 is tested in compliance with UL544 dielectric withstand voltage requirements for primary circuits.

SIMPLIFIED CIRCUIT DIAGRAM



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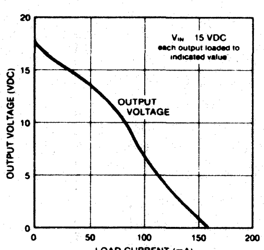
SPECIFICATIONS

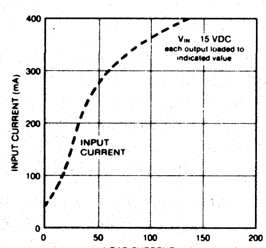
ELECTRICAL

At T_A = +25°C, $+V_{IN}$ = 15VDC, and I_{OUT} = ±25mA unless otherwise noted.

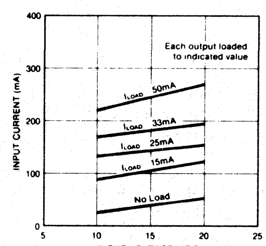
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Rated Voltage			15		VDC
Voltage Range		10		20	VDC
Input Current	I_{OUT} = No Load		55	75	mA
	I_{OUT} = Rated Load		155	175	mA
Ripple Current	I_{OUT} = No Load		80		mA, p.p
	I_{OUT} = Rated Load		100		mA, p.p
ISOLATION	Ratings apply input-to-output and channel-to-channel				
Rated Voltage	60 sec, 60 Hz, 4000 V_{PK}	1500			V_{PK}
Resistance			10G		Ω
Capacitance			12		pF
Leakage Current	V_{ISO} = 240VAC, 60Hz			2	μA
OUTPUT					
Rated Voltage	-25°C ≤ T_A ≤ +85°C		±15		VDC
Voltage Accuracy				5	%
Rated Current	-25°C ≤ T_A ≤ +85°C		±25		mA
Current Range		0		±50	mA
Line Regulation	10VDC ≥ V_{IN} ≥ 20VDC		1.15		V/V
Load Regulation	±5mA ≥ I_{OUT} ≥ ±25mA		18		mV/mA
Ripple Voltage	I_{OUT} = ≥ No Load		20		mV, p.p
	I_{OUT} = ≥ Rated Load		40	100	mV, p.p
TEMPERATURE					
Specification		-25		+85	°C
Operating		-55		+125	°C
Storage		-65		+150	°C



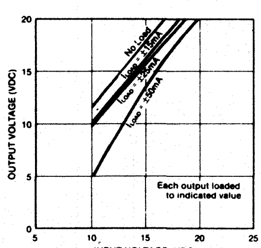
OUTPUT VOLTAGE vs. LOAD CURRENT



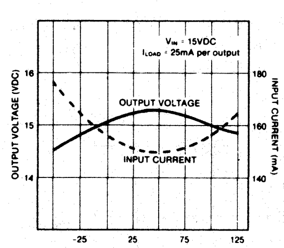
INPUT CURRENT vs. LOAD CURRENT



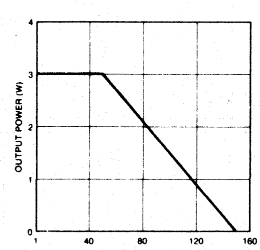
INPUT CURRENT vs. INPUT VOLTAGE



OUTPUT VOLTAGE vs. INPUT VOLTAGE



PERFORMANCE vs. TEMPERATURE

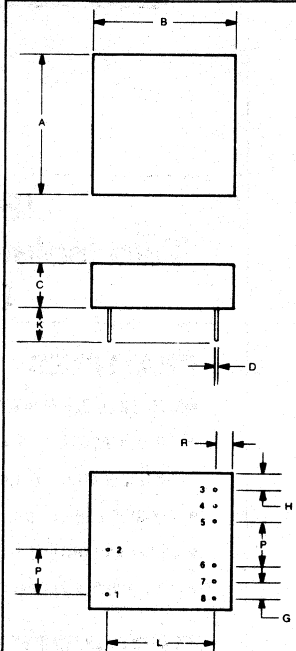


OUTPUT POWER DERATING

ABSOLUTE MAXIMUM RATINGS

Input Voltage 20VDC
Output Current .... ±100mA
Output Short-Circuit Duration .... 45 Seconds

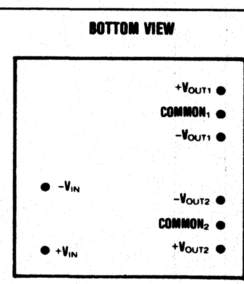
MECHANICAL



DIM.	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.075	1.175	27.31	29.85
B	1.075	1.175	27.31	29.85
C	.350	.420	8.89	10.67
D	.018	.022	0.46	0.56
G	.100 BASIC		2.54 BASIC	
H	.085	.175	2.16	4.45
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
P	.500 BASIC		12.7 BASIC	
R	.085	.175	2.16	4.45

Material: Black Epoxy
Weight: 15 gm. (0.53 oz.)
Grid: 2.50mm (0.10")

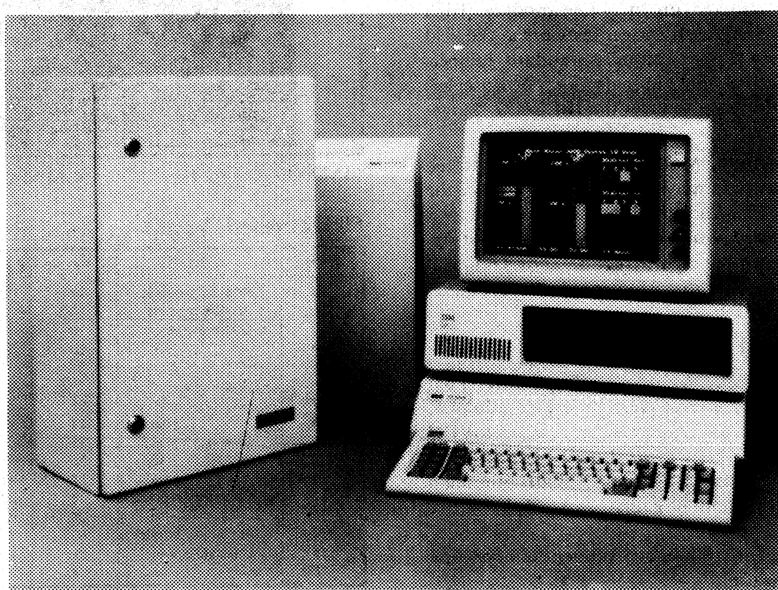
CONNECTION DIAGRAM



SCADAR SERIES 10

Supervisory Control and Data Acquisition Remote

SCADAR Series 10 is a compact, rugged supervisory control and data acquisition system for local and remote monitoring and control applications. Intelligent and self-contained, Series 10 is a single-board microcomputer system complete with CPU, memory, power supply, and I/O. It is easily interfaced to any host computer through standard communications techniques, and is ideal for remote monitoring and control installations that require low power. The packaging is designed to allow expansion I/O and intelligence for conditioning I/O via plug-in modules. Field I/O connections are made via screwdriver-locked terminations. Two-piece pluggable terminal blocks integral to the base board and I/O modules allow removal of I/O modules and base board electronics without disturbing field connections. SCADAR Series 10 is available in attractive desk-mount or wall-mount general-purpose housings for control-room applications. Series 10 is also available packaged in NEMA-4 enclosures for use in harsh environments.



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SCADAR Series 10

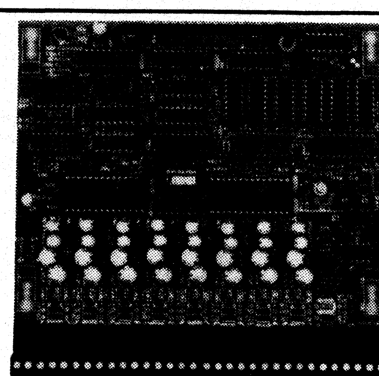
Spec Sheet	MM20-10
Effective	10/15/84
Supersedes	None

ANALOG INPUT MODULE

DESCRIPTION

MM20-10 is a MOS-multiplexed analog (input only) module. Eight differential channels are provided, each with a detection range of ±10VDC and overvoltage protection to ±16VDC. Analog inputs are auto-zeroed to correct for input zero drift. All channels include auto-ranging which allows high level inputs (1-5VDC, 4-20mADC) and low level inputs (mV, RTD, thermocouple), to be intermixed on the same module. High level current inputs require turnover resistors at the field terminations. Sensor "fail-detection" is standard; jumper-selects provide full action "upscale" or "downscale". Input circuitry is designed to meet the IEEE-472 "surge-withstand" specifications.

MM20-10 Analog Input Modules self-configure to the Series 10 baseboard and may be installed at any of the four module positions. Each module is fitted with a two-piece pluggable terminal block and header for field signal interface. The two-piece construction allows removal of input modules without disturbing field connections.



MM20-10 Analog Input/Output Module.

FIELD PINOUTS

Pin No.	Use	Pin No.	Use
1	Analog ground	17	Channel 5 shield
2	Analog ground	18	Channel 6 + in
3	Channel 1 + in	19	− in
4	− in	20	shield
5	shield	21	Channel 7 + in
6	Channel 2 + in	22	− in
7	− in	23	shield
8	shield	24	Channel 8 + in
9	Channel 3 + in	25	− in
10	− in	26	shield
11	shield	27	Unused
12	Channel 4 + in	28	Unused
13	− in	29	Unused
14	shield	30	Unused
15	Channel 5 + in	31	Unused
16	− in	32	Unused

SPECIFICATIONS

Number of inputs .... Eight differential
Input signal range .... ±10VDC
Max input voltage .... ±16VDC
Input filter .... 2-pole, 60dB at 60Hz
Common-mode rejection .... 80dB minimum
Programmable-gain amplifier gains 1, 8, 64, 512
Thermocouple
compensator......... On-board ambient temperature sensor for compensation
Accuracy at +25°C .... 0.2% full scale range

ORDERING INFORMATION

Specify quantity required and part number MM20-11. Add suffix "L" or "R" to indicate field wiring termination—LOCAL at module or via REMOTE termination assemblies.

BURR-BROWN®

SCADAR Series 10

Spec Sheet MM20-11
Effective 10/15/84
Supersedes None

ANALOG INPUT/OUTPUT MODULE

DESCRIPTION

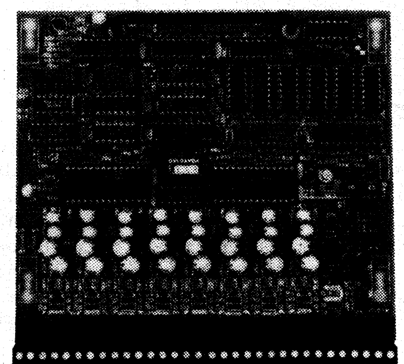
MM20-11 is a MOS-multiplexed analog input/output module. Eight differential (input) channels are provided, each with a detection range of ±10VDC and overvoltage protection to ±16VDC. Analog inputs are auto-zeroed to correct for input zero drift. All channels include auto-ranging, which allows high level inputs (1-VDC, 4m-20mADC) and low level inputs (mV, RTD, thermocouple) to be intermixed on the same module. High level current inputs require turnover resistors at the field terminations. Sensor fail-detection is standard; jumper-selects provide full action "upscale" or "downscale". Input circuitry is designed to meet the IEEE-472 "surge-withstand" specifications.

Two analog output channels are provided, each with 12-bit digital-to-analog converters (DACs) which generate voltage and current outputs. These outputs are scaled at 1-5VDC and 4-20mADC with ±10% overrange and underrange capability. The output circuitry is designed to meet the IEEE-472 surge-withstand specification. A watchdog timer activates upon communication from the baseboard processor to assure "fail-safe" operation of outputs. The "fail-safe" modes are jumpered to provide full upscale, zero scale, or last set value upon timeout of the watchdog.

MM20-11 Analog Input/Output Modules self-configure to the Series 10 baseboard and may be installed at any of the four module positions. Each module is fitted with a two-piece pluggable terminal block and header for field signal interface. The two-piece construction allows removal of input modules without disturbing field connections.

SPECIFICATIONS

Number of inputs	Eight differential
Input signal range	±10VDC
Max input voltage	±16VDC
Input filter	2-pole, 60dB at 60Hz
Common-mode rejection	80dB minimum
Programmable-gain amplifier gains	1, 8, 64, 512
Thermocouple compensator	On-board ambient temperature sensor for compensation
Accuracy at 25°C	0.2% full scale range
Number of outputs	Two voltage or current source
Output resolution	12 bits
Output accuracy	0.2%
Diagnostics	Hardware readback from output stage



MM20-11 Analog Input/Output Module.

FIELD PINOUTS

Pin No.	Use	Pin No.	Use
1	Analog ground	17	Channel 5 shield
2	Analog ground	18	Channel 6 + in
3	Channel 1 + in	19	− in
4	− in	20	shield
5	shield	21	Channel 7 + in
6	Channel 2 + in	22	− in
7	− in	23	shield
8	shield	24	Channel 8 + in
9	Channel 3 + in	25	− in
10	− in	26	shield
11	shield	27	Channel 1 output I/V(1)
12	Channel 4 + in	28	analog ground
13	− in	29	Channel 2 output I/V(1)
14	shield	30	analog ground
15	Channel 5 + in	31	EXTV+(2)
16	− in	32	EXTV− (analog ground)

NOTES: (1) On-board jumper selects I or V output. (2) EXTV+ is used when analog output voltage/current is accomplished from an external source. (Normal power is supplied from the system +12VDC supply.) A jumper change on the MM20-11 module is required to use EXTV+.

ORDERING INFORMATION

Specify quantity required and part number MM20-11. Add suffix "L" or "R" to indicate field wiring terminations—LOCAL at module or via REMOTE termination assemblies.

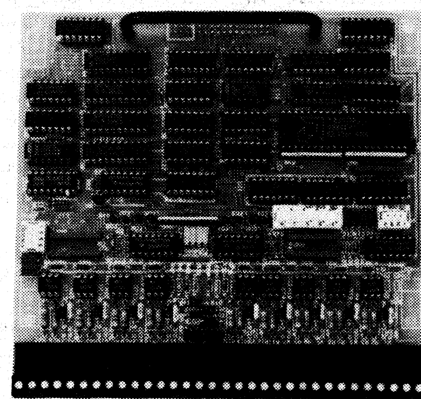
DISCRETE I/O and PULSE INPUT MODULE

DESCRIPTION

MM20-40 Discrete Input/Output and Pulse Input Modules provide a combination of digital inputs, digital outputs, and pulse inputs. These modules self-configure to the Series 10 baseboard and may be installed at any of the four module positions. Each module is fitted with a two-piece pluggable terminal block and header for field signal interface. The two-piece construction allows removal of input modules without disturbing field connections.

Four channels of optically-isolated, contact-debounced circuits are provided for discrete inputs. The contact debounce circuit provides a hardware response to a positive transition of an input (contact closure) within 1msec of its occurrence. A negative transition of the input (contact opening) is sensed after 100msec of occurrence, thereby eliminating false signals due to bouncing of mechanical contacts. The debounce circuit may be disabled by a jumper-select. Discrete inputs are jumper-selectable to respond to low voltage (TTL) or higher voltage (24V) input signals. A 24VDC wetting source is provided for dry contacts. A diagnostic LED is inherent to each channel. The LED is lighted when the field input current is sufficient to indicate a "logic-one" status (opto-isolator turned on). All inputs are protected against surges, short circuits, and reverse polarities of field wiring.

Four channels of discrete outputs are provided by unisolated power transistors capable of sinking up to 400mA. Outputs may be continuous or momentary (software-selectable). A watchdog timer activates upon communications from the baseboard processor to assure "fail-safe" operation of outputs. The "fail-safe" modes are jumpered to allow a high or low impedance state upon timeout of the watchdog. (This selected state is also assumed during system power-up and reset. The hardware is designed with read-backs for each output transistor. One diagnostic LED is provided for each channel. The LED is lighted when the output transistor is ON (low).



MM20-40 Discrete Input/Output and Pulse Input Module

Pulse inputs are accomplished via five channels of optically-isolated, contact-debounce circuits. The contact-debounce circuits are identical to those specified for the discrete inputs. Jumper-selects allow TTL or 24V inputs. A 24V wetting source is provided for dry contacts. All inputs are protected from surges, short circuits, and reverse polarities of field wiring. The pulse circuits may be independently configured via software as frequency or accumulator channels. Maximum frequency is 20kHz. The accumulator software allows incrementation on either the "open" or "close" transitions. Register overflows interrupt the processor system, allowing overflows to be counted and extending accumulation range to 24 bits per channel.

SPECIFICATIONS

Number of discrete inputs .... Four
Input voltage 0–15VDC, 0–80VDC
Reverse polarity protection
  0–15V .... 1.2V clamp at 1A max
  0–80V .... 80VDC continuous
Input impedance
  0–15V .... 470Ω, −1.2V drop
  0–80V .... 7200Ω, −1.2V drop
Channel/channel isolation .... 300V peak
Channel/bus isolation 1200V
(60-second test at 2300V)
Contact debounce
  (selectable on/off).................... 1msec response,
100msec recovery
Contact wetting voltage .... +24VDC
Diagnostics .... LED per channel, ON indicates
presence of field input current
Surge protection .... Designed to meet IEEE-472
surge-withstand specification

Number of Discrete Outputs .... Four
Type of output .... Current sink,
momentary or continuous
Output current rating at +25°C 400mA
  (derate above +25°C) .... 3.33mA/°C
Output voltage rating...................... 80VDC max
Reverse polarity protection ..... 1.2V clamp at 1A max
Diagnostics .... LED per channel,
ON indicates output ON (low).
Hardware readback from output transistor.

Surge Protection.......... Designed to meet IEEE-472
surge-withstand specification

Number of Pulse Inputs .... Five
Accumulator register size................... 24 bits each
Frequency range .... 20kHz max (debounce off)
Input voltage (jumper-selectable) 0–15VDC
or 0–80VDC

Reverse polarity protection
  0–15V .... 1.2V clamp at 1A max
  0–80V .... 80VDC continuous
Input Impedance
  0–15V .... 470Ω, −1.2V drop
  0–80V .... 7200Ω, −1.2V drop
Channel/channel isolation .... 300V peak
Channel/bus isolation 1200V
(60-second test at 2300V)

Contact debounce
  (selectable on/off).................... 1msec response,
100msec recovery
Surge protection .... Designed to meet IEEE-472
surge-withstand specification
Contact wetting voltage (protected)........... +24VDC

FIELD PINOUTS

Pin No.	Use
1	+24V Source(1)
2	+24V Return
3	+24V Return
4	D/I Channel 1 + In(2)
5	− In
6	Channel 2 + In
7	− In
8	Channel 3 + In
9	− In
10	Channel 4 + In
11	− In
12	D/O Channel 1 Output (sink)
13	Return (gnd)
14	Channel 2 Output (sink)
15	Return (gnd)
16	Channel 3 Output (sink)
17	Return (gnd)
18	Channel 4 Output (sink)
19	Return (gnd)
20	P/I Channel 1 + In(2)
21	− In
22	Channel 2 + In
23	− In
24	Channel 3 + In
25	− In
26	Channel 4 + In
27	− In
28	Channel 5 + In
29	− In
30	+24V Return
31	+24V Return
32	+24V Source(1)

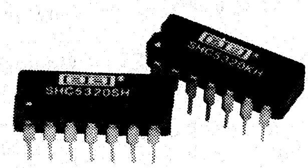
NOTES: (1) +24V output is provided to supply wetting current for the discrete inputs and pulse inputs. This is a current limited, transient protected +24V power supply. (2) All inputs are optically isolated and surge protected.

ORDERING INFORMATION

Specify quantity required and part number MM20-40. Add suffix "L" or "R" to indicate field wiring termination—local at module or via remote termination assemblies.

BURR-BROWN®

SHC5320



High Speed Bipolar Monolithic SAMPLE/HOLD AMPLIFIER

FEATURES

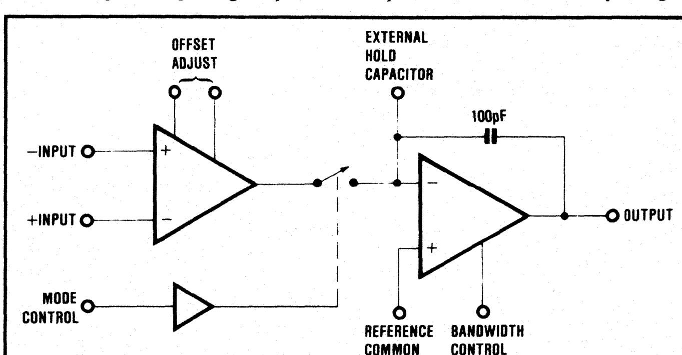
- 1.5μsec max ACQUISITION TIME TO 0.01%
- 250nsec max HOLD MODE SETTLING TIME
- 0.5μV/μsec max DROOP RATE AT +25°C
- TWO TEMPERATURE RANGES:
  0°C to +75°C (KH)
  −55°C to +125°C (SH)
- FULL DIFFERENTIAL INPUTS
- INTERNAL HOLDING CAPACITOR
- 14-PIN CERAMIC DIP PACKAGE

DESCRIPTION

The SHC5320 is a bipolar monolithic sample/hold circuit designed for use in precision high-speed data acquisition applications.

The circuit employs an input tranconductance amplifier capable of providing large amounts of charging current to the holding capacitor, thus enabling fast acquisition times. It also incorporates a low leakage analog switch and an output integrating amplifier with input bias current optimized to assure low droop rates. Since the analog switch always drives into a load at virtual ground, charge injection into the holding capacitor is constant over the entire input voltage range. As a result, the charge offset (pedestal voltage) resulting from this charge injection can be adjusted to zero by use of the offset adjustment capability. The device includes an internal holding capacitor to simplify ease of application; however, provision is also made to add additional external capacitance to improve the output voltage droop rate.

The SHC5320 is manufactured using a dielectric isolation process which minimizes stray capacitance (enabling higher-speed operation), and eliminates latch-up associated with substrate SCRs. The SHC5320KH features fully specified operation over the temperature range of 0°C to +75°C, while the SHC5320SH operates over the temperature range of −55°C to +125°C. The device requires ±15V supplies for operation, and is packaged in a reliable 14-pin ceramic dual-in-line package.



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SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies, gain = +1, and with internal holding capacitor, unless otherwise noted.

MODEL	SHC5320KH			SHC5320SH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
ANALOG							
Voltage Range	±10			•			V
Common-Mode Range	±10			•			V
Input Resistance	1	5		•	•		MΩ
Input Capacitance			3			•	pF
Bias Current		±100	±300		±70	±200	nA
Bias Current Over Temperature Range			±300			±200	nA
Offset Current		±30	±300		•	±100	nA
Offset Current Over Temperature Range			±300			±100	nA
DIGITAL (over temperature range)							
V_{IH} (Logic "1")	2.0			•			V
V_{IL} (Logic "0")			0.8			•	V
I_{IH} (V_I = +5V)			0.1			•	μA
I_{IL} (V_I = 0V)			4			•	μA
Logic "0" = SAMPLE							
Logic "1" = HOLD							
OUTPUT CHARACTERISTICS							
Voltage Range	±10			•			V
Current	±10			•			mA
Output Impedance (Hold Mode)		1			•		Ω
Capacitance Load for Stability		300			•		pF
Noise, DC to 10MHz: Sample Mode		125	200		•	•	μV rms
Hold Mode		125	200		•	•	μV rms
DC ACCURACY/STABILITY							
Gain, Open Loop, DC	3×10^5	2×10^6		10^6	•		V/V
Input Offset Voltage		±0.5			±0.2		mV
Input Offset Voltage Over Temperature Range			±1.5			±2	mV
Input Offset Voltage Drift		±5	±20		•	±15	μV/°C
CMRR(1)	72	90		80	•		dB
Power Supply Rejection(2): $+V_{CC}$	80			•			dB
$-V_{CC}$	65			•			dB
HOLD-TO-SAMPLE MODE DYNAMIC CHARACTERISTICS							
Acquisition Time, A = −1, 10V Step(3):							
to ±0.01%		1	1.5		•	•	μsec
to ±0.1%		0.8	1.2		•	•	μsec
SAMPLE MODE							
Gain-bandwidth Product (Gain = +1)(4):							
C_H = 100pF		2			•		MHz
C_H = 1000pF		180			•		kHz
Full Power Bandwidth(5)		600			•		kHz
Slew Rate(6)		45			•		V/μsec
Rise Time(4)		100			•		nsec
Overshoot(4)		15			•		%
SAMPLE-TO-HOLD MODE DYNAMIC CHARACTERISTICS							
Aperture Time(7)		25			•		nsec
Effective Aperture Time	−50	−25	0	•	•	•	nsec
Aperture Uncertainty (Aperture Jitter)		0.3			•		nsec
Charge Offset (Pedestal)(8) (adjustable to zero)		1			•		mV
Charge Transfer(8)		0.1	0.5		•	•	pC
Sample-to-Hold Transient Settling Time to ±0.01% of FSR		165	250		•	•	nsec
HOLD MODE							
Droop(8)		0.08	0.5		•	•	μV/μsec
Droop at Maximum Temperature		1.2	100		17	•	μV/μsec
Drift Current(8)		8	50		•	•	pA
Drift Current at Maximum Temperature		0.12	10		1.7	•	nA
Feedthrough, 10V p-p, 100kHz sinewave		2			•		mV
POWER SUPPLIES							
$+V_{CC}$	+14.5	+15	+16	•	•	•	V
$-V_{CC}$	−14.5	−15	−16	•	•	•	V
$+I_{CC}$ ($+V_{CC}$ = 15V)(9)		11	13		•	•	mA
$-I_{CC}$ ($-V_{CC}$ = 15V)(9)		−11	−13		•	•	mA

ELECTRICAL (CONT)

MODEL	SHC5320KH			SHC5320SH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TEMPERATURE RANGE							
Specification	0		+75	−55		+125	°C
Storage	−65		+150	*		*	°C
PACKAGE	Hermetic Ceramic			Hermetic Ceramic			
PRICING							
1-24	13.40			61.00			$
25-99	11.60			52.75			$
100-249	9.80			44.70			$

*Specification same as grade to the left.

NOTES: (1) $V_{CM} = \pm 5VDC$. (2) Based on a ±0.5V swing for each supply with all other supplies held constant. (3) $V_O = 10V$ step, $R_L = 2k\Omega$, $C_L = 50pF$. (4) $V_O = 200mV$ p-p, $R_L = 2k\Omega$, $C_L = 50pF$. (5) $V_{IN} = 20V$ p-p, $R_L = 2k\Omega$, $C_L = 50pF$, unattenuated output. (6) $V_O = 20V$ step, $R_L = 2k\Omega$, $C_L = 50pF$. (7) Simulated only, not tested. (8) $V_{IN} = 0V$, $V_{IH} = +3.5V$, $t_R < 20nsec$ (V_{IL} to V_{IH}). (9) Specified for zero differential input voltage between pins 1 and 2. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±28mA average at 20V differential.

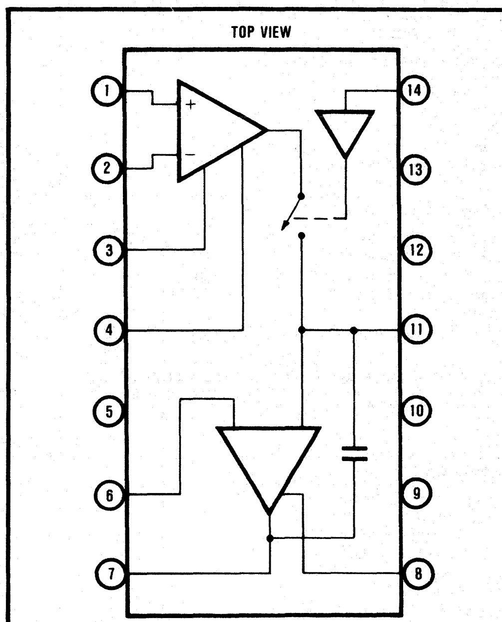
ABSOLUTE MAXIMUM RATINGS[1]

Voltage Between $+V_{CC}$ and $-V_{CC}$ Terminals	40V
Input Voltage	Actual Supply Voltage
Differential Input Voltage	±24V
Digital Input Voltage	+8V, −15V
Output Current, continuous[2]	±20mA
Internal Power Dissipation	450mW
Storage Temperature Range	$-65°C < T_A < +150°C$
Output Short-circuit Duration[3]	Momentary to Common
Lead Temperature (soldering, 10 seconds)	300°C

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

NOTES: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. (2) Internal power dissipation may limit output current to less than +20mA (3) **WARNING: This device cannot withstand even a momentary short circuit to either supply.**

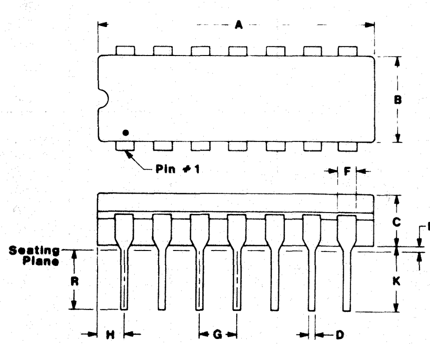
CONNECTION DIAGRAM



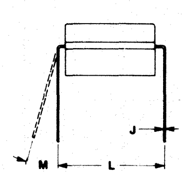
PIN ASSIGNMENTS

Pin		Pin	
Pin 1	−Input	14	Mode Control
2	+Input	13	Supply Common
3	Offset Adjust	12	NC
4	Offset Adjust	11	External Hold Capacitor
5	$-V_{CC}$	10	NC
6	Reference Common	9	$+V_{CC}$
7	Output	8	Bandwidth Control

MECHANICAL



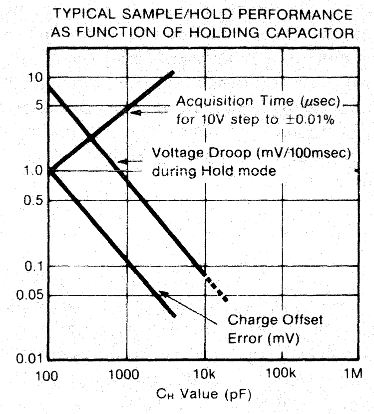
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

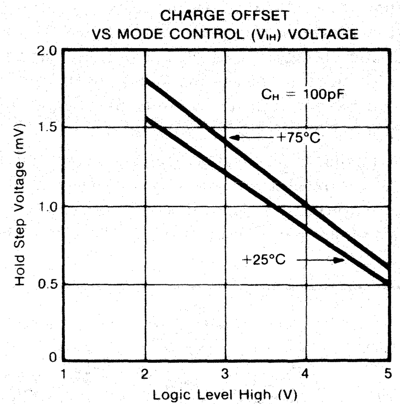


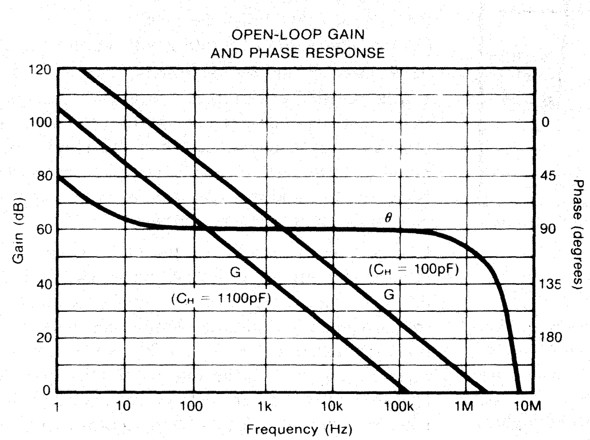
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	.790	-	20.07
B	.220	.310	5.59	7.87
C	-	.185	-	4.70
D	.014	.023	0.36	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	-	.098	-	2.49
J	.008	.012	0.20	0.30
K	.140	.260	3.56	6.60
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52
R	.125	.200	3.18	5.08

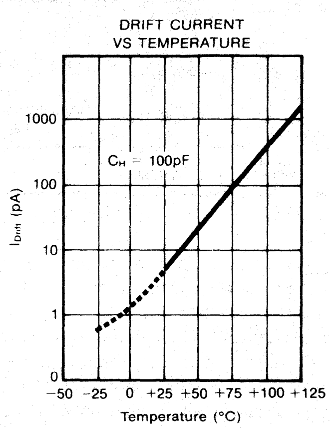
TYPICAL PERFORMANCE CURVES

±V_{CC} = 15V.









DISCUSSION OF SPECIFICATIONS

WHAT IS A SAMPLE/HOLD AMPLIFIER?

A sample/hold amplifier (also sometimes called a track-and-hold amplifier) is a circuit that captures and holds an analog voltage at a specific point in time under control of an external circuit, such as a microprocessor. This type of circuit has many applications; however, its primary use is in data acquisition systems which require that the voltage be captured and held during the analog-to-digital conversion process. Use of a sample/hold effectively increases the bandwidth of a data acquisition system by a significant amount. For further discussion of this capability, refer to "Signal Digitization" in the Applications section of this data sheet.

The ideal sample/hold amplifier in its simplest form contains four primary components as illustrated in Figure 1, although in actual practice they may not be internally connected exactly as shown. Amplifier A_1, the input buffer, provides a high impedance load to the source circuit and supplies charging current to the holding capacitor C_H. Switch S_1 opens and closes under external control to gate the buffered input signal to the holding circuit or to remove it so that the most recently sampled signal will be held. Amplifier A_2 serves to present a high impedance load to the holding capacitor and to provide a low impedance voltage source for external loads. A

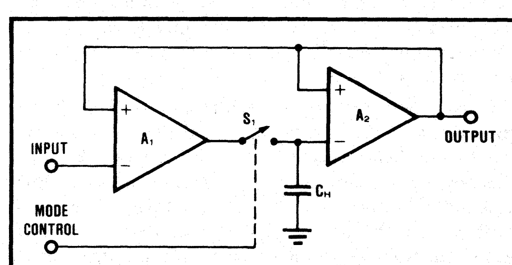


FIGURE 1. Ideal Sample/Hold Amplifier.

minimum of three terminals are provided for the user: input, output, and mode control (or sample/hold control). When S_1 is closed, the output signal follows the input signal, subject to errors imposed by amplifier bandwidth and other errors as discussed below. When S_1 is opened, the voltage stored on the holding capacitor will be held indefinitely (in the ideal case), and will appear at the output of the circuit until S_1 is again closed under command of the mode control signal.

The following discussion of specifications covers the critical types of errors which may be experienced in applications of a sample/hold amplifier. These errors are depicted graphically in Figure 2, and in the Typical Performance Curves.

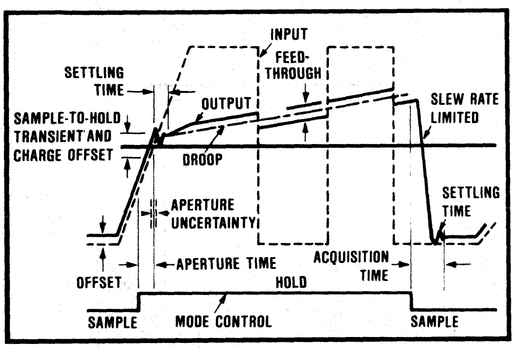


FIGURE 2. Illustration of Sample/Hold Specifications.

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value after the sample mode is initiated. Included in this time are effects of switch delay time, slew rate of the buffer amplifier, and settling time for a specified change in held voltage value. Slew rate limitations of the buffer amplifier will cause actual acquisition time to be highly dependent on the amplitude of the voltage to be acquired, relative to the value already held by the capacitor. Therefore, proper specification of sample/hold amplifier performance includes definition of both output value step size and required error band accuracy.

Aperture Time (or aperture delay time) is the time required for switch S_1 to open and remove the charging signal from the capacitor after the mode control signal has changed from "sample" to "hold". This time is measured from the 50% point of the Hold mode transition to the time at which the output stops tracking the input. This parameter is very important in applications for which the input signal is changing very rapidly when the Hold mode is initiated.

Effective Aperture Time is the difference in propagation delay times of the analog signal and the mode control signal from their respective input pins to switch S_1. This time may be negative, zero, or positive. A negative value indicates that the mode control propagation delay is shorter than the analog propagation delay, with the result that the analog value present on the capacitor at the time the switch opens occurred earlier than the application of the mode control signal by the amount of the effective aperture delay time.

Aperture Uncertainty (or aperture jitter) is the variation observed in the aperture time over a large number of observations. This parameter is important when the analog input is a rapidly changing signal, as aperture uncertainty contributes to lack of knowledge (at the output) about the true value of the input at the precise time the Hold mode is initiated. The maximum input frequency for a given acceptable error contribution due to aperture uncertainty is

$$f_{max} = \text{Maximum Fractional Error} / 2\pi t_u$$

where Maximum Fractional Error (MFE) is the ratio of the maximum allowable error voltage to peak voltage, and t_u is the aperture uncertainty time. For a bipolar ±10V signal and a maximum uncertainty error of 1/2LSB in a 12-bit system, the MFE is equal to 1/2LSB ÷ V_{PEAK} = 2.44mV ÷ 10V = 0.000244V/V, since 1/2LSB = 2.44mV for a 20V full-scale range.
For the same system operating with a unipolar 0V to 10V signal, MFE would be 0.000122V/V.

Charge Offset (pedestal) is the output voltage change that results from charge transfer into the hold capacitor through stray capacitance when the Hold mode command is given. This charge appears as an offset voltage at the output, and in some sample/hold amplifiers may be a function of the input voltage.

Charge offset is specified for the SHC5320 using only the internal holding capacitor. When an external capacitor is added, charge offset is calculated as Charge Transfer (pC) divided by total hold capacitance. Charge Transfer is also specified for the SHC5320, and total hold capacitance is the sum of the internal hold capacitor value (100pF) and the external hold capacitor. Since charge transfer is not a function of analog input voltage for the SHC5320, this error may be removed by means of the offset adjustment capability of the amplifier.

Droop Rate is the change in output voltage over time during the Hold mode as a result of hold capacitor leakage, switch leakage, and bias current of the output amplifier. Droop rate varies with temperature and the quality of the external holding capacitor, if used. Careful circuit layout is also required to minimize droop.

Drift Current is the net leakage current affecting the hold capacitor during the Hold mode. With knowledge of the drift current, droop can be calculated as:

$$\text{Droop (V/sec)} = I_D(\text{pA}) / C_H(\text{pF})$$

Hold Mode Feedthrough is the fraction of the input signal which appears at the output while in the Hold mode. It is primarily a function of switch capacitance, but may also be increased by poor layout practices.

Hold Mode Settling Time is the time required for the sample-to-hold transient to settle within a specified error band.

OPERATING INSTRUCTIONS

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold modes. The offset should then be adjusted to zero output for the periods when the amplifier is in the Hold mode. In this way, the effects of both amplifier offset and charge offset will be accounted for.

SAMPLE/HOLD CONTROL

A TTL logic "0" applied to pin 14 switches the SHC5320 into the Sample (track) mode. In this mode, the device acts as an amplifier which exhibits normal operational amplifier behavior, with the relationship of output to input signal depending upon the circuit configuration selected (see the Installation section below). Application of a logic "1" to pin 14 switches the SHC5320 into the Hold mode, with the output voltage held constant at the value present when the hold command is given. Pin 14 presents less than one LSTTL load to the driving circuit throughout the full operating temperature range.

ADDITION OF AN EXTERNAL CAPACITOR

The SHC5320 contains an internal 100pF MOS holding capacitor, sufficient for most high-speed applications. If improved droop performance is desired (with increased acquisition time), additional capacitance may be added between pins 7 and 11. If an external holding capacitor C_H is used, then a noise-bandwidth capacitor with a value of $0.1C_H$ should be connected from pin 8 to ground. The exact value and type of this bandwidth capacitor are not critical.

Capacitors with high insulation resistance and low dielectric absorption, such as Teflon® or polystyrene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor to minimize droop errors.

The value of the external capacitor determines the droop, charge offset, and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with total hold capacitance from the values given in the specification table for the internal 100pF capacitor. The behavior of acquisition time versus total hold capacitance is shown in the Typical Performance Curves.

OUTPUT PROTECTION

In order to optimize high-frequency performance of this device, output protection is not included. This high-frequency performance is mandatory for a good sample/hold, which must absorb high-frequency changes in load current when driving a successive-approximation A/D converter. Due to the lack of output protection, the output circuit will not tolerate an indefinite short to common, but a momentary short is permissible. The output should never be shorted to supply.

Teflon® DuPont Corporation

INSTALLATION

LAYOUT PRECAUTIONS

Since the holding capacitor is connected to virtual ground at one end (pin 11) and to a low-impedance voltage source at the other (pin 7), the SHC5320 does not require the use of guard rings and other careful layout techniques which are required by many sample/hold circuits. However, normal good layout practice should be observed, minimizing the possibility of leakage paths across the holding capacitor. As in all digital-analog circuits, analog signal lines on the circuit board should cross digital signal paths at right angles whenever possible.

GROUNDING AND BYPASSING

Pin 6 (REFERENCE COMMON) should be connected to the system analog signal common as close to the unit as possible. Likewise, pin 13 (SUPPLY COMMON) should be connected to the system supply common. If the system design prevents running these two common lines separately, they should be connected together close to the unit, preferably to a large ground plane surrounding the sample/hold. Bypass capacitors (0.01μF to 0.1μF ceramic in parallel with 1μF to 10μF tantalum) should be connected from each power supply terminal of the device to pin 13 (SUPPLY COMMON).

OFFSET ADJUSTMENT

Offset adjustment capability may be achieved by connecting a 10kΩ, 10-turn potentiometer as illustrated in Figure 3.

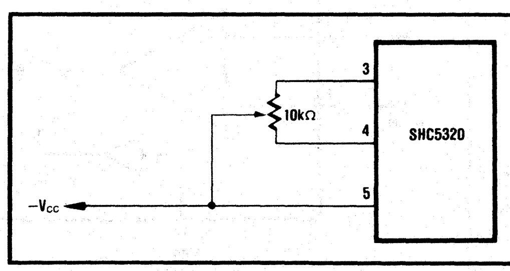


FIGURE 3. Connection of Offset Adjustment Potentiometer.

NONINVERTING MODE

The most common application of the SHC5320 will utilize the connection illustrated in Figure 4. In this mode of operation, the sample/hold will operate as a unity-gain noninverting amplifier when in the Sample mode, and the output signal will track the input. The high bandwidth of the SHC5320 and the large open-loop gain assure that gain error will be minimized.

When sampling lower-amplitude signals, the SHC5320 may also be connected as a noninverting amplifier with gain, as illustrated in Figure 5. In this circuit the gain of the amplifier is equal to $1 + R_2/R_1$ when sampling.

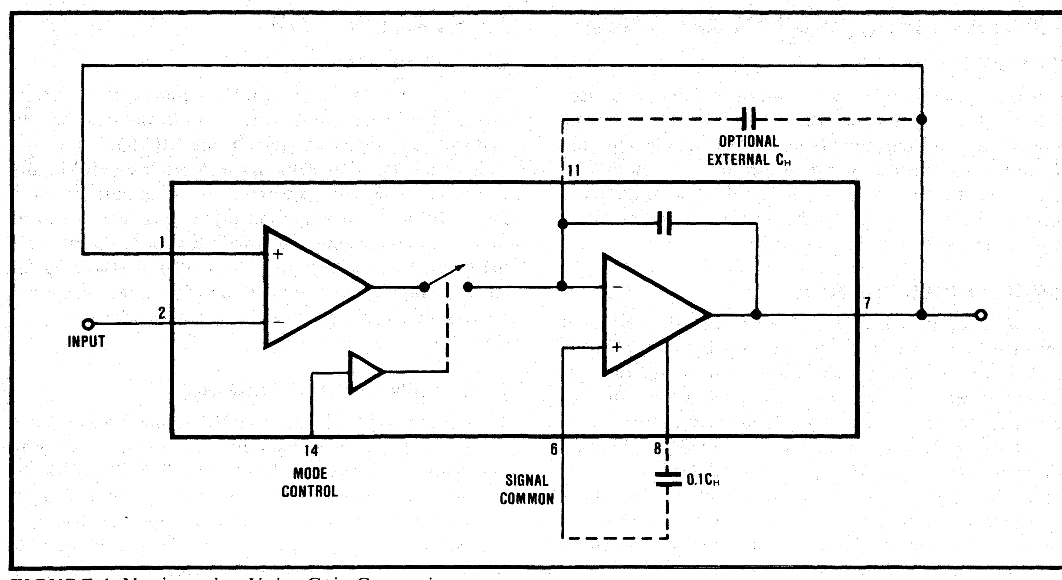


FIGURE 4. Noninverting Unity-Gain Connections.

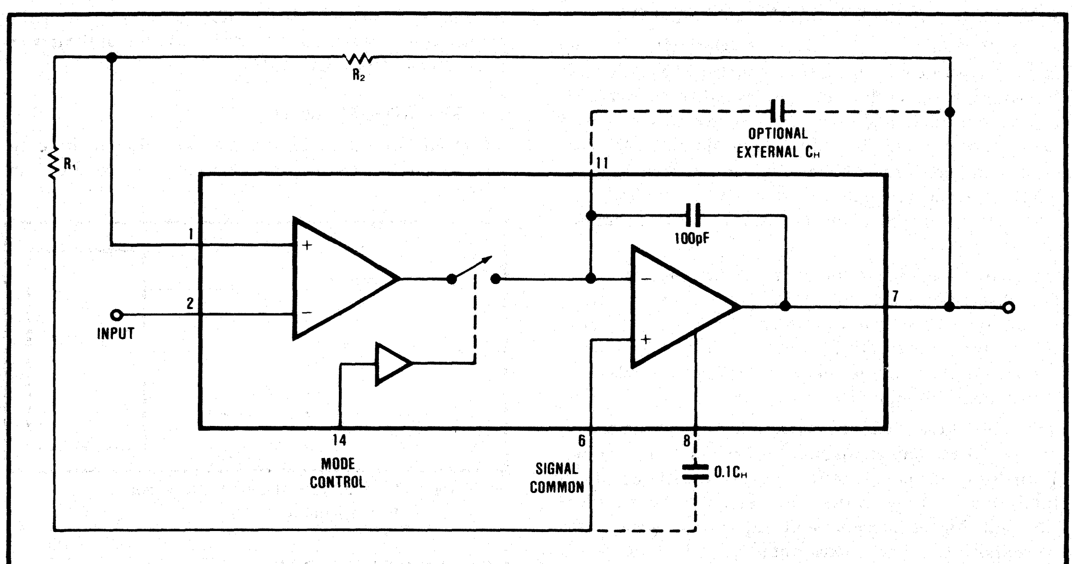


FIGURE 5. Noninverting Configuration with Gain = $1 + R_2/R_1$.

INVERTING MODE

Unlike most sample/holds, the SHC5320 may also be connected to act as an inverting amplifier, as shown in Figure 6. For this configuration, the gain is equal to $-R_2/R_1$.

For further discussions of operational amplifiers and how to use them, consult the Burr-Brown/McGraw-Hill Electronics Series of reference books, available through your local Burr-Brown sales office.

INPUT OVERLOAD PROTECTION

It is possible that the input transconductance amplifier of the SHC5320 will saturate when the unit is in the Hold mode, due to a nonzero differential signal appearing between pins 1 and 2. This differential signal may be the result of a rapidly changing input signal or application of a new channel from an input multiplexer. When the input buffer is saturated in this fashion, acquisition time may be degraded because of the time required for

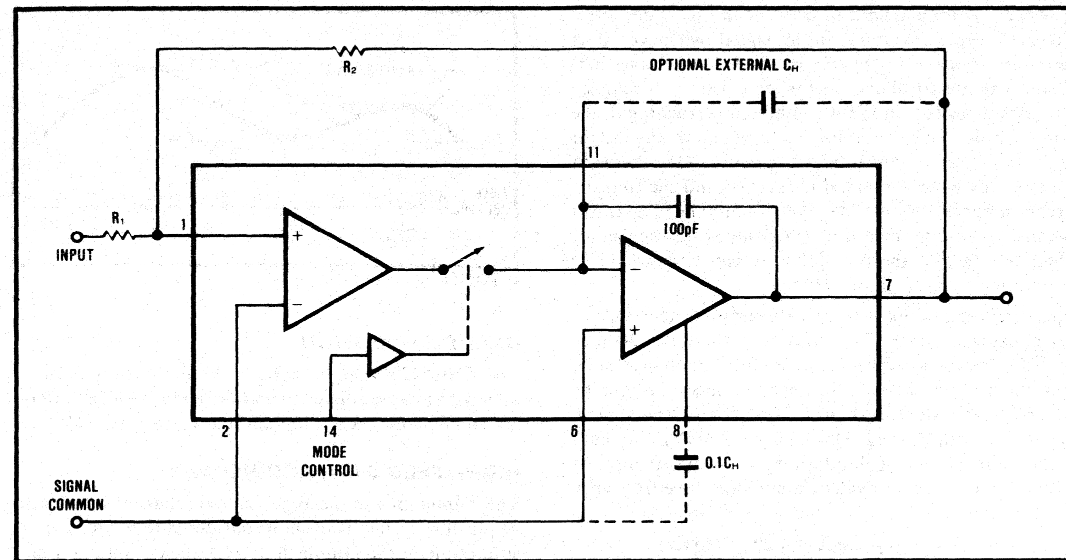


FIGURE 6. Inverting Configuration with Gain = $-(R_2/R_1)$.

the buffer to recover from saturation. In addition, the input buffer, which is designed to provide large amounts of charging current to the output integrator, may draw large amounts of supply current which may exceed 40mA peak in some applications. For these reasons, it is desirable to limit the differential voltage which may appear at the summing junction of the input buffer. Figures 7 and 8 illustrate possible methods of providing this

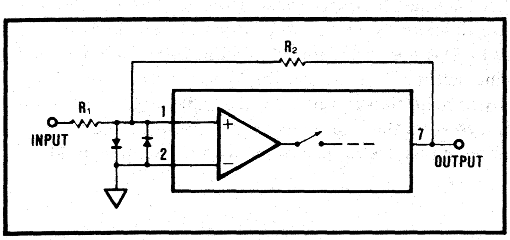


FIGURE 7. Input Overload Protection—Inverting Configuration.

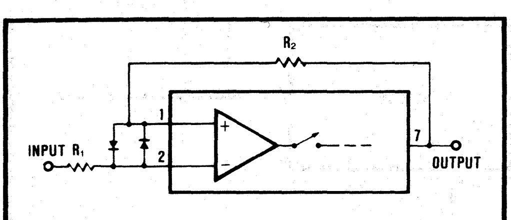


FIGURE 8. Input Overload Protection—Noninverting Configuration.

voltage limitation for the inverting and noninverting configurations. The diodes may be Schottky diodes, which will provide the fastest clamping action and lowest clamping voltage, but fast signal diodes such as 1N914 will also work in most applications. In each configuration the value of R_1 should be large enough to avoid excessive loading of the input signal source. Similarly, R_2 should have a value of 2kΩ or greater to insure sufficient load current capability from the sample/hold. If the value of R_2 becomes too large, however, the added capacitance of the diodes may change the sample/hold phase response enough to cause oscillation.

APPLICATIONS

SIGNAL DIGITIZATION

Sample/hold amplifiers are normally used to hold input voltages to an A/D converter constant during conversion. Digitizing errors result if the analog signal being digitized varies excessively during conversion.

For example, the Burr-Brown ADC80H-AH-12 is a 12-bit successive-approximation converter with a 25μsec conversion time. To insure the accuracy of the output data, the analog input signal to the A/D converter must not change more than 1/2LSB during conversion.

The maximum rate of change of a sine wave of frequency, f, is $dv/dt\,(max) = 2\pi Af\,(V/sec)$. If one allows a 1/2LSB change (2.44mV) for a ±10V input swing to the A/D converter, the allowable input rate-of-change limit would be 2.44mV/25μsec = 0.0976mV/μsec. Thus the sampled sinusoidal signal frequency limit is

$$f = (0.0976 \times 10^3)/2\pi A = 15.5/A\ (Hz),$$

where A is the peak amplitude of the sine wave. For a ±10V sine wave, this corresponds to a frequency of 1.6Hz, hardly acceptable for the majority of sampled data systems.

However, a sample/hold in front of the A/D converter "freezes" the converter's input signal whenever it is necessary to make a conversion. The rate-of-change limitation calculated above no longer exists. If a sample/hold has acquired an input signal and is tracking it, the sample/hold can be commanded to hold it at any instant in time. There is a short delay (aperture delay) between the time the hold command is asserted and the time the circuit actually holds. The hold command signal can usually be advanced in time (or delayed, in the case of negative effective aperture delay) to cause the amplifier to hold the signal actually desired.

Aperture uncertainty (also called aperture jitter) is also a key consideration. For the SHC5320 there is a 300psec period during which the signal should not change more than the amount allowed for aperture uncertainty in the system error budget, perhaps 1/2LSB for a 12-bit system. For a ±10V input range (1/2LSB = 2.44mV), the input signal rate of change limitation is 2.44mV/0.3nsec = 8.13mV/nsec. The equivalent input sine wave frequency is

$$f = 8.13 \times 10^6 / 2\pi A = 1.29/A \text{ (MHz)},$$

a factor of almost 84,000 higher than using the A/D alone.

However, there are other considerations. The resampling rate of an ADC80H/SHC5320 combination is 26.5μsec (25μsec A/D conversion time plus 1.5μsec S/H acquisition time). Sampling a sine wave at the Nyquist rate, this permits a maximum input signal frequency of 37.7kHz. The above analysis assumes that the droop rate of the sample/hold is negligible—less than 1/2LSB during the conversion time—and that the large signal bandwidth response of the sample/hold causes negligible waveform distortion. Both of these assumptions are valid for the SHC5320 in this application.

DATA ACQUISITION

The SHC5320 may be used to hold data for analog-to-digital conversion or may be used to provide pulse-amplitude modulation (PAM) data output (see Figures 9 and 10).

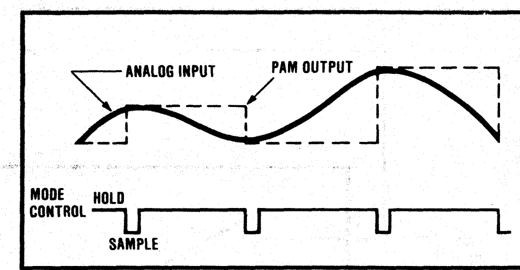


FIGURE 10. PAM Output.

DATA DISTRIBUTION

The SHC5320 may be used to hold the output of a digital-to-analog converter and distribute several different analog voltages to different loads (see Figure 11).

HIGH-SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the A/D converter. If two or more sample/holds are used with a multiplexer (such as the Burr-Brown MPC8S or MPC16S) as shown in Figure 12, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched into the A/D converter, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this signal by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed. In low level systems an instrumentation amplifier (such as the Burr-Brown INA101) and a differential multiplexer (such as the Burr-Brown MPC4D or MPC8D) may be required in front of the sample/hold. The settling and acquisition times of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the total conversion time as before by operating in this overlapped mode with the sample/holds.

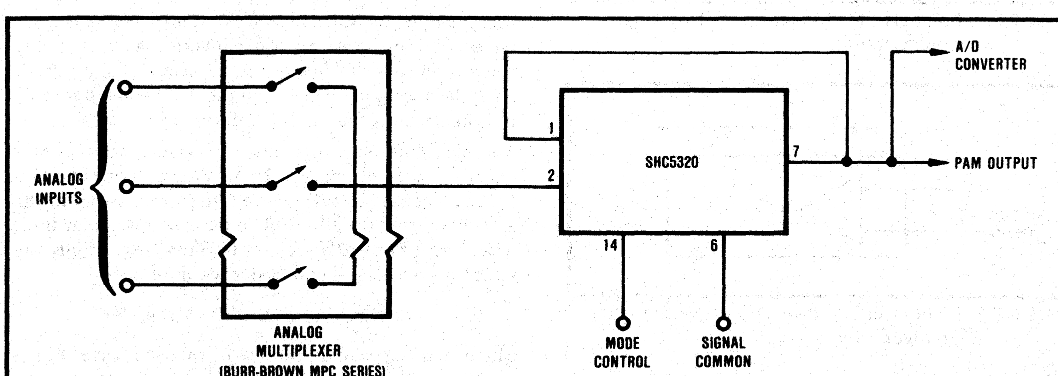


FIGURE 9. Typical Data Acquisition Configuration.

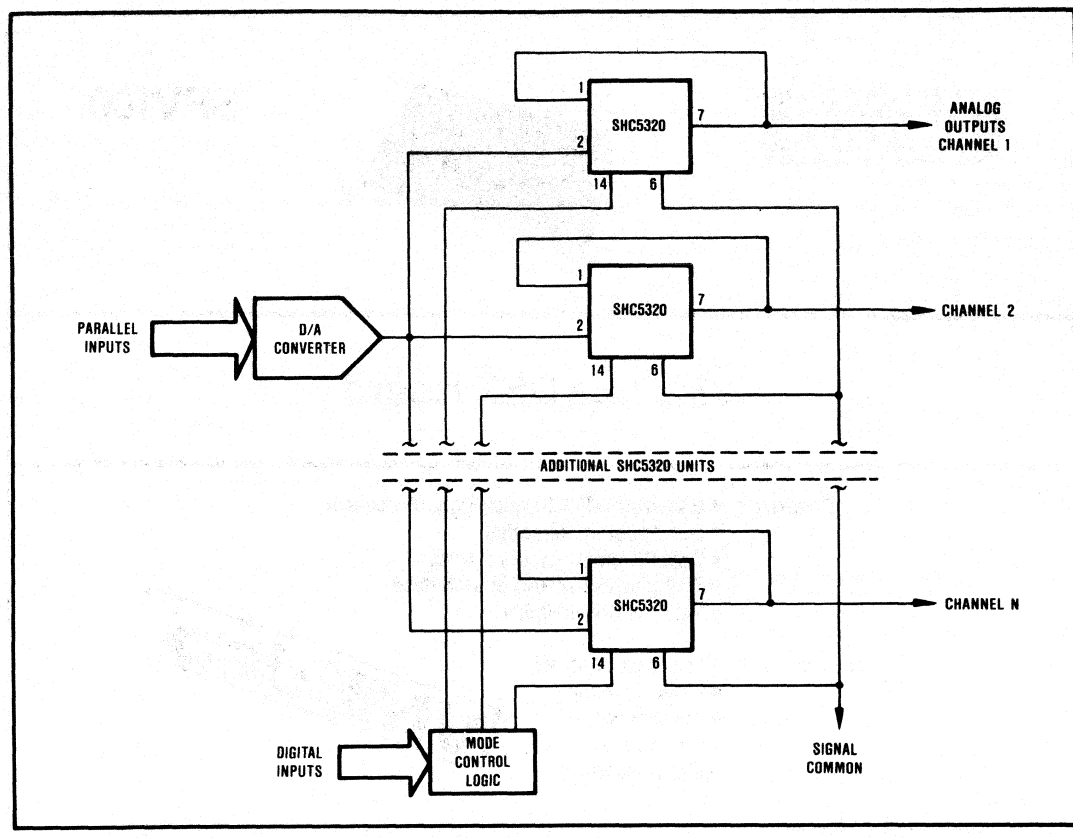


FIGURE 11. Typical Data Distribution Configuration.

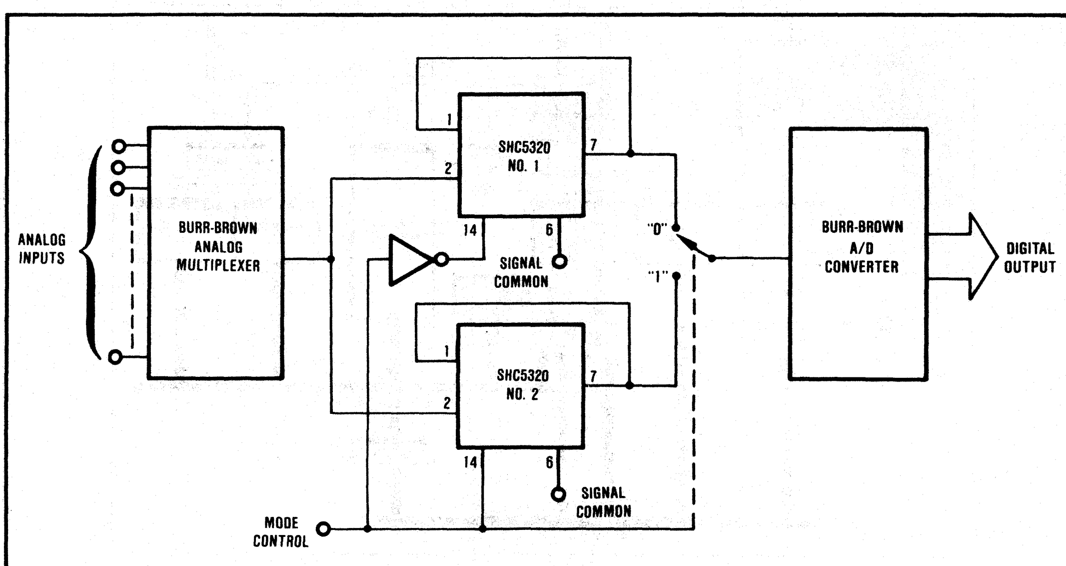
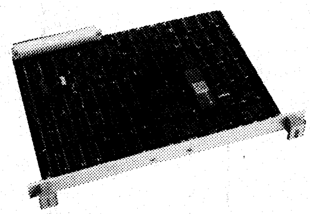


FIGURE 12. Typical Overlapped Sample/Hold Configuration.



SPV100

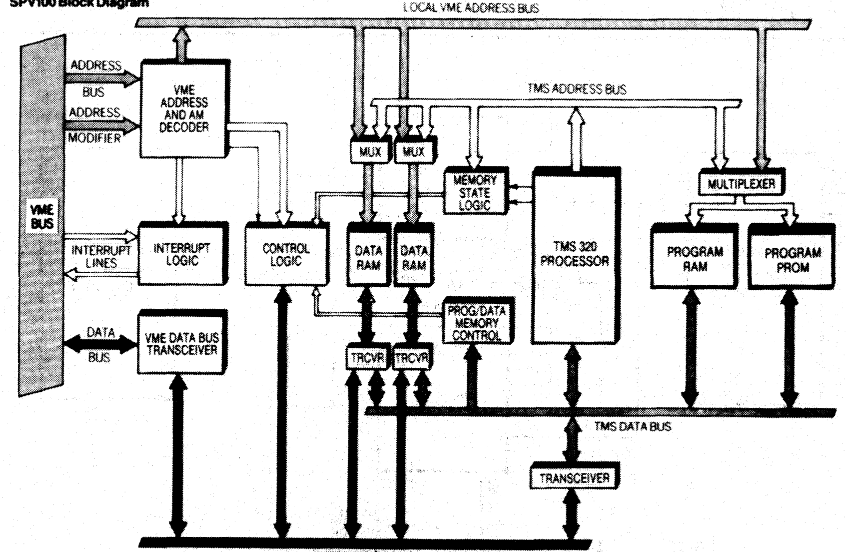
VMEbus DSP Board

Features
- Based on TMS320 Digital Signal Processor
- Dual Program Memories
- Data/Program memory overlap
- Swinging Buffer RAM bus Interface
- VMEbus Compatibility

Applications
- Spectrum Analysis
- Digital Filtering
- Correlation
- Convolution
- Matrix Inversion

VMEdsp™

SPV100 Block Diagram



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SPV100 – Adaptable Digital Signal Processing Board

Flexibility Through Software

Since the board function is defined by software, the SPV100 can be easily programmed for a wide range of functions from general purpose programs to very specialised user originated programs.
The board has been specially designed for two types of user. Those who wish to use standard software packages and those who wish to develop their own software.

TMS 320 Processor

The SPV100 is a fixed-point digital signal processor board with full VMEbus compatibility. It incorporates the advanced Texas Instruments TMS320 digital signal processor chip with its 5MHz instruction cycle and a specialised arithmetic section significantly more powerful and faster than traditional microprocessors.

Program Memories

To enhance user flexibility, the SPV100 has two program memories:-

1. 4K x 16 PROM – This is primarily used for software packages supplied by Burr-Brown on PROM. The board is supplied with test software in PROM to allow the user to check the correct operation on the board. Other application software is available from Burr-Brown (eg FFT packages).
   If desired, PROM-based packages can be stored on the host system's main storage device and down-loaded to run in the SPV100 program RAM.
2. 4K x 16 RAM – Programs developed by the user can be down-loaded and run in program RAM.

Program memories are software or jumper selectable.

Data/Program Memory Overlap

The TMS320 can address only 4K words of memory, which means that data and program memory have usually to be combined into a single 4K word address space. This limits the size of either the program or quantity of data that can be processed.
The SPV100 overcomes this limitation by incorporating hardware which allows the TMS320 to address both 4K words of program memory **and** 4K words of data memory with no loss of speed.

Swinging Buffer Data Memory

Two 4K x 16 bit data RAM's operating in a swinging buffer mode ensure that while the TMS320 is processing the data in one memory (say data RAM A) the other data RAM (B) can be emptied of processed data and refilled with new raw data. When processing of data in RAM A is complete, the TMS320 switches its attention to data RAM B and this cyclical process continues.
For most programs, a data RAM can be emptied and refilled in less time than the TMS320 takes to process the new set of data. In this way system data flow is maintained at almost the same speed as the TMS320 processing speed.

Test Software

The SPV100 is supplied with self test firmware (located in the program memory PROM) to ensure that the board is functioning correctly. Commands from the host computer initiate the self test and check for a correct result. In addition to checking basic board operation, the self test checks the memory and generates a checkword which can be used to give error code and address information.

Software Support

Software packages (2 PROMS plus software manual) are available from Burr-Brown which are specially designed to operate on the SPV100. Availability on request.

Ordering Information

SPV100 – Digital Signal Processing Board
OM100 – Hardware Operating Manual for SPV100 (As supplied with board)

Hardware Specifications:

TMS320 Digital Signal Processor Chip
- 5MHZ clock rate
- 16 x 16 bit multiply and accumulate in 400nS

Program Memory
- 4K x 16 bit RAM
- 4K x 16 bit PROM

Data Memory
- Dual 4K x 16 bit RAM

Maximum Transfer Rate
- 4 Megawords/sec

Data Organisation
- Complex with 16 bit real and 16 bit imaginary components

Data Format
- Signed 2's complement fixed-point

VMEbus Interface
- A24, D16, DTB SLAVE
- 32 Kbyte Address block selectable within 16 Mbyte memory space
- Short addressing availability if required (64K)
- Address Modifier selections with PROM options
- 7 level interrupt priority selection
- Full interrupt vector capability

Size
- double Eurocard 160mm x 233mm.

Environmental
- Operating temperature 0°C to 60°C relative humidity 5% to 90% non-condensing

TOP QUALITY VMEbus PRODUCTS FROM BURR-BROWN

In addition to the full Q.C. vetting of incoming components, the boards are subjected to a comprehensive temperature cycled burn-in (8 cycles between −20°C and +50°C).

Exhaustive tests before and after burn-in ensure that any problems are identified before the product leaves the factory.

SUPPORT DOCUMENTATION

Each VMEbus board is fully supported with a comprehensive operating manual. In addition to detailed set-up and operating instructions, the manual includes schematics and assembly language software written for the 68000 processor.

THE SYSTEMS APPROACH

This board is one of a family of VMEbus boards in which a systems approach has been taken in the design of the bus interface. This ensures software compatibility between the boards as well as giving the system designer a wide range of VMEbus features.

- Configuration A24, D16, DTB slave
- Address block selectable within 16M byte memory space
- Short addressing available if required (64K bytes)
- Multiple address modifier capability

Contact Burr-Brown for the full range of Analog I/O and DSP boards on the VMEbus

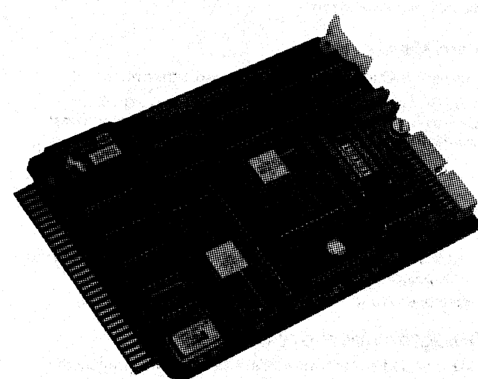
BURR-BROWN®

ST4603

STD BUS ANALOG INPUT PROCESSOR

FEATURES

- **6809 PROCESSOR**
- **6839 FLOATING POINT MATH ROM**
- **UP TO 32 KBYTES EPROM**
- **2 KBYTES STATIC RAM**
- **12 BIT 10 μSEC A/D CONVERTER**
- **ONBOARD SAMPLE/HOLD AMPLIFIER**
- **±15 VDC POWER SUPPLY**



DESCRIPTION

The ST4603 is a sophisticated Analog Input Processor which can accept conditioned analog signals from the ST4703 Signal Conditioning Interface. The onboard processor, math ROM, and combination of RAM and EPROM provide a considerable degree of flexibility for complex data acquisition applications.

Up to 8 Signal Conditioning Interfaces may be interconnected to an individual ST4603, thereby providing 64 differential and 8 special function analog inputs to be processed.

The Analog section consists of a 12 bit successive approximation Analog to Digital converter, buffered by a precision Sample/Hold Amplifier. Gain and offset of the A/D are potentiometer adjustable, and either bipolar or unipolar operation is selectable by jumper option. An onboard DC to DC converter supplies ±15 VDC for all analog functions.

The Digital section consists of the 6809 processor, EPROM and RAM memory, 6839 math ROM, and bus control logic. Commands to select a channel, set offset, or select a special function are built in to the resident EPROM and are controlled by the ST4603 processor. Communication with the host STD system is accomplished through two registers and involves the use of a simple software protocol.

The ST4603 occupies two I/O addresses within host system memory. To communicate with the board, the host places an attention byte in the ST4603 Read register. The ST4603 acknowledges that it has received a request by placing an "acknowledge" byte in the host Read register. The host places a command in the register, and expects a second acknowledgment, in return. Communication continues in this fashion. An example protocol is outlined in the technical manual, where certain byte values have been reserved for inter-processor communication and a group of commands have been established for the ST4603 processor. The board can also set or reset the INTRQ line, for subsequent service by the host processor.

The 6839 Math ROM provides the capability of further processing the data prior to presentation to the host. If the intended application requires more EPROM than is provided in the standard configuration, the 6839 may be removed and a 2732-type EPROM may be inserted in its place.

For ease of system integration and product familiarization, the product is shipped with a standard EPROM containing a simple test program. This program allows for communication between the host and a ST4603/4703 board set. Also provided with each board is a technical manual with a comprehensive applications section, including software listings and logic diagrams of a typical thermocouple application.

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SPECIFICATIONS

HOST SYSTEM CLOCK RATE, max.
6.0 MHz

OPERATING RANGE
0° C to +50° C

I/O ADDRESSING
Any 2 consecutive addresses, jumper selectable on any even address boundary

I/O PORT DESCRIPTION
1 Write only and 1 Read only port, the parameters of which are user defined

COMPATIBILITY
STD-6809
STD-8080
STD-Z80
note: compatible with Mode 0 and Mode 1 interrupts. Options allow for compatibility with other standards—contact factory.

VOLTAGE REQUIREMENTS
+5 VDC @ 1 A

DIMENSIONS
4.50″ x 6.50″ x .48″

CONNECTOR TYPE
26 pin (2 x 13 x .10″)

PROCESSOR TYPE
68B09

PROCESSOR CLOCK RATE
2.0 MHz

FLOATING POINT MATH ROM TYPE
68B39

A/D CONVERTER TYPE
ADC84KG-12 or equivalent

CONVERSION TIME
10 μSEC

MEMORY ORGANIZATION
16K EPROM, 2K Static RAM standard
32K EPROM extended optional

EXAMPLE COMMAND TABLE

DESCRIPTION	D7	D6	D5	D4	D3	D2	D1	D0
Channel definition	0	0	T	T	C	C	C	C
Read channel data	0	1	0	0	C	C	C	C
Read status	0	1	0	X	X	X	X	X
Calibrate	1	0	X	X	X	X	X	X

notes: T T = Thermocouple type C = Channel number 0–15

T T	Type
0 0	K
0 1	J
1 0	S
1 1	T

X = Don't care

Typical status codes

CODE	DESCRIPTION
00	Normal operation
01	Invalid command
02	Offset error
03	Timeout/Bus interface error
04	Undefined
05	Table lookup error

Typical communication bytes

NAME	BYTE VALUE (HEX)
ACK0	00
ACK1	01
SRDY	03
HDACK0	F0
HDACK1	F1
HDACK2	F2
HDACK3	F3
HRDY	FE
HACK	FD

PIN ASSIGNMENTS

P2 DATA I/O CONNECTOR:

Pin	Description	Pin	Description
1	COMMON	14	DATA 6
2	ANALOG SIGNAL	15	DIGITAL GND
3	DIGITAL GND	16	DATA 5
4	DIGITAL GND	17	DIGITAL GND
5	ADDRESS 4	18	DATA 4
6	ENABLE	19	DIGITAL GND
7	ADDRESS 3	20	DATA 3
8	ADDRESS 1	21	DIGITAL GND
9	ADDRESS 2	22	DATA 2
10	ADDRESS 0	23	DIGITAL GND
11	DIGITAL GND	24	DATA 1
12	DATA 7	25	DIGITAL GND
13	DIGITAL GND	26	DATA 0

All products are shipped with a complete documentation package which includes comprehensive operating instructions, user option tables, parts placement diagrams, and software examples.

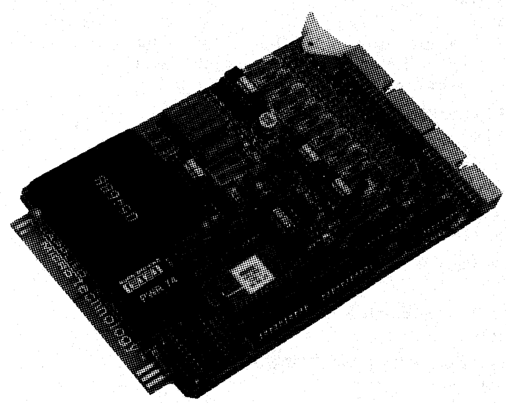
BURR-BROWN®

ST4703

STD BUS SIGNAL CONDITIONING INTERFACE

FEATURES

- EIGHT GENERAL PURPOSE DIFFERENTIAL INPUT CHANNELS
- ONE SPECIAL PURPOSE SINGLE ENDED INPUT CHANNEL
- SOFTWARE PROGRAMMABLE OFFSET COMPENSATION
- SOFTWARE PROGRAMMABLE GAIN
- INPUT PRE-CONDITIONING
- MULTIPLE POLE FILTER
- TEMPERATURE SENSOR
- TRANSDUCER EXCITATION
- ±15 VDC POWER SUPPLY
- ISOLATED INPUTS



DESCRIPTION

The ST4703 is an Eight Channel Signal Conditioning Interface which can accept inputs from a wide variety of sensor devices, including strain gauges, RTDs, and thermocouples. It easily interfaces with a companion product, the ST4603 Analog Input Processor, and provides the basis for a sophisticated analog data acquisition system.

The board is comprised of three functional stages: the Isolated Input Processor, the Programmable Gain and Offset Generator, and the Host Processor Interface.

The Isolated Input Processor stage consists of an input attenuation network, low pass filter, analog multiplexers, and an Instrumentation Amplifier. The attenuation network and low pass filter allow scaling and intermixing of practically any combination of input signals. This stage further provides four special function features: Isolated Zero Volts, Isolated Excitation Voltage, Onboard Temperature Sensor, and Offboard Temperature Sensor. These features permit the board to be used in applications such as cold junction compensation, ratiometric measurement, and environmental temperature monitoring.

The Excitation Voltage source provides 0 to 10 volts at up to 40 mA for transducers such as load cells and RTDs. An external source may also be used. The Onboard Temperature Sensor provides a reference point for applications where temperature drift is critical to the measurement.

All signals are coupled through a high quality optically isolated amplifier to the Programmable Gain/Offset stage.

Both offset and gain are software controllable through the ST4603. The Offset Generator is a 12 bit DAC, which provides a programmable range of up to 50% of the full scale input signal. The DAC output is summed with the signal at the input of the gain element. Gain can be programmed within the range of 1 to 100. The output of this element is filtered by a multi-pole active Chebyshev band pass network to reduce the effects of 60 Hz noise. The filter may be easily modified to suit different frequency response or settling time requirements.

The Host Processor Interface section decodes the board address, and transfers digital data and control bytes and the conditioned analog signal between the board and the ST4603. Up to eight ST4703 boards may be interconnected to a single host, thereby allowing 64 differential and 8 single ended inputs to be processed.

Onboard power supplies derive the ±15 VDC from the STD Bus +5V. These supplies provide all of the isolated and non-isolated voltages required for operation. If desired, external supplies may be used in their place.

Each ST4703 is supplied with the appropriate ST4603 interface cable. An optional signal interface cable set which includes a terminal block, the AC4703, may be ordered separately.

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SPECIFICATIONS

OPERATING RANGE
0° to +50° C

ADDRESSING
Responds to 1 of 8 jumper selectable addresses

FORM FACTOR
STD Bus

DIMENSIONS
4.50" x 6.50" x .50"

VOLTAGE REQUIREMENTS
+ 5 VDC @ 2.8 Amps.

MAXIMUM INPUT VOLTAGE
±15V relative to isolated ground

INPUT BIAS CURRENT
±30 nA

ISOLATION BARRIER
750V

COMMON MODE REJECTION (CMRR)
90 dB

FIXED GAIN
1.7 approx.

PROGRAMMABLE GAIN
1 to 100

INSTRUMENTATION AMP GAIN
1 to 500

OFFSET GENERATOR
12 bit DAC

OFFSET RANGE
50% FSR

EXCITATION OUTPUT
0 to 10 VDC @ 40 mA

CONNECTOR TYPES
Analog Input: 34 pin
Data I/O: 26 pin
(both .100 x .100")

OPTIONS

- AC4703 Cable set and terminal block; please specify length
- ST4603 Interconnect cables for multiple ST4703 applications

PIN ASSIGNMENTS

P1 ANALOG INPUT CONNECTOR:

Pin	Description
1	CHANNEL 0 +
2	CHANNEL 0 −
3	CHANNEL 0 AUX
4	CHANNEL 0 GND
5	CHANNEL 1 +
6	CHANNEL 1 −
7	CHANNEL 1 AUX
8	CHANNEL 1 GND
9	CHANNEL 2 +
10	CHANNEL 2 −
11	CHANNEL 2 AUX
12	CHANNEL 2 GND
13	CHANNEL 3 +
14	CHANNEL 3 −
15	CHANNEL 3 AUX
16	CHANNEL 3 GND
17	CHANNEL 4 +
18	CHANNEL 4 −
19	CHANNEL 4 AUX
20	CHANNEL 4 GND
21	CHANNEL 5 +
22	CHANNEL 5 −
23	CHANNEL 5 AUX
24	CHANNEL 5 GND
25	CHANNEL 6 +
26	CHANNEL 6 −
27	REMOTE TEMP SENSOR
28	CHANNEL 6 GND
29	CHANNEL 7 +
30	CHANNEL 7 −
31	NEGATIVE ISOLATED DC
32	CHANNEL 7 GND
33	REFERENCE EXCITER
34	POSITIVE ISOLATED DC

P2 DATA I/O CONNECTOR:

Pin	Description
1	COMMON
2	ANALOG SIGNAL
3	DIGITAL GND
4	DIGITAL GND
5	ADDRESS 4
6	ENABLE
7	ADDRESS 3
8	ADDRESS 1
9	ADDRESS 2
10	ADDRESS 0
11	DIGITAL GND
12	DATA 7
13	DIGITAL GND
14	DATA 6
15	DIGITAL GND
16	DATA 5
17	DIGITAL GND
18	DATA 4
19	DIGITAL GND
20	DATA 3
21	DIGITAL GND
22	DATA 2
23	DIGITAL GND
24	DATA 1
25	DIGITAL GND
26	DATA 0

I/O PORT DESCRIPTION

		INTERFACE DATA								INTERFACE ADDRESS				
LATCH	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0	A4	A3	A2	A1	A0
0	DAC LSB	D	D	D	D	D	D	D	D	B	B	B	0	0
1	OUTPUT ENABLE	1	X	X	X	X	X	X	X	B	B	B	0	1
1	DAC MSB	X	X	X	X	D	D	D	D	B	B	B	0	1
1	GAIN SELECT	X	G	G	G	X	X	X	X	B	B	B	0	1
2	CHANNEL SELECT	0	X	X	X	X	C	C	C	B	B	B	1	0
2	SPECIAL FUNCTION	1	X	X	A	A	X	F	F	B	B	B	1	0

notes: B = Board select address
D = offset DAC data bits
G = Gain select
X = Don't care

Special function select bits:

F	F	Description
0	0	Isolated Ground
0	1	Onboard temperature sensor
1	0	Offboard temperature sensor
1	1	Exciter

S	S	Description
0	1	Offset DAC amplified
1	0	Offset DAC not amplified

All products are shipped with a complete documentation package which includes comprehensive operating instructions, user option tables, parts placement diagrams, and software examples.

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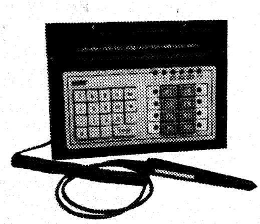

TM200

DATA ENTRY TERMINAL AND BAR CODE READER For Heavy Industrial Environments

FEATURES

- STEEL CASE-RUGGED CONSTRUCTION
- PANEL MOUNTING WITH GASKET FOR WATER/DIRT RESISTANCE
- DIRT/MOISTURE PROTECTED INDUSTRIAL KEYBOARD
- 40-CHARACTER VACUUM FLUORESCENT DISPLAY
- RS-232, RS-422, AND CURRENT LOOP INTERFACES
- ONE-TO-ONE OR MULTIDROP (POLLED) OPERATION
- BUFFERED INPUT AND OUTPUT
- PARALLEL PRINTER PORT
- 10 TTL OUTPUTS
- USER EPROM
- OPTIONAL BAR CODE WAND

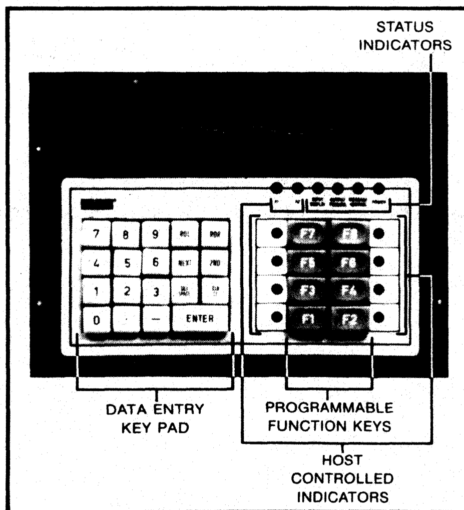

FIGURE 1. TM200 Front Panel Features.

DESCRIPTION

Data entry/control/display requirements have always been a problem in heavy industrial environments. Standard CRT terminals cannot survive long in heat, dust, and moisture. Special CRT terminals made for these areas are very large and expensive, and often too complex for untrained employees to operate. There is a better solution to get the job done economically and efficiently.

Microterminals are designed expressly to fill the human interface demands of widely dispersed control and communications networks—in machine and process control, energy management systems, inventory control, and factory data collection. Microterminals, because of their interface flexibility, appearance, size, durability, and easy installation, function equally well as consoles and control centers for instruments and small systems.

The TM200 is an extension of Burr-Brown's widely accepted family of Microterminals—designed for heavy industrial environments. Display, keyboard and enclosure are well-suited to the conditions found in these application.

Housed in a tough steel case, the TM200 is protected from debris and moisture. The bright green vacuum fluorescent display is readable from a distance of over 10 feet in varying light conditions. Full-travel keys on 0.75″ centers allow easy data entry by workers wearing gloves.

Buffered data features reduce on-line input/output time with the host computer or CPU and improve accuracy of operator inputs, and, because of its design simplicity, the TM200 doesn't require special operator skills or training. Depressing a single programmable function key can initiate actions by the host.

The terminal communicates in serial ASCII with

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RS-232, RS-422, or current-loop conditioning—making it compatible with almost any CPU. Baud rates are from 110 to 19,200. If desired, units may be connected in multidrop fashion and operated in a "polled" mode (see Figure 2).

The TM200 features an 80-character message buffer, 40-character display, serial ASCII interface, parallel printer interface, and TTL outputs to interface to external equipment. In addition, a connector is provided for the optional BCW200 Bar Code Reader. As a result, the TM200 provides a data entry and display station with hard copy and I/O capabilities.

Alphanumeric data can be entered and displayed with the TM200. A 27-key keypad is provided for manual data entry. With the BCW200 installed, alphanumeric bar codes using code 39 may be entered.

The keys are constructed of ABS plastic and provide excellent tactile feedback. A dust/moisture barrier located beneath the keypad protects the internal electronics from dust and liquid spills. Another gasket seals the tough display bezel.

The 40-character display accommodates messages up to 80 characters long. Displayed messages may be scrolled bidirectionally at varying rates and flashed for attention under host control. Keys for manual scrolling permit review of data entered before transmission.

Two 80-character buffers are provided for keyboard and bar-code-generated data. The output buffer holds a message to be written or reviewed; the transmit buffer holds a prepared message ready for transmission. This feature allows a second message to be entered while the first awaits transmission when in polled mode.

Similarly, two 80-character buffers are available for incoming messages. The receive buffer holds an incoming message until it can be transferred to the input buffer, where it is displayed. With this feature, the operator can visually review a line of input while a second line from the host can be received and held until it is called up for display.

The parallel printer port allows connection of a Centronics type printer to the TM200. Data may be sent directly to the printer from the host, bypassing the display, or the printer may be set to echo keyboard and display messages.

Fourteen status LEDs, 10 under host control, are located on the TM200's front panel (see Figure 1). An audible beeper allows the host system to signal the operator, or this beeper may be set to confirm keyboard or bar code inputs.

A socket is provided for a user-supplied EPROM which may be used to store communications parameters and function messages. While not necessary for normal operation, this feature allows the terminal to be customized to a particular application.

The TM200 is a compact panel-mount terminal that measures 8.25″ × 11.0″ × 1.50″. The front panel provides six mounting holes for bolting the unit to equipment or wall panels. The 1.5″ depth allows mounting in areas with relatively shallow rear clearances. A polycarbonate front panel overlay is provided for indicator legends and labelling of programmable function keys.

It is important to realize that while these Microterminals have many features, normal operation is very uncomplicated. Virtually untrained operators can use the terminal productively. Most special features are invisible to the operator.

APPLICATIONS

- MACHINE CONTROL
- PROCESS CONTROL
- ENERGY MANAGEMENT SYSTEMS
- INVENTORY CONTROL
- FACTORY DATA COLLECTION
- ACCESS/SECURITY

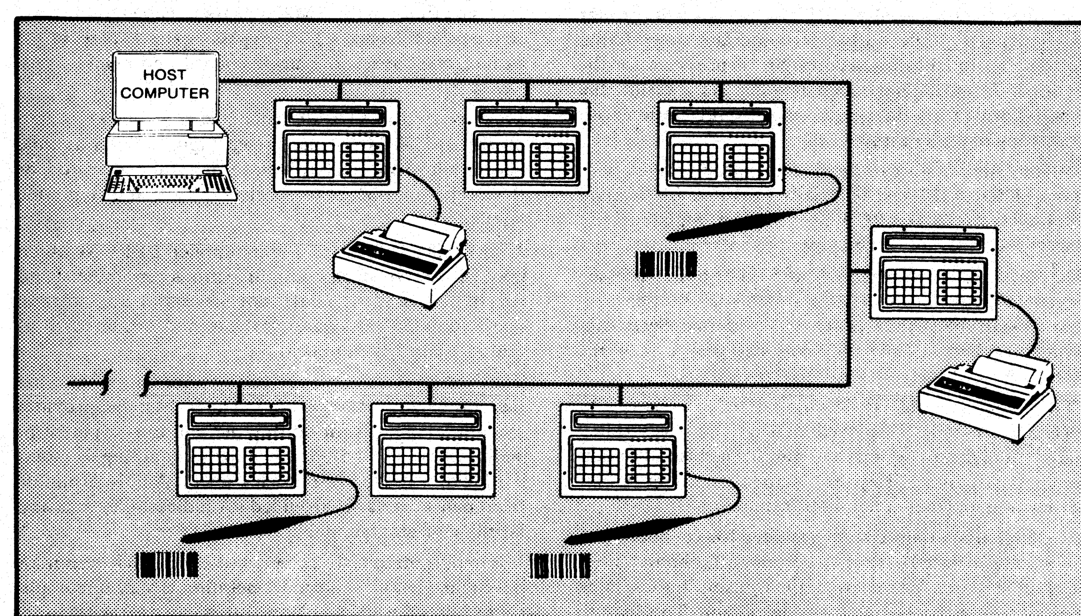


FIGURE 2. Multidrop Connection for Distributed Systems.

OPERATION

The TM200 transmits and receives blocks of up to 80 characters. The protocol is an extension of the command set used on other Microterminal models.

Internal operation of the TM200 is easily pictured as five buffer memories as seen in Figure 3. In addition, function messages are stored in separate RAM or ROM memory areas. The receive buffer receives incoming messages of up to 80 characters and when the message is complete, it is automatically transferred to the input buffer. The display buffer is then filled with the first 40 characters of the input message. The operator may then scroll the input message through the display buffer with the display acting as a "window" looking at a part of the input line.

The output buffer, which serves as temporary storage for keyboard or bar code entries, is transferred to the transmit buffer when the 'ENTER' key is pressed. At that time the message is transmitted to the host or, in polled operation, held until the host requests the message.

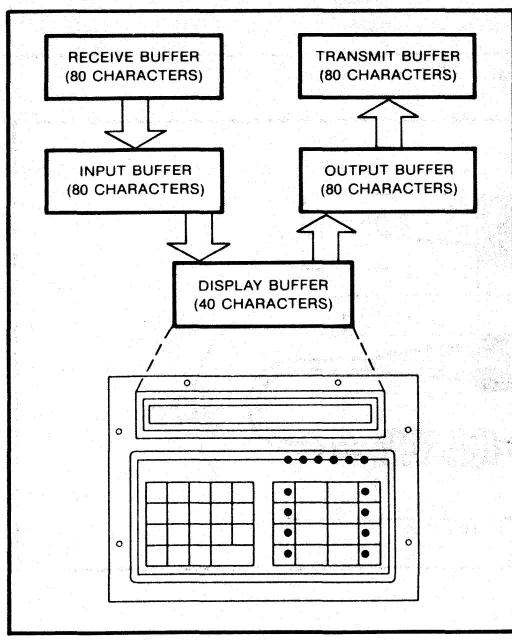


FIGURE 3. TM200 Internal Buffers.

MULTIDROP

Up to 63 TM200s may be operated on one host communication port. This is referred to as polled operation. A unique multidrop address may be set on each terminal allowing the host computer to control the flow of data. A number of command sequences are available to allow the host computer to control the operation of many features of the terminal.

SOFTWARE COMMANDS

Following is a summary of software commands recognized by the TM200. In polled operation, each command would be preceded by a terminal's two-digit multidrop address.

BASIC OPERATION	
[XX] (Message) (CR)	Input/output format
[XX] (ESC) A (CR)	Request transmit buffer
[XX] (ESC) B (CR)	Retransmit transmit buffer
[XX] (ESC) C (CR)	Clear input buffer
[XX] (ESC) D zz (Message) (CR)	Define function message
[XX] (ESC) D zz (CR)	Delete function message
[XX] (ESC) D 00 (CR)	Delete all function messages
[XX] (ESC) En (CR)	Output to LED A1
[XX] (ESC) Fn (CR)	Output to LED A2
[XX] (ESC) Gn (CR)	Display scrolling with n speed
[XX] (ESC) Hn (CR)	Display flashing
[XX] (ESC) In (CR)	Display blanking
[XX] (ESC) Jn (CR)	Keyboard locking
[XX] (ESC) K (CR)	Transmit input buffer
[XX] (ESC) L ddd (CR)	Set turnaround delay
[XX] (ESC) M (CR)	Clear output buffer
[XX] (ESC) T (Message) (CR)	Place (message) in input and output buffers
[XX] (ESC) Un (CR)	Keyboard audible indication
[XX] (ESC) W (CR)	Copy output buffer to transmit buffer
[XX] (ESC) Yn (CR)	TM900-compatible buffered mode
PRINTER CONTROL	
[XX] (ESC) Nn (CR)	Define printer interface
[XX] (ESC) On (CR)	Control printer from host
[XX] (ESC) Pn (CR)	Control printer from keyboard
[XX] (ESC) Qn (CR)	Request status of printer buffer
[XX] (ESC) R (CR)	Transmit from host to printer only
[XX] (ESC) S ddd (CR)	Output to TTL port B as well as to LEDs L2 to L8
BAR CODE CONTROL	
[XX] (ESC) Vn (CR)	Autowand (transmits bar code input without ENTER)
[XX] (ESC) Xn (CR)	Enables bar code wand.

[XX] optional multidrop address in polled mode.

CONTROL CHARACTERS

EOT	04	Suppress (CR) on transmission
BEL	07	Sound audible alarm
CR	0D	Message and command terminator
CAN	18	Clear receive, input buffers
EM	19	Clear receive buffer
RS	1E	Autotransmit function key terminator

BAR CODE

The TM200 with BCW200 decodes code 3 of 9 and full ASCII code 3 of 9 symbologies. Full ASCII code 3 of 9 is an extension of standard code 3 of 9 which allows encoding of all 128 ASCII characters by using two-character sequences to represent control characters and lower-case alphabetics. A command from the host computer selects whether the terminal will interpret bar codes as standard or full ASCII code 3 of 9.

Bar code input to the terminal is treated in much the same way as keyboard input. Two modes of operation are possible—Auto Wand and Manual Wand modes.

In Auto Wand mode, bar code data is added to the TM200's output buffer after a successful read. The buffer is then automatically transmitted as if the 'ENTER' key had been depressed.

In Manual Wand mode, bar code data is added to the output buffer after each read, but the buffer is not transmitted, thus allowing the concatenation of several bar code and/or keyboard entries in a single message to the host. Transmission of data in this mode occurs when the 'ENTER' key is manually depressed or a special bar code 'transmit' symbol (a start character followed stop character) is wanded.

The bar code wand is designed especially for comfortable holding and ease of use (Figure 5). A wide 0 to 45 degree scan angle (see Figure 4) allows bar codes to be read easily in a number of orientations. Successful reads are indicated by an audible tone.

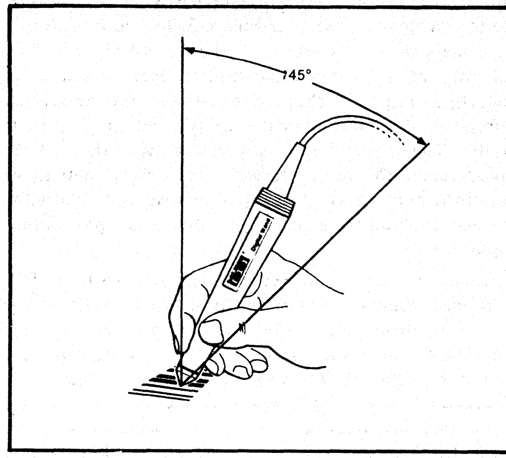


FIGURE 4. Scan Angle.

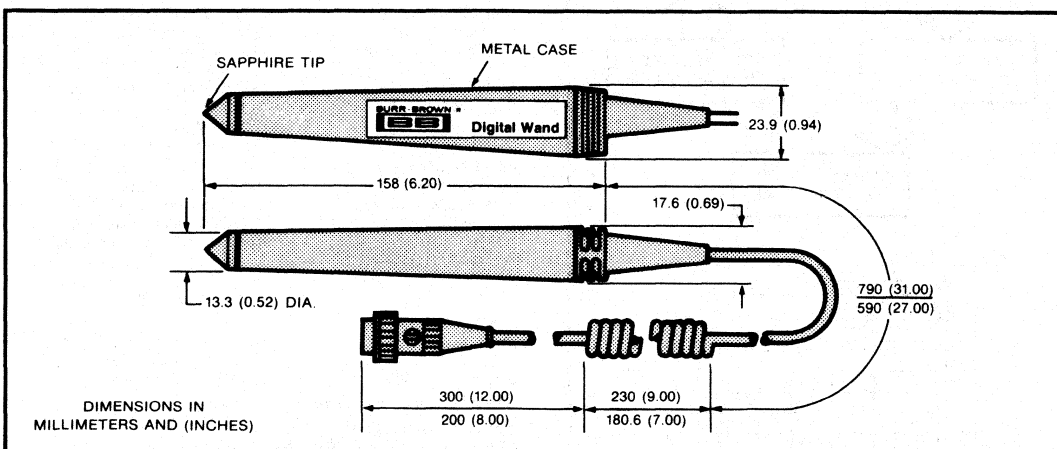


FIGURE 5. Bar Code Wand—BCW200.

SPECIFICATIONS

DISPLAY

Type .... Vacuum fluorescent (green)
Number of Characters 40
Matrix Size .... 5″ × 7″ with cursor
Character Height .... 0.21″
Message Buffer Size .... 80 characters
Status Indicators 4
Host-Controlled Indicators 10

KEYBOARD

Type .... Full-travel mechanical switch with moisture barrier
Material .... ABS
Spacing .... 0.75″ centers
Number 27
Programmable Functions ...... 16, max 76 characters per function key, max 220 characters total

COMMUNICATIONS

Jumper-selectable ..... RS-232, RS-422, 20mA I loop
Baud Rate 110–19,200
Code .... Asynchronous ASCII
Polled Operation .... Yes
Multidrop Address Range 63
Connector Type .... DB-25S (female, mates with TRW Cinch DB-25P)

USER EPROM

Type 2716
Programming .... Byte-mapped
Selectable Parameters .... Baud rate, parity, multidrop address, printer enable, function key messages

AUXILIARY INTERFACE

Printer .... Parallel
Digital Outputs: Number 10
Type .... Latched TTL
Connector .... 26-pin locking cable header (mates with 3M no. 3399)

BAR CODE READER (BCW200)

Wand Type .... Digital
Resolution .... 0.0075 inches (0.19mm)
Maximum Density .... 10.25 characters/inch
Light Source .... 700nm visible LED
Scan Angle .... 0–45 degrees from normal
Case .... Sealed metal
Tip .... Sapphire, sealed, replaceable
Cable .... Coiled, strain-relieved, 75″ nominal, 100 inches maximum extension
Connector .... DB-9 to terminal
Symbologies .... Code 3 of 9, Full ASCII Code 3 of 9
Modes .... Auto Wand (transmit on read), Manual Wand (accumulation with manual transmit)

POWER SUPPLY

7.5W, 5VDC ±3%, 1.5A max with options

PHYSICAL

Size .... 8.25″ × 11.00″ × 1.50″
Weight 4.7lbs
Case .... Steel
Keys .... ABS plastic
Display Window .... 30 mil polycarbonate

ENVIRONMENTAL

Operating Temperature .... 0°C to +60°C
Storage .... −20°C to +60°C
Relative Humidity 95%
Gasketed ..... Front panel, display window, keyboard
Resists .... Dust, liquid

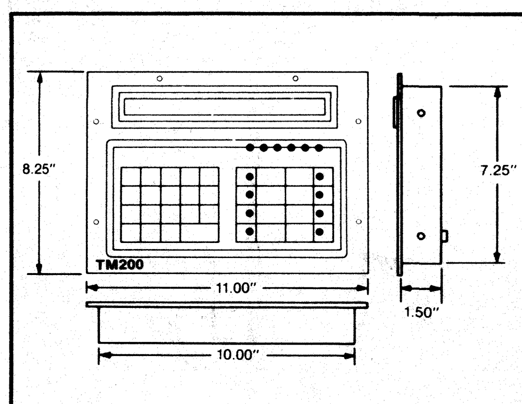


FIGURE 6. Mechanical Dimensions

INSTALLATION

The TM200 mounts easily through a wall or equipment panel (see Figure 7). A gasket allows a tight seal to keep out dirt and moisture.

All electrical connections are protected since they are located on the back of the unit, behind the panel.

Interface to the host system is provided by a standard DB-25 connector. This connector is pinout-compatible with TM71B and TM77B Microterminals. Printer interface and TTL outputs are provided through an auxiliary 26-pin connector.

Five-volt power for the unit may be connected either to the communications connector (as with previous Microterminal models) or to a separate two-position terminal block.

The BCW200 plugs into the back of the TM200 using a DB-9 connector. The wand itself features a sealed black metal case for heavy industrial environments. A coiled cable (extended length 75″) connects the wand to the terminal. The wand has a replaceable sapphire tip that is sealed to protect it from contamination by dirt and debris.

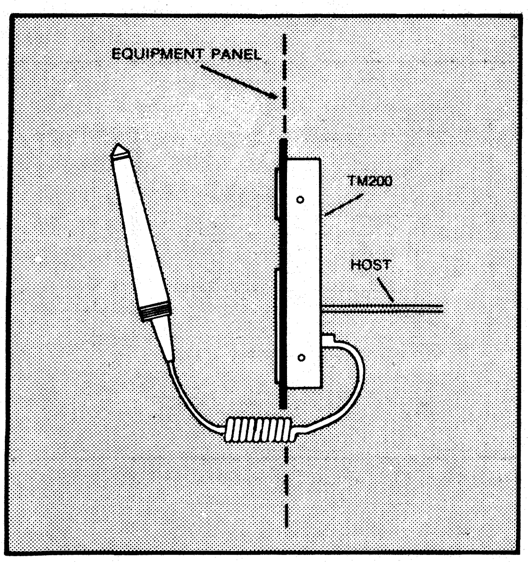


FIGURE 7. TM200 Installation.

ORDERING INFORMATION

TM200 is the full part number for TM200 Microterminal base model.

ACCESSORIES

Printer Cable (1 meter) SM50316
Bar Code Reader BCW200

COMPATIBLE PRODUCTS

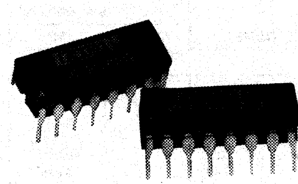
TM900 Transaction
Processor .... see TMC900 Brochure, LI-290

SPECIAL OPTIONS-Contact Factory

Ultra-High Resolution
Digital Wand .... 0.005in (0.13mm) for high density codes to 15.4 characters/inch
Infrared Digital Wand ...... 820nm LED light source

BURR-BROWN®

VFC100



Synchronized VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- FULL-SCALE FREQUENCY SET BY SYSTEM CLOCK, NO CRITICAL EXTERNAL COMPONENTS REQUIRED
- PRECISION 10V FULL-SCALE INPUT, 0.5% MAX GAIN ERROR
- ACCURATE 5V REFERENCE VOLTAGE
- EXCELLENT LINEARITY, 0.02% MAX AT 100kHz FS
  0.1% MAX AT 1MHz FS
- VERY-LOW GAIN DRIFT, 50ppm/°C

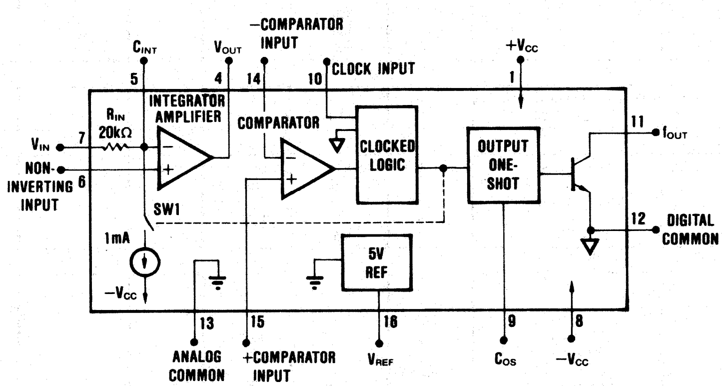
APPLICATIONS

- A/D CONVERSION
- PROCESS CONTROL
- DATA ACQUISITION
- VOLTAGE ISOLATION

DESCRIPTION

The VFC100 voltage-to-frequency converter is an important advance in VFCs. The well-proven charge balance technique is used, however, the critical reset integration period is derived from an external clock frequency. The external clock accurately sets an output full-scale frequency, eliminating error and drift from the external timing components required for other VFCs. A precision input resistor is provided which accurately sets a 10V full-scale input voltage. In many applications the required accuracy can be achieved without external adjustment.

The open collector active-low output provides fast fall time on the important leading edge of output pulses, and interfaces easily with TTL and CMOS circuitry. An output one-shot circuit is particularly useful to provide optimum output pulse widths for optical couplers and transformers to achieve voltage isolation. An accurate 5V reference is also provided which is useful for applications such as offsetting for bipolar input voltages, exciting bridges and sensors, and autocalibration schemes.



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SPECIFICATIONS

ELECTRICAL

At $T_A = +25°C$ and ±15VDC supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC100AG/SG MIN	VFC100AG/SG TYP	VFC100AG/SG MAX	VFC100BG MIN	VFC100BG TYP	VFC100BG MAX	UNITS
TRANSFER FUNCTION								
Voltage-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (V_{IN}/20V)$							
Gain Error[1]	FSR[2] = 100kHz		±0.5	±1		±0.2	±0.5	% of FSR
Linearity Error	FSR = 100kHz, over temp.		±0.01	±0.025		•	±0.02	% of FSR
	FSR = 500kHz, V_{OS} = 60pF		±0.015			•	±0.05	% of FSR
	FSR = 1MHz, C_{OS} = 60pF		±0.025			•	±0.1	% of FSR
Gain Drift[2]	FSR = 100kHz		±70	±100		±30	±50	ppm of FSR/°C
Referred to Internal V_{REF}			10	±25		10	±15	ppm of FSR/°C
Offset Referred to Input			±1	±3		±1	±2	mV
Offset Drift			±12	±100		±6.5	±25	μV/°C
Power Supply Rejection	Full supply range			0.01			•	%/V
Response Time	to Step Input Change	One period of new output frequency plus one clock period						
Current-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (I_{IN}/1mA)$							
Gain Error			±0.5	±1		±0.2	±0.5	% of FSR
Gain Drift[2]			±120	±200		±80	±140	ppm of FSR/°C
Frequency-to-Voltage Mode[3]	$V_{OUT} = 20V \times (f_{IN}/f_{CLOCK})$							
Gain Accuracy[1]	FSR = 100kHz		±0.5	±1		±0.2	±0.5	%
Linearity	FSR = 100kHz		±0.01	±0.025		•	±0.02	%
Input Resistor (R_{IN})								
Resistance		19.8	20	20.2	•	•	•	kΩ
Temperature Coefficient (T_C)[2]			±50	±100		•	•	ppm/°C
INTEGRATOR OP AMP								
V_{OS}[1]			±150	±1000		•	•	μV
V_{OS} Drift			±5			•		μV/°C
I_B			±50	±100		±25	±50	nA
I_{OS}			100	200		50	100	nA
A_{ol}	Z_{LOAD} = 5KΩ/10000pF	100	120		•	•		dB
CMRR		80	105		•	•		dBV
CM Range		−7.5		+0.1	•		•	V
V_{OUT} Range	Z_{LOAD} = 5kΩ/10000pF	−0.2		+12		•	•	V
Bandwidth			14			•		MHz
COMPARATOR INPUTS								
Input Bias Current (I_B)	$-11V < V_{IN} < +V_{CC}$			5			•	μA
CLOCK INPUT (referenced to digital common)								
Frequency (maximum operating)			4.0			•		MHz
Threshold Voltage			1.4			•		V
	Over temperature	0.8		2.0	•		•	V
Voltage Range		$-V_{CC}$		$+V_{CC}$	•		•	V
Input Current	$-V_{CC} < V_{CLOCK} < +V_{CC}$		0.5	5		•	•	μA
Rise Time				2			•	μsec
OPEN COLLECTOR OUTPUT (referenced to digital common)								
V_{OL}	I_{OUT} = 10mA			0.4			•	V
I_{OL}				15			•	mA
I_{OH} (off leakage)	V_{OH} = 30V		.01	10		•	•	μA
Delay Time, positive clock edge to output pulse			300			•		nsec
Fall Time			100			•		nsec
Output Capacitance			5			•		pF
OUTPUT ONE-SHOT								
Pulse Width Out	Nominal PW_{OUT} = (5nsec/pF) × C_{OS} − 90nsec; C_{OS} = 300pF	1	1.4	2	•	•	•	μsec
REFERENCE VOLTAGE								
Accuracy	No load	4.90	5.0	5.10	4.95	•	5.05	V
Drift[2]			±60	±150		±40	±100	ppm/°C
Current Output	(Sourcing capability)	10				•		mA
Power Supply Rejection				0.015			0.015	%/V
Output Impedance			0.5	2		•	•	Ω
POWER SUPPLY								
Rated Voltage			±15			•		V
Operating Voltage Range (see Figure 9)	$+V_{CC}$	+7.5		+28.5	•		•	V
	$-V_{CC}$	−7.5		−28.5	•		•	V
Total Supply	$+V_{CC} - (-V_{CC})$	15		36	•		•	V
Digital Common		$-V_{CC} + 2$		$+V_{CC} - 4$	•		•	V
Quiescent Current: $+I_{CC}$	Over temperature		10.6	15		•	•	mA
$-I_{CC}$			9.6	15		•	•	mA

ELECTRICAL (CONT)

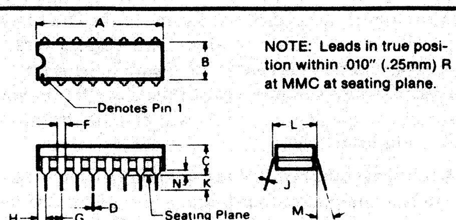
At $T_A = +25°C$ and ±15VDC supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC100AG/SG MIN	VFC100AG/SG TYP	VFC100AG/SG MAX	VFC100BG MIN	VFC100BG TYP	VFC100BG MAX	UNITS
TEMPERATURE RANGE								
Specification	AG/BG	−25		+85	*		*	°C
	SG	−55		+125				°C
Storage	AG/BG/SG	−65		+150	*		*	°C
θ Junction—ambient			150			*		°C/W
θ Junction—case			100			*		°C/W

*Specification same as AG grade.

NOTES: (1) Offset and gain error can be trimmed to zero. See text. (2) Specified by the box method: (Max. − Min.) ÷ (Avg. × ΔT). (3) Refer to detailed timing diagram in Figure 16 for frequency input signal timing requirements.

MECHANICAL



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.760	.885	19.30	22.48
B	.220	.280	5.59	7.11
C		.200		5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100		2.54	
L	.300 BASIC		7.62 BASIC	
M	–	15°		15°
N	.020	.050	0.51	1.27

PIN CONFIGURATION

$+V_{cc}$	1	16	V_{ref}
NC	2	15	+ COMPARATOR IN
NC	3	14	−COMPARATOR IN
INTEGRATOR OUT	4	13	ANALOG COMMON
C_{int}	5	12	DIGITAL COMMON
NONINVERTING IN	6	11	f_{out}
V_{in}	7	10	CLOCK INPUT
$-V_{cc}$	8	9	C_{os}

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($+V_{cc}$ to $-V_{cc}$) 36V
$+V_{cc}$ to Analog Common 28V
$-V_{cc}$ to Analog Common 28V
Integrator Out Short-Circuit-to-Ground .... Indefinite
Integrator Differential Input .... ±10V
Integrator Common-Mode Input .... $-V_{cc}$ +5V to +2V
V_{IN} (pin 7) .... $\pm V_{cc}$
Clock Input .... $\pm V_{cc}$
V_{REF} Out Short-Circuit-to-Ground .... Indefinite
Pin 9 (C_{OS}) .... 0 to $+V_{cc}$
f_{OUT} (referred to digital common) .... −0.5V to 36V
Digital Common .... $\pm V_{cc}$
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (soldering 10sec) .... 300°C

VFC100 (X) G

Basic Model Number

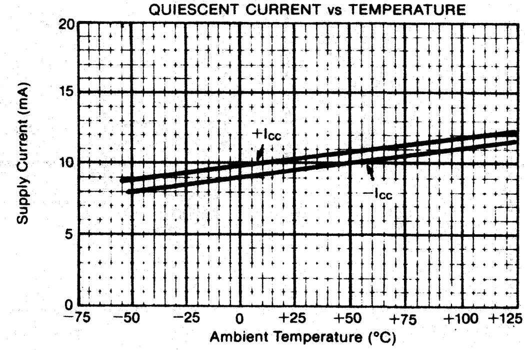
Performance Code
A, B = −25°C to +85°C
S = −55°C to +125°C

Ceramic Package

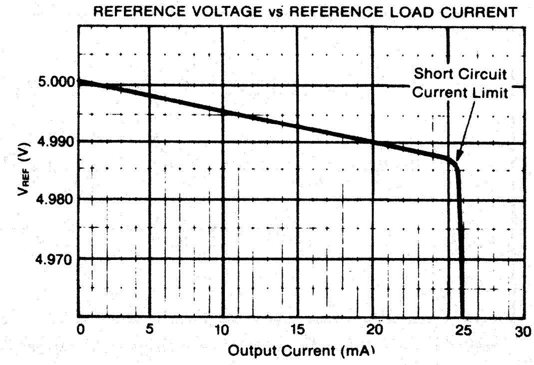
TYPICAL PERFORMANCE CURVES

At +25°C, $\pm V_{cc}$ = 15VDC, and in circuit of Figure 1 unless otherwise specified.

QUIESCENT CURRENT vs TEMPERATURE



REFERENCE VOLTAGE vs REFERENCE LOAD CURRENT



THEORY OF OPERATION

The VFC100 monolithic voltage-to-frequency converter provides a digital pulse train output with an average frequency proportional to the analog input voltage. The output is an active low pulse of constant duration, with a repetition rate determined by the input voltage. Falling edges of the output pulses are synchronized with rising edges of the clock input.

Operation is similar to a conventional charge balance VFC. An input operational amplifier (Figure 1) is configured as an integrator so that a positive input voltage causes an input current to flow in R_{IN}. This forces the integrator output to ramp negatively. When the output of the integrator crosses the reference voltage (5V), the comparator trips, activating the clocked logic circuit. Once activated, the clocked logic awaits a falling edge of the clock input, followed by a rising edge (see Figure 2). On the rising edge, switch S1 is closed for one complete clock cycle, causing the reset current, I_1 to switch to the integrator input. Since I_1 is larger than the input current, I_{IN}, the output of the integrator ramps positively during the one clock cycle reset period. The clocked logic circuitry also generates a VFC output pulse during the reset period.

Unlike conventional VFC circuits, the VFC100 accurately derives its reset period from an external clock frequency. This eliminates the critical timing capacitor required by other VFC circuits. One period (from rising edge to rising edge) of the clock input determines the integrator reset period.

When the negative-going integration of the input signal crosses the comparator threshold, integration of the input signal will continue until the reset period can start (awaiting the necessary transitions of the clock). Output pulses are thus made to align with rising edges of the external clock. This causes the instantaneous output frequency to be a subharmonic of the clock frequency. The average frequency, however, will be an accurate analog of the input voltage.

A full scale input of 10V (or an input current of 0.5mA) causes a nominal output frequency equal to one half the

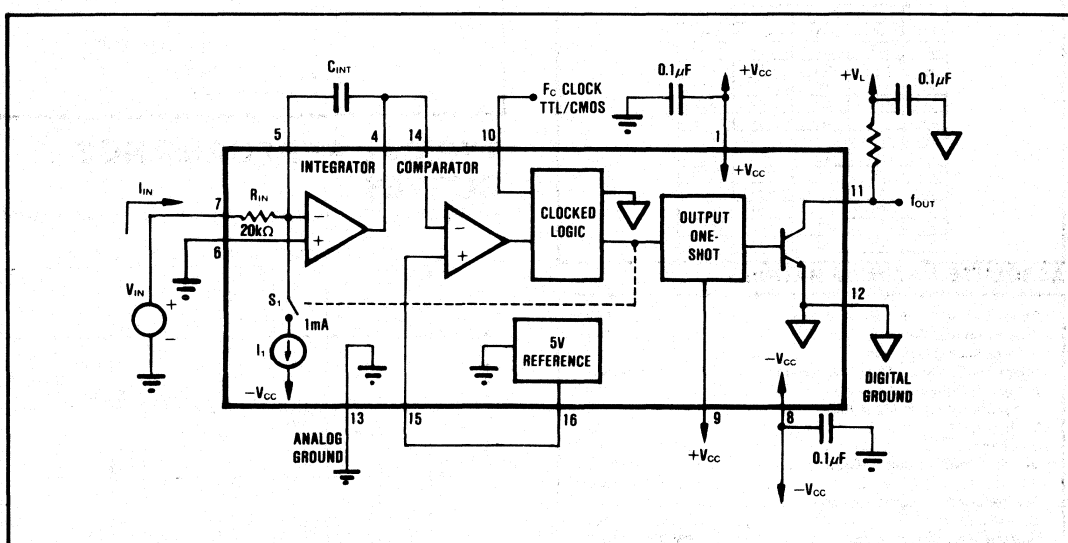


FIGURE 1. Circuit Diagram for Voltage-to-Frequency Mode.

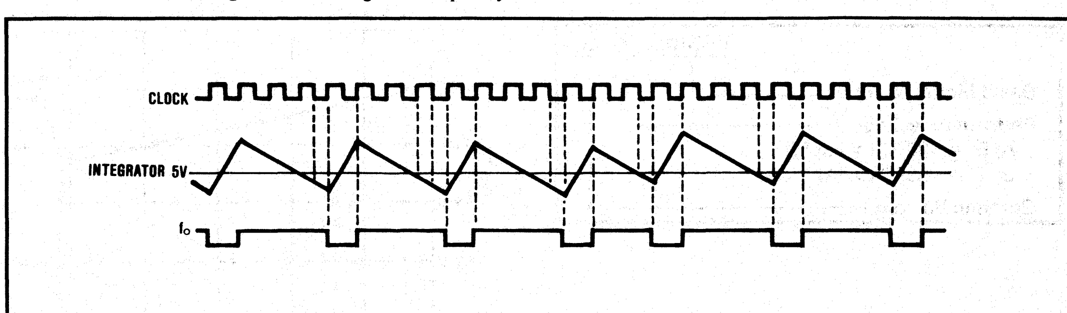


FIGURE 2. Timing Diagram for Voltage-to-Frequency Mode.

clock frequency. The transfer function is

$$f_{OUT} = (V_{IN}/20V)\, f_{CLOCK}$$

Figure 3 shows the transfer function graphically. Note that inputs above 10V (or 0.5mA) do not cause an increase in the output frequency. This is an easily detectable indication of an overrange input. In the overrange condition, the integrator amplifier will ramp to its negative output swing limit. When the input signal returns to within the linear range, the integrator amplifier will recover and begin ramping upward during the reset period.

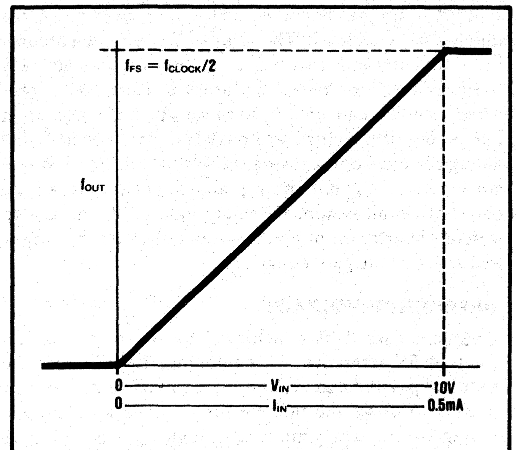
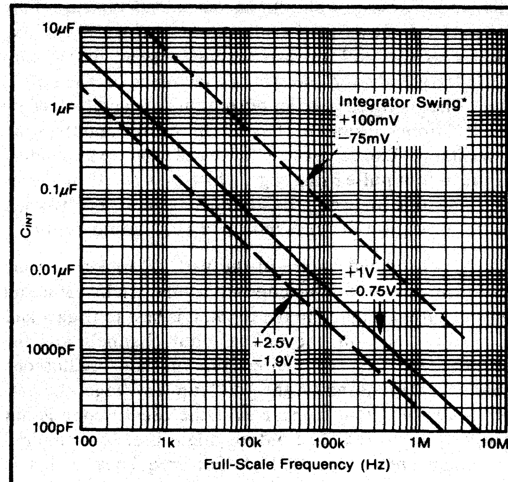


FIGURE 3. Transfer Function for Voltage-to-Frequency Mode.

INSTALLATION AND OPERATING INSTRUCTIONS

The integrator capacitor C_{INT} (see Figure 1) affects the magnitude of the integrator voltage waveform. Its absolute accuracy is not critical since it does not affect the transfer function. This allows a wide range of capacitance to produce excellent results. Figure 4 facilitates choosing an appropriate standard value to assure that the integrator waveform voltage is within acceptable limits. Good dielectric absorption properties are required to achieve best linearity. Mylar®, polycarbonate, mica, polystyrene, Teflon® and glass types are appropriate choices. The choice in a given application will depend on the particular value and size considerations. Ceramic capacitors vary considerably from type to type and some produce significant nonlinearities. Polarized capacitors should not be used.

Deviation from the nominal recommended +1V to −0.75V integrator voltage (as controlled by the integrator capacitor value) is permissible and will have a negligible effect on VFC operation. Certain situations may make deviations from the suggested integrator swing highly desirable. Smaller integrator voltages, for instance, allow more "headroom" for averaging noisy input signals. The VFC is a fully integrating input converter, able to reject large levels of interfering noise. This ability is limited only by the output voltage swing range of the integrator amplifier. By setting a small integrator voltage swing using a large C_{INT} value, larger levels of noise can be integrated without output saturation and loss of accuracy. For instance, with a 50kHz full-scale output and $C_{INT} = 0.1\mu F$, the circuit in Figure 1 can accurately average an input through the full 0 to 10V input range with 1V p-p superimposed 60Hz noise.



* This is the maximum swing of the integrator output voltage referred to the comparator noninverting input voltage.

FIGURE 4. Integrator Capacitor Selection Graph.

The integrator output voltage should not be allowed to exceed +12V or −0.2V, otherwise saturation of the operational amplifier could cause inaccuracies. Operation with positive power supplies less than +15V will limit the output swing of the integrator operational amplifier. Smaller integrator voltage waveforms may be required to avoid output saturation of the integrator amplifier. See "Power Supply Considerations" for information on low voltage operation.

The maximum integrator voltage swing requirement is nearly symmetrical about the comparator threshold voltage (see Figure 12). One-third greater swing is required above the threshold than below it. Maximum demand on positive integrator swing occurs at low scale, while the negative swing is greatest just below full scale.

CLOCK INPUT

The clock input is TTL- and CMOS-compatible. Its input threshold is approximately 1.4V (two diode voltage drops) referenced to digital ground (pin 12). The clock "high" input may be standard TLL or may be as high as $+V_{CC}$. A CMOS system, for instance, could be powered directly from the positive supply voltage of the VFC. The clock input has a high input impedance, so no special drivers are required for CMOS circuits. Rise time in the transition region from 0.5V to 2V must be less than 2µsec for proper operation.

OUTPUT

The frequency output is an open collector current-sink transistor. Output pulses are active low such that the output transistor is on only during the reset integration period (see Shortened Output Pulses). This minimizes power dissipation over the full frequency range and provides the fastest logic edge at the beginning of the output pulse where it is most desirable.

Interface to a logic circuit would normally be made using a pull-up resistor to the logic power supply. Selection of the pull-up resistor should be made such that no more than 15mA flows in the output transistor. The actual choice of the pull-up resistor may depend on the full-scale frequency and the stray capacitance on the output line. The rising edge of an output pulse is determined by the RC time constant of the pull-up resistor and the stray capacitance. Excessive capacitance will produce a rounding of the output pulse rising edge, which may create problems driving some logic circuits. If long lines must be driven, a buffer or digital line transmitter circuit should be used.

The synchronized nature of the VFC100 makes viewing its output on an oscilloscope somewhat tricky. Since all output pulses align with the clock, it is best to trigger and view the clock on one of the input channels and the output can then be viewed on another oscilloscope channel. Depending on the VFC input voltage, the output waveform may appear as if the oscilloscope is not properly triggered. The output might best be visualized by imagining a constant output frequency which is locked to a submultiple of the clock frequency with occasional extra pulses or missing pulses to create the necessary average frequency. It is these extra or missing pulses that make the output waveform appear as if the oscilloscope is not properly triggered. This is normal. Experimentation with the input voltage and oscilloscope triggering will generally allow a stable view of the output and provides an understanding of its nature.

SHORTENED OUTPUT PULSES

In normal operation, the negative output pulse duration is equal to one period of the clock input. Shorter output pulses may be useful in driving optical couplers or transformers for voltage isolation or noise rejection. This can be accomplished by connecting capacitor C_{OS} as shown in Figure 5. Pin 9 may be connected to $+V_{CC}$, deactivating the output one-shot circuit. The value of C_{OS} is chosen according to the curve in Figure 6. Output pulses cannot be made to exceed one clock period in duration. Thus, a C_{OS} value which would create an output pulse which is longer than one period of the clock will have the same effect as disabling the one-shot, causing the output pulse to last one clock period. The minimum practical pulse width of the one-shot circuit is approximately 100nsec. Using C_{OS} to generate shorter output pulses does not affect the output frequency or the gain equation.

REFERENCE VOLTAGE

Excellent gain drift is achieved by use of a precision internal 5V reference. This reference is brought to an external pin and can be used for a variety of purposes. It is used to offset the noninverting comparator input in voltage-to-frequency mode (although a precise voltage is not requried for this function). It is very useful in many other applications such as offsetting the input to handle bipolar input signals. It can source up to 10mA and sink

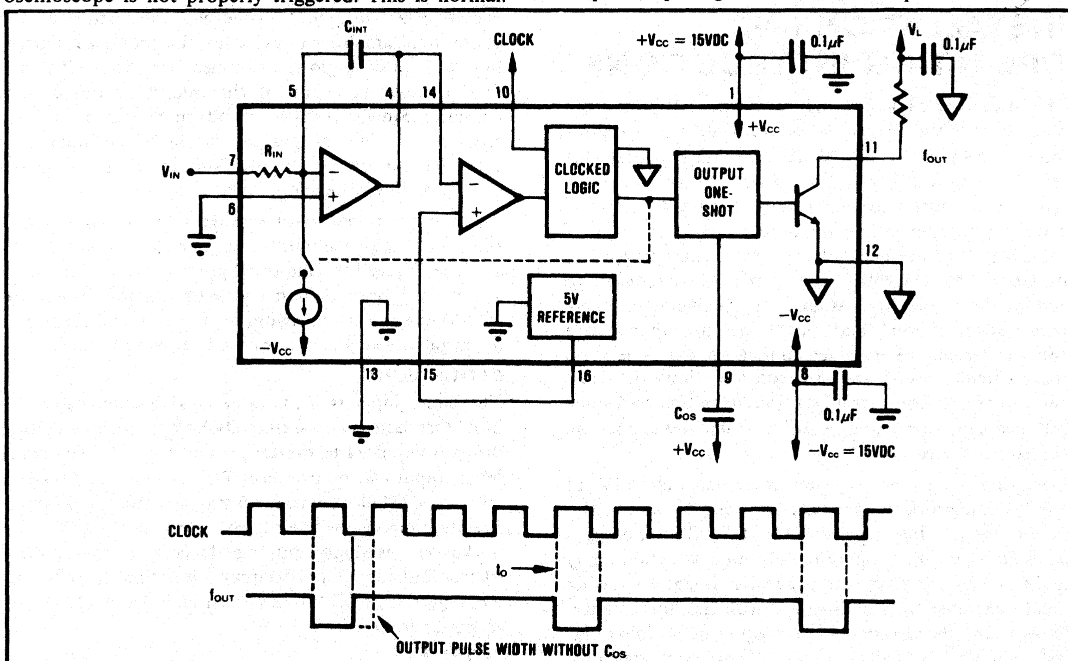


FIGURE 5. Circuit and Timing Diagram for Shortened Output Pulses.

100μA. Heavy loading of the reference will change the gain of the VFC as well as affecting the external reference voltage. For instance, a 10mA load interacting with a 0.5Ω typical output impedance will change the VFC gain equation and reference voltage by 0.1%.

Figure 7 shows the reference used to offset the VFC transfer function to convert a −5V to +5V input to zero to 500kHz output. The circuit in Figure 8 uses the reference to excite a 300Ω bridge transducer. R_1 provides the majority of the current to the bridge while the V_{REF} output supplies the balance and accurately controls the bridge voltage. The VFC gain is inversely proportional to the reference voltage, V_{REF}. Since the bridge gain is directly proportional to its excitation voltage, the two equal and opposite effects cancel the effect of reference voltage drift on gain.

The reference output amplifier is specifically designed for excellent transient response to provide precision in a noisy environment. Although not required for normal operation, a 0.05μF bypasss capacitor from the reference

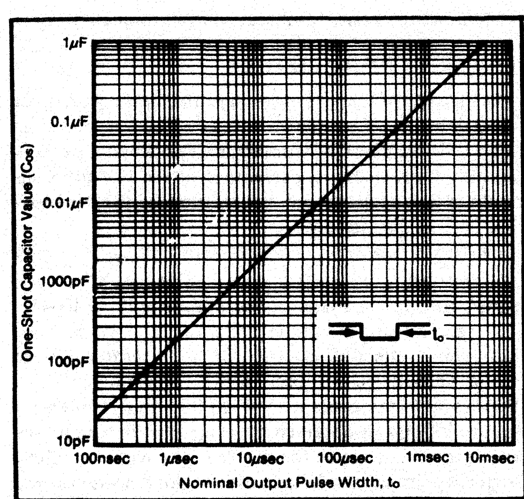


FIGURE 6. Output One-Shot Capacitor Selection Graph.

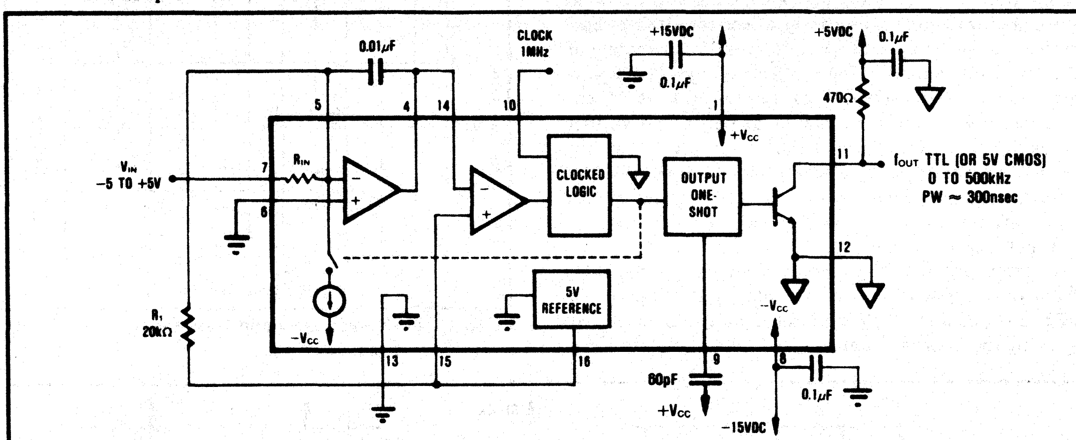


FIGURE 7. Circuit Diagram for Bipolar Input Voltages.

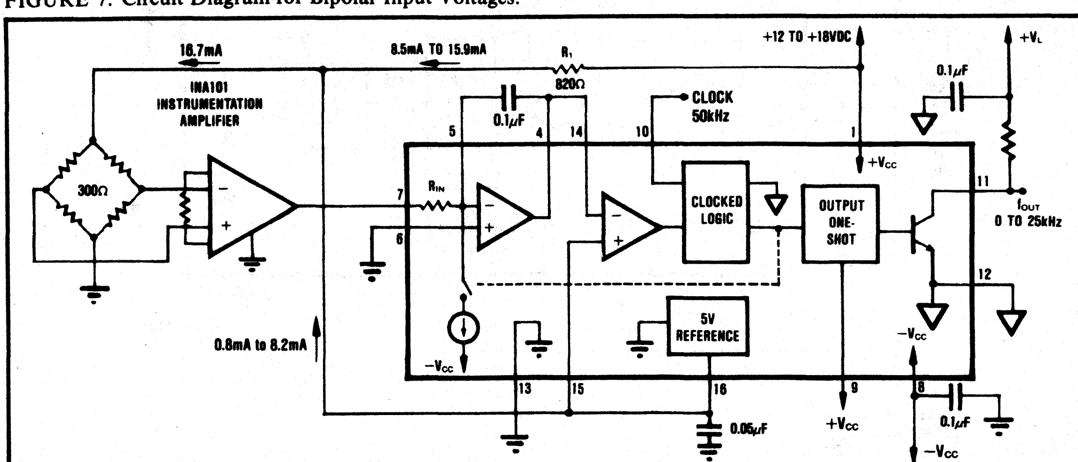


FIGURE 8. Circuit Diagram for Bridge Excitation Using V_{REF}.

output to analog ground (pin 13) may improve the rejection of digital noise from external circuitry.

OTHER INPUT VOLTAGE RANGES

The internal input resistor, $R_{IN} = 20k\Omega$, sets a full-scale input of 10V. Other input ranges can be created by using an external gain set resistor connected to pin 5. Since the excellent temperature drifts of the VFC100 are achieved by careful matching of internal temperature coefficients, use of an external gain set resistor will generally degrade this drift. Using an external resistor to set the gain, the resulting gain drift would be equal to the sum of the external resistor drift and the specified current gain drift of the VFC100. Different voltage input ranges are best implemented by using the internal input resistor, R_{IN}, in series or parallel with a high quality external resistor, thus maintaining as much of the precision temperature tracking as possible.

For best drift performance, the adjustment range of a fine gain trim should be made as narrow as practical. R_1 and R_2 in Figure 9 allow gain adjustment over a ±1% range (adequate to trim the 100kHz FS gain error to zero) and will not significantly affect the drift performance of the VFC100. R_3, R_4, and R_5 allow trimming of the integrator amplifier input offset voltage. The adjustment range is determined by the ratio of R_4 to R_5. Accurate end-point calibration would be performed by first adjusting the offset trim so that zero volts input just causes all output pulses to cease. The gain trim is then adjusted for the proper full-scale output frequency with an accurate full-scale output frequency with an accurate full scale input voltage.

A different input voltage range could also be made by using only a portion of the normal input range of the VFC. For instance, a 2V full-scale input could be created by using the internal input resistor and a clock frequency of 10 times the desired full-scale output frequency.

LINEARITY PERFORMANCE

The linearity of the VFC100 is specified as the worst-case deviation from a straight line defined by low scale and high scale endpoint measurements. This worst-case deviation is expressed as a percentage of the 10V full-scale input. All units are tested and guaranteed for the specified level of performance.

Linearity performance and gain error change with full-scale operating fequency as shown in Figure 10. Figure 11 shows the typical shape of the nonlinearity at 100kHz full scale. Integrator voltage swing (determined by C_{INT}) has a minor effect on linearity. Small integrator voltage swing typically leads to best linearity performance.

Best linearity performance at high full-scale frequencies (above 500kHz) is obtained by using short output pulses with a one-shot capacitor of 60pF. As with any high-frequency circuit, careful attention to good power supply

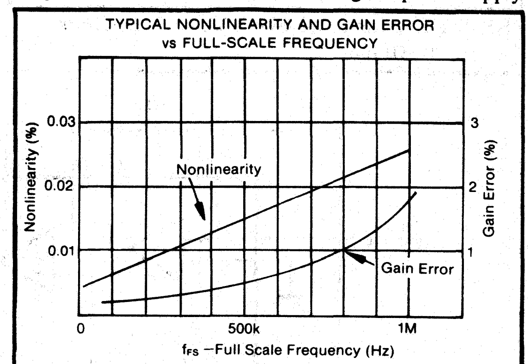


FIGURE 10. Nonlinearity and Gain Error vs Full Scale Frequency.

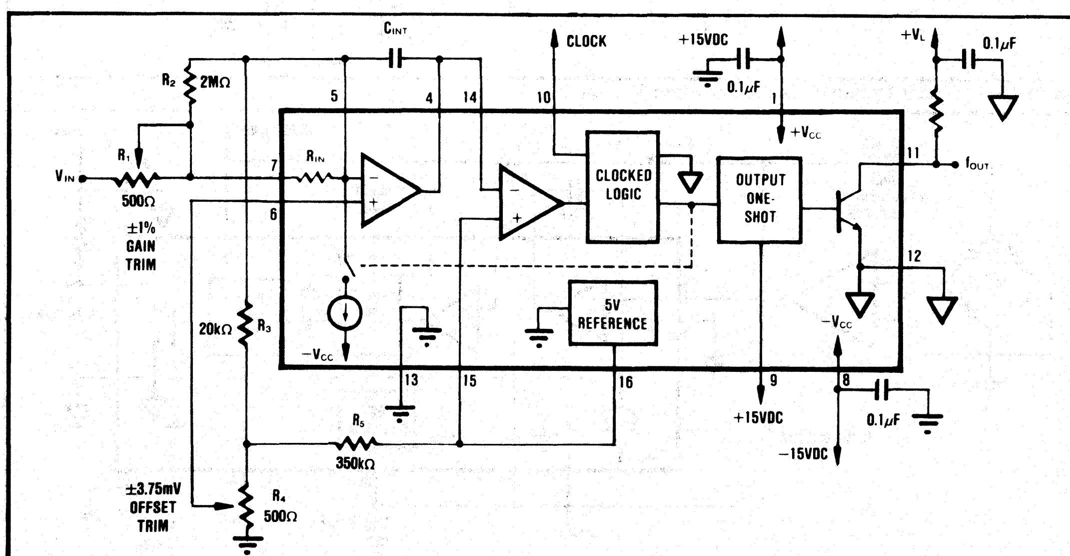


FIGURE 9. Circuit Diagram for Fine Offset and Gain Trim.

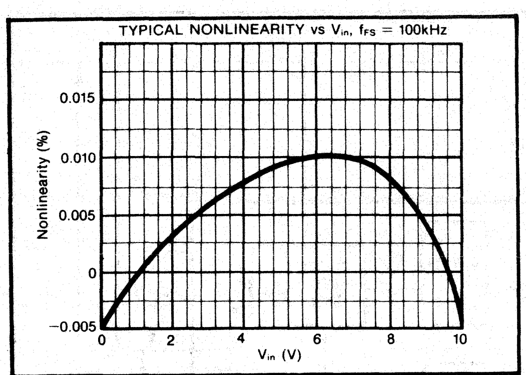


FIGURE 11. Typical Nonlinearity vs V_{IN}.

bypassing techniques (see "Power Supplies and Grounding") is also required.

TEMPERATURE DRIFT

Conventional VFC circuits are affected significantly by external component temperature drift. Drift of the external input resistor and timing capacitor required with these devices may easily exceed the specified drift of the VFC itself.

When used with its internal input resistor, the gain drift of the complete VFC100 circuit is totally determined by the performance of the VFC100. Gain drift is specified at a full scale output frequency of 100kHz. Conventional VFC circuits usually specify drift at 10kHz and degrade significantly at higher operating frequency. The VFC-100's gain drift remains excellent at higher operating frequency, typically remaining within specification at f_{FS} = 1MHz.

Drift of the external clock frequency directly affects the output frequency, but by using a common clock for the VFC and counting circuitry this drift can be cancelled (see Counting the Output).

POWER SUPPLIES AND GROUNDING

Separate analog and digital grounds are provided on the VFC100 and it is important to separate these grounds to attain greatest accuracy. Logic sink current flowing in the f_{OUT} pin is returned to the digital ground. If this "noisy" current were allowed to flow in analog ground, errors could be created. Although analog and digital grounds may eventually be connected together at a common point in the circuitry, separate circuit connections to this common point can reduce the error voltages created by varying currents flowing through the ground return impedance. The +5V V_{REF} pin is referenced to analog ground.

The power supplies should be well bypassed using capacitors with low impedance at high frequency. A value of 0.1μF is adequate for most circuit layouts.

The VFC100 is specified for a nominal supply voltage of ±15V. Supply voltages ranging from ±7.5V to ±18V may be used. Either supply can be up to 28V as long as the total of both does not exceed 36V. Steps must be taken, however, to assure that the integrator output does not exceed its linear range. Although the integrator output is capable of 12V output swing with 15V power supplies, with 7.5V supplies, output swing will be limited to approximately 4.5V. In this case, the comparator input cannot be offset by directly connecting to the 5V reference output pin. The comparator input must be connected to a lower voltage point (approximately 2V). This allows the integrator output to operate around a lower voltage point, assuring linear operation. This threshold voltage does not affect the accuracy or drift of the VFC as long as it is not noisy. It should not be made too

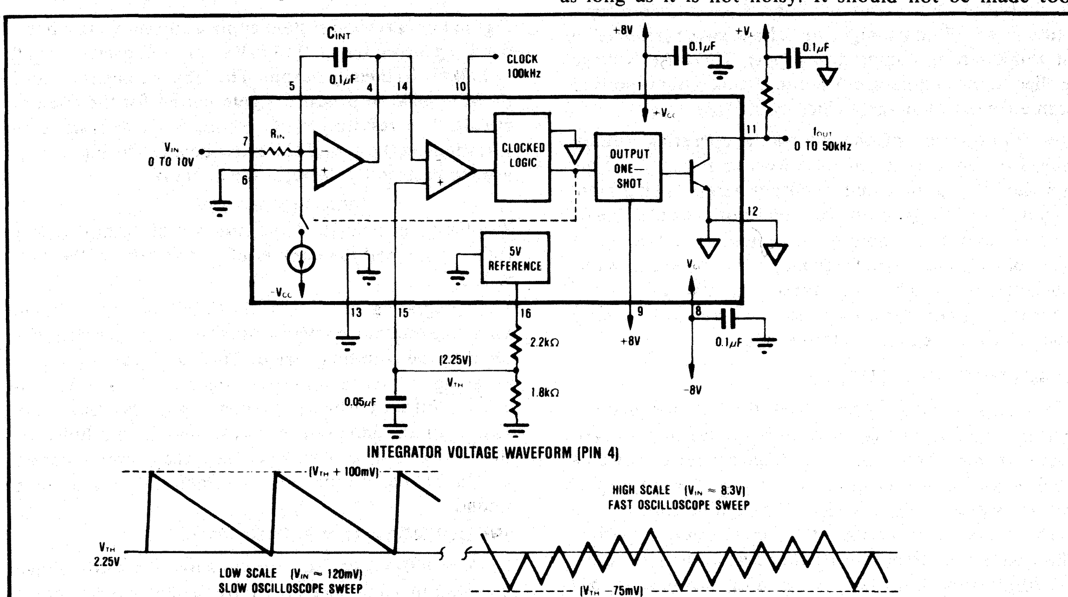


FIGURE 12. Circuit Diagram and Integrator Voltage Waveform for Low Power Supply Voltage Operation.

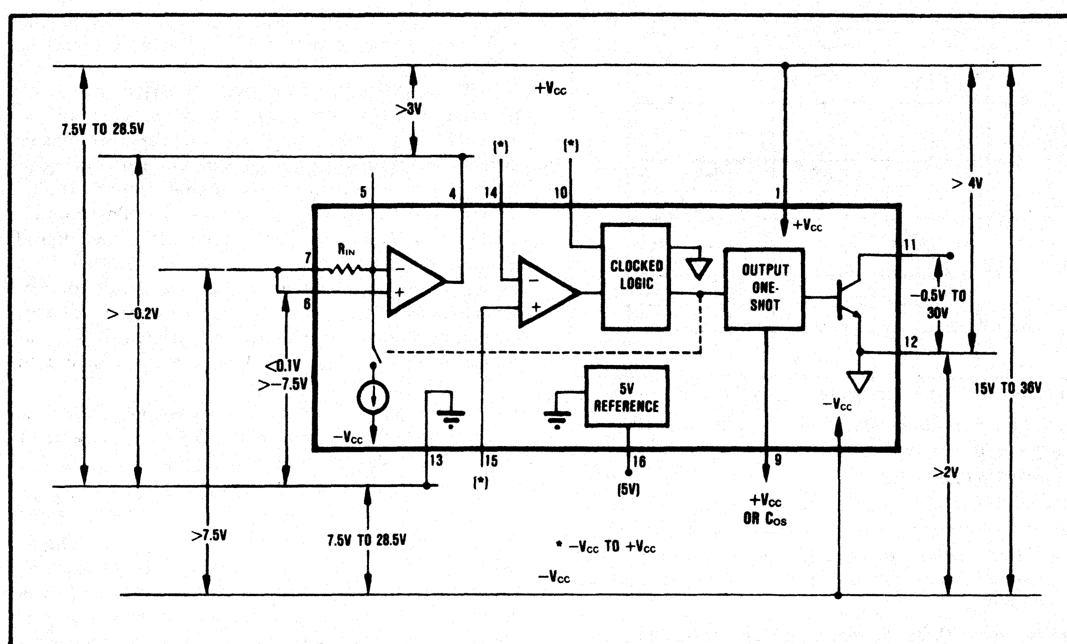


FIGURE 13. Relationships of Allowable Voltages.

small, however, or the negative output limitation of the integrator (−0.2V) may cause saturation. Additionally, a large integrator capacitor may be used to limit the required integrator waveform swing to approximately 100mV (see Integrator Capacitor).

Figure 12 shows a circuit for operating from the minimum power supplies, avoiding saturation of the integrator amplifier and loss of accuracy. C_{INT} is chosen for a +100mV to −75mV integrator voltage swing (referred to the noninverting comparator input). The offset voltage applied to the comparator's noninverting input is derived from a resistive voltage divider from V_{REF}.

The relationships of the allowable operating voltage ranges on important pins is shown in Figure 13. Note that the integrator amplifier output cannot swing more than 0.2V below ground. Although this is not "normal" for an operational amplifier, a special internal design of this type optimizes high frequency performance. It is this charactersitic which necessitates the offsetting of the noninverting comparator input in voltage-to-frequency mode to avoid negative output swing.

COUNTING THE OUTPUT

In evaluation and use of the VFC100, you may want to measure the output frequency with a frequency counter. Since synchronization of the VFC100 causes it to await a clock edge for any given output pulse, the output frequency is essentially quantized. The quantized steps are equal to one clock period of the counting gate period. The quantizing error can be made arbitrarily small by counting with long gate times. For instance, a one second counter gate period and a 100kHz full-scale frequency has a one part in 100,000 resolution. Many of the more sophisticated laboratory frequency counters, however, use period measurement schemes to count the input frequency quickly. These instruments work equally well, but the gate period must be set appropriately to achieve the desired count resolution. Short gate periods will produce many digits of "accuracy" in the display, but the results may be very inaccurate.

Figure 14 is a typical system application showing a basic counting technique. A 0 to 10V input is converted to a 0 to 100kHz frequency output. The VFC's clock is divided by M = 4000 to produce a gate period for the counter circuit. The resulting VFC count, N, is insensitive to variations in the actual clock frequency. The input voltage represented by the resulting count is

$$V_{IN} = (N/M)\,20V$$

Resolution is related to the number of counts at full scale, or one-half the number of clock pulses in the gate period.

The integrating nature of the VFC is important in achieving accurate conversions. The integrating period is equal to the counting period. This can be used to great advantage to reject unwanted signals of a known frequency. Figure 15 shows that response nulls occur at the inverse of the integration period and its multiples. If 60Hz is to be rejected, for instance, the counting period should be made equal to, or a multiple of 1/60 of a second.

FREQUENCY-TO-VOLTAGE MODE

The VFC100 can also function as a frequency-to-voltage converter by applying an input frequency to the comparator input as shown in Figure 16. The input resistor, R_{IN}, is connected as a feedback resistor. The voltage at the

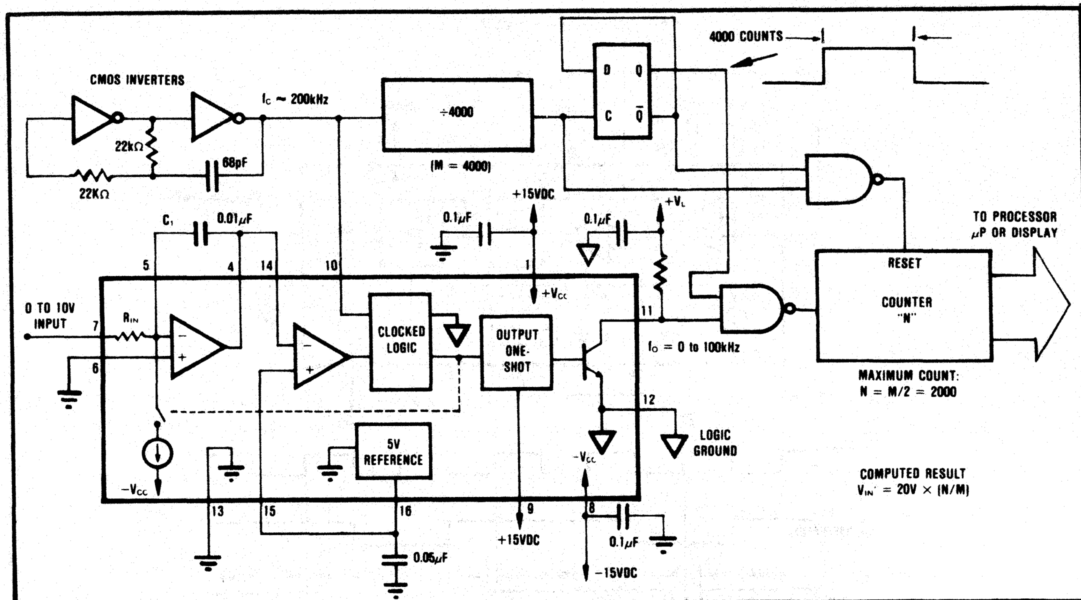


FIGURE 14. Diagram of a Voltage-to-Frequency Converter and Counter System.

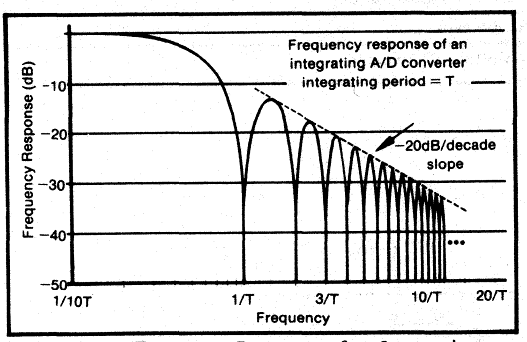


FIGURE 15. Frequency Response of an Integrating Analog-to-Digital Converter.

integrator amp output is proportional to the ratio of the input frequency to the clock frequency. The transfer function is

$$V_{OUT} = (f_{IN}/f_{CLOCK})\ 20V$$

This transfer function is complementary to the voltage-to-frequency mode transfer function, making voltage-to-frequency-to-voltage conversions simple and accurate.

Direct coupling of the input frequency to the comparator is easily accomplished by driving both comparators with complementary frequency input signals. Alternatively, one of the comparator inputs can be biased at half the logic voltage (using V_{REF} and a voltage divider) and the other input driven directly.

The proper timing of the input frequency waveform is shown in Figure 16. The input pulse should go low for one clock cycle, centered around a falling edge of the clock. The minimum acceptable input pulse width must fall no later than 200nsec before a negative clock edge and rise no sooner than 200nsec after the falling clock edge. An input pulse which remains low for more than one falling edge of the clock will produce incorrect output voltages. Positive (active high) input pulses can be accepted by reversing the connections to pins 14 and 15. Figure 17 shows a digital conditioning circuit which will accept any input duty cycle and provide the proper pulse width to the comparator. Each rising edge at this circuit's input generates the required negative pulse at the inverting comparator input. The noninverting comparator is driven by a complementary signal.

The integrator amplifier output is designed to drive up to 10,000pF and 5kΩ loads in frequency-to-voltage mode. This allows driving long lines in a large system.

Ripple voltage in the voltage output is unavoidable and is inversely proportional to the value of the integrator capacitor. Figure 18 shows the output ripple and settling time as a function of the C_{INT} value.

The ripple frequency is equal to the input frequency. Its magnitude can be reduced by using a large integrator capacitor value, but at the sacrifice of slow settling time at the voltage output in response to an input frequency change. The settling time constant is equal to $R_{IN} \times C_{INT}$. A better compromise between output ripple and settling time can be achieved by using a moderately low integrator capacitor value and adding a low-pass filter on the analog output. The cutoff frequency of the filtter should be made below the lowest expected input frequency to the frequency-to-voltage converter.

The system in Figure 20 makes use of both voltage-to-frequency and frequency-to-voltage mode to send a signal across an optically-isolated barrier. This technique is useful not only for providing safety in the presence of high voltages, but for creating high noise rejection in electrically noisy environments. The use of a common

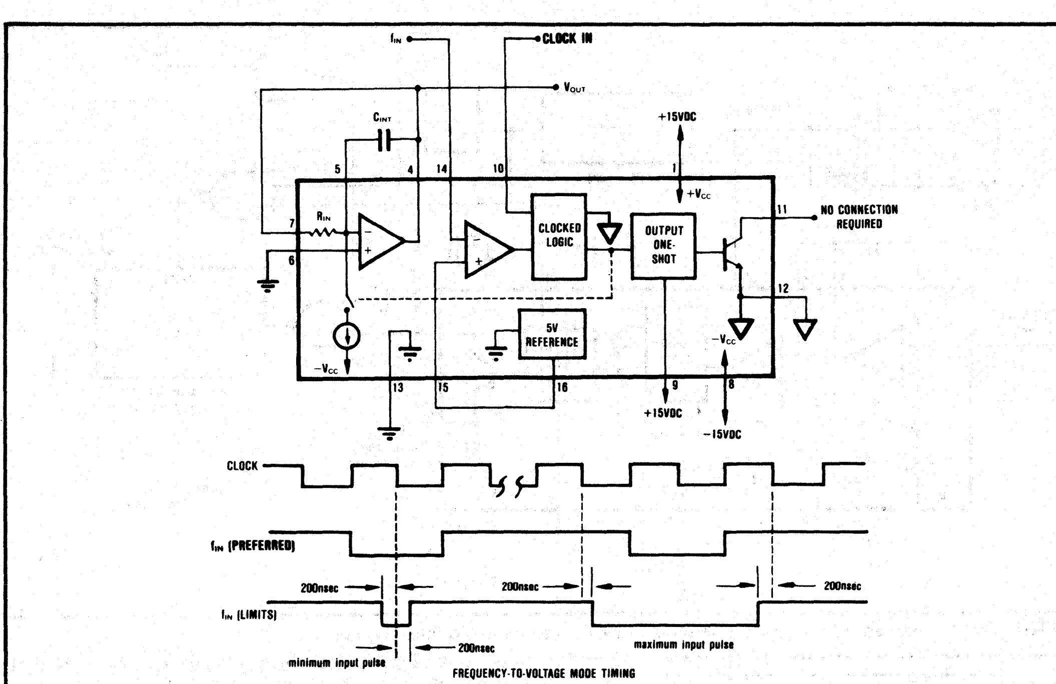


FIGURE 16. Circuit and Timing Diagram of a Frequency-to-Voltage Converter.

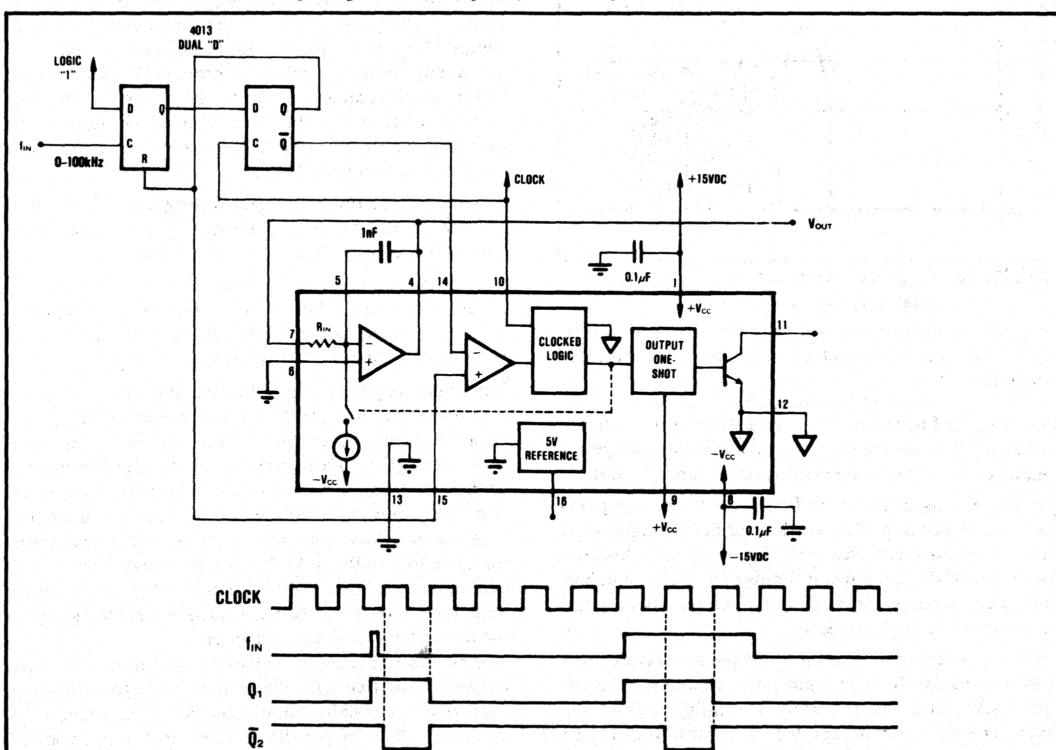


FIGURE 17. Digital Timing Input Conditioning Circuit for Frequency-to-Voltage Operation.

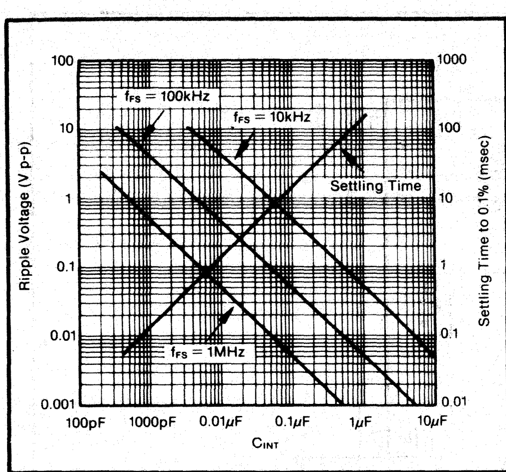


FIGURE 18. Frequency-to-Voltage Mode Output Ripple and Settling Time vs Integrator Capacitance.

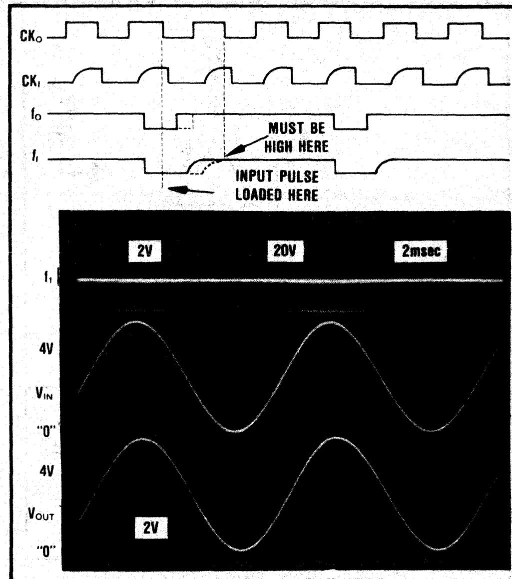


FIGURE 19. Timing Diagram and Oscilloscope Photo of Isolated Voltage-to-Frequency/ Frequency-to-Voltage System.

clock frequency causes the two devices to have complementary transfer functions, which minimizes errors.

Optical coupling is facilitated by use of the output one-shot feature. The output pulse is shortened (see Shortened Output Pulses) to allow for the relatively slow turn-off time of the LED. The timing diagram in Figure 19 shows how the accumulated delay of both optical couplers could produce too long an input pulse for the frequency-to-voltage converter, VFC_2 of Figure 20.

An output filter is used to reduce the ripple in the output of VFC_2. In order to most effectively filter the output, both input and output VFCs are offset. By connecting R_1 to V_{REF}, an accurate offset is created in the voltage-to-frequency function. Zero volts input now creates a 10kHz output. This offset is subtracted in the frequency-to-voltage conversion on the output side, by V_{REF} and R_5.

MORE PULSE POSITION RESOLUTION

Since output pulses must always align with clock edges, the instantaneous output frequency is quantized and appears to have phase jitter. This effect can be greatly reduced by using a high speed clock so that available clock edges come more frequently. This would also create a high full-scale frequency, but the technique shown in Figure 21 offers an alternative. A high speed clock is used to produce high resolution of the output pulse position, but a low full-scale frequency can be programmed.

When an output pulse is generated, the next rising edge of the high frequency clock is delayed for a programmable number of clock counts. Since the integrator reset period (which sets the full-scale range) is determined by the time from rising edge to rising edge at the VFC's clock input once the comparator is tripped, the effective clock frequency is $f_{CLOCK}/16$. The circuit shown can be programmed for any N from 2 to 16. Since an output pulse must propagate through the VFC before the next rising edge of the clock arrives, maximum clock frequency is limited by the delay time shown in the timing diagram.

With output pulses now able to align with greater resolution, the output has lower phase jitter. Using this technique, the output is suitable for ratiometric (period measurement) type counting. This counting technique achieves the maximum possible resolution for short gate periods (see Burr-Brown Application Note AN-130).

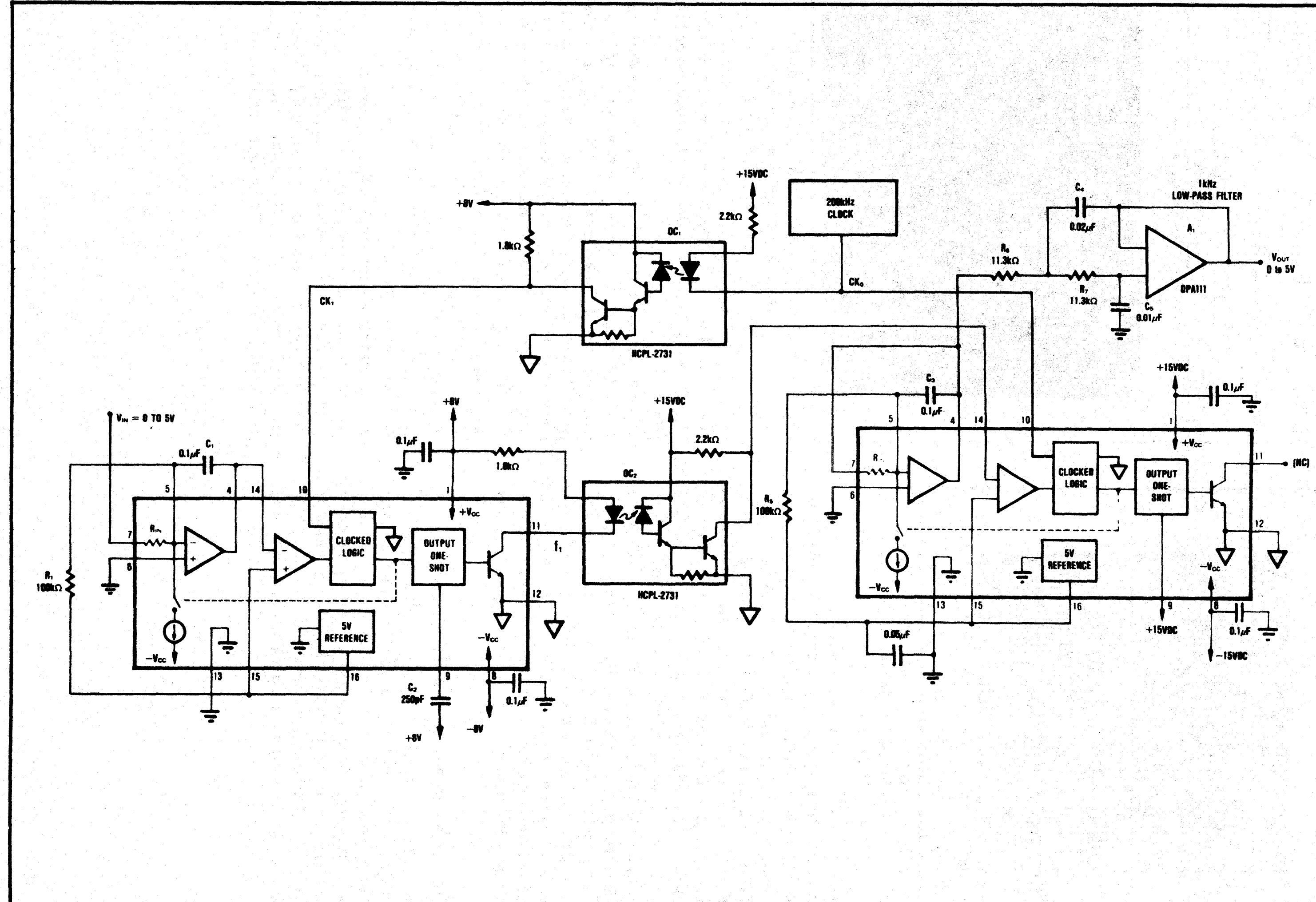


FIGURE 20. Circuit Diagram of Isolated Voltage-to-Frequency/Frequency-to-Voltage System.

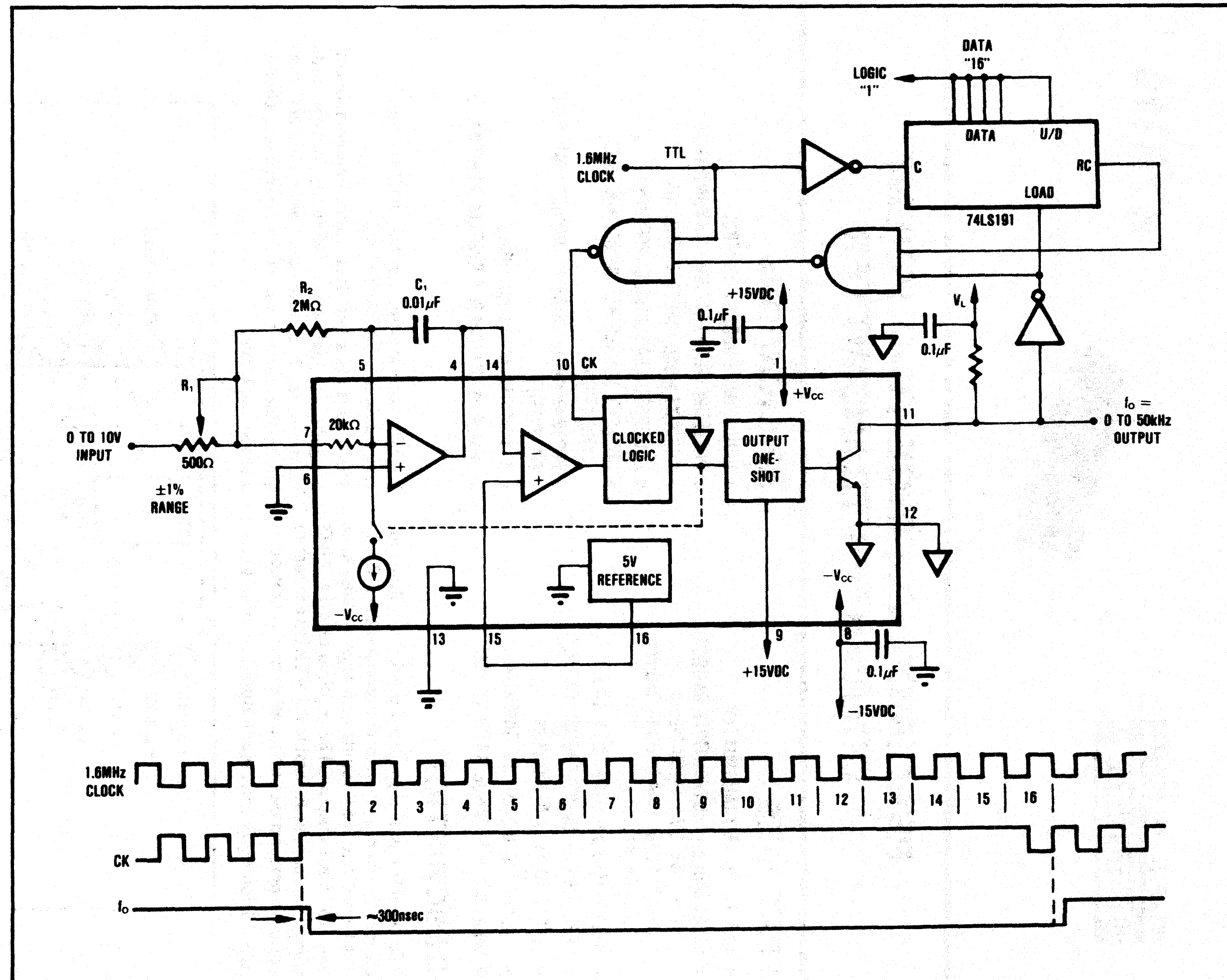
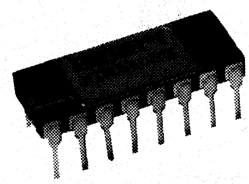


FIGURE 21. Circuit Diagram for Increased Pulse Position Resolution.

BURR-BROWN®

XTR110



PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER

FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:
  0V to +5V, 0V to +10V Inputs
  0mA to 20mA, 5mA to 25mA Outputs
  Other Ranges
- 0.005% MAX NONLINEARITY, 14 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE SUPPLY OPERATION
- CURRENT SOURCING TO COMMON
- WIDE SUPPLY RANGE, 13.5V TO 40V

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDED TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

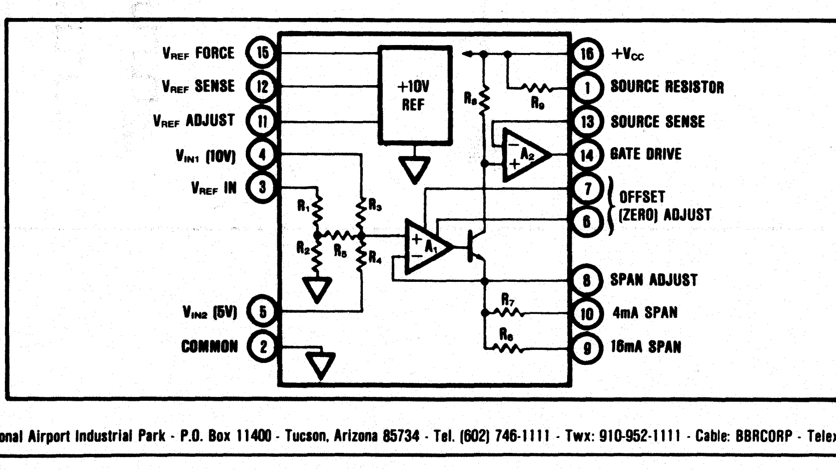
DESCRIPTION

The XTR110 is a monolithic precision voltage-to-current converter. It can convert standard 0V to +10V or 0V to +5V inputs into 4mA to 20mA, or 5mA to 25mA outputs. The required external MOS transistor keeps heat outside the XTR110 package to optimize performance under all output conditions.

A precision +10V reference output can drive 10mA.

An external transistor can be added for more current, e.g. 33mA for 300Ω bridges.

The XTR110 is a key data acquisition component, designed for high noise immunity current-mode transmission. It is also ideal as a precision programmable current source for transducer circuits and test equipment.



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SPECIFICATIONS

ELECTRICAL

At $T_A = +25°C$ and $V_{CC} = +24V$ and $R_L = 250\Omega$† unless otherwise specified. Test circuit: see Figure 1.

PARAMETER	CONDITIONS	XTR110AG MIN	XTR110AG TYP	XTR110AG MAX	XTR110BG MIN	XTR110BG TYP	XTR110BG MAX	UNITS
TRANSMITTER								
Transfer Function			$I_O = 10\,[(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}$					
Input Range: V_{IN1}	Specified performance	0		+10	*		*	V
V_{IN2}	Specified performance	0		+5	*		*	V
Current, I_O	Specified performance[1]	4		20	*		*	mA
	Derated performance[1]	0		40	*		*	mA
Nonlinearity	16mA/20mA span[2]		0.01	0.025		0.002	0.005	% of span
Offset Current, I_{OS}	$I_O = 4mA$[1]							
Initial	[1]			0.4			0.1	% of span
vs Temp	[1]			0.005			0.003	% of span/°C
vs Supply, V_{CC}	[1]			0.005			*	% of span/V
Span Error	$I_O = 20mA$							
Initial	[1]			0.6			0.2	% of span
vs Temp	[1]			0.005			0.003	% of span/°C
vs Supply, V_{CC}	[1]			0.005			*	% of span/V
Output Resistance	From drain of FET (Q_{EXT})[3]		10×10^9			*		Ω
Input Resistance	V_{IN1}		27			*		kΩ
	V_{IN2}		22			*		kΩ
	V_{REF} IN		19			*		kΩ
Dynamic Response								
Settling Time	To 0.1% of span		15			*		μsec
	To 0.01% of span		20			*		μsec
Slew Rate			1.3			*		mA/μsec
VOLTAGE REFERENCE								
Output Voltage		+9.95	+10	+10.05	+9.98	*	+10.02	V
vs Temp				50			30	ppm/°C
vs Supply, V_{CC}	Line regulation			0.005			*	%/V
vs Output Current	Load regulation			0.01			*	%/mA
vs Time			100			*		ppm/1k hrs
Trim Range	[4]	−0.100		+0.25	*		*	V
Output Current[5]	Specified performance	10			*			mA
POWER SUPPLY								
Input Voltage, V_{CC}		+13.5		+40	*		*	V
Quiescent Current	Excluding I_O		3	4.5		*	*	mA
TEMPERATURE RANGE								
Specification		−40		+85	*		*	°C
Operating		−55		+125	*		*	°C
Storage		−55		+125	*		*	°C

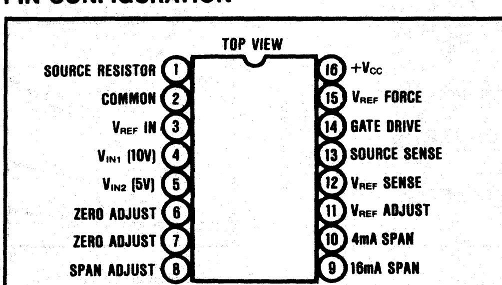
*Specification same as grade to the immediate left. †Specifications apply to the range of R_L shown in Typical Performance Curves.

NOTES: (1) Including internal reference. (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by $(+V_{CC} - 2V) + V_{DS}$ required for linear operation of the FET. (4) For V_{REF} adjustment circuit see Figure 4. (5) For extended I_{REF} drive circuit see Figure 8.

ABSOLUTE MAXIMUM RATINGS

Power Supply, $+V_{CC}$ 40V
Input Voltage, V_{IN1}, V_{IN2}, V_{REF} IN .... $+V_{CC}$
Storage Temperature Range .... −55°C to +125°C
Lead Temperature (soldering, 10sec) .... 300°C
Output Short Circuit Duration, Gate Drive
and V_{REF} Force .... Continuous to common and $+V_{CC}$
Output Current Using Internal 50Ω Resistor 40mA

PIN CONFIGURATION



ORDERING INFORMATION

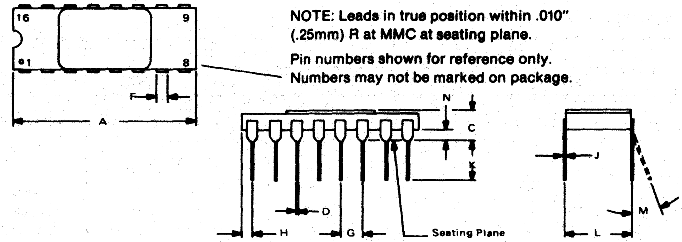
XTR110 X G

Basic model number

Performance grade code
A, B: −40°C to +85°C

Package code
G: 16-pin hermetic DIP

MECHANICAL

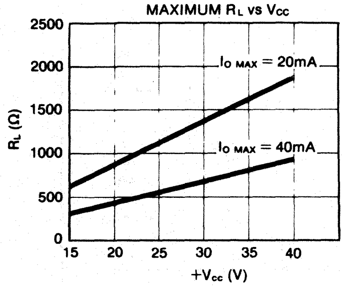


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

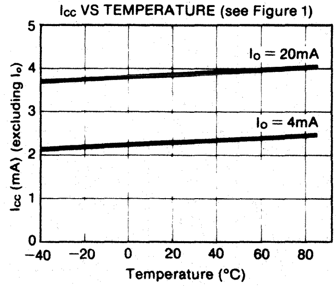
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = 24VDC$, $R_L = 250\Omega$ unless otherwise noted.

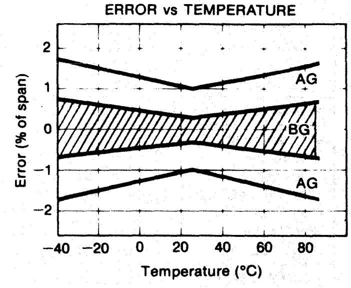
MAXIMUM R_L vs V_{CC}



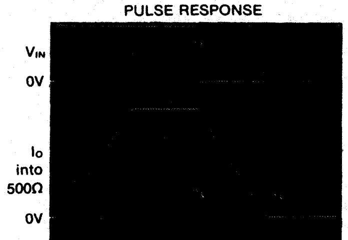
I_{CC} VS TEMPERATURE (see Figure 1)



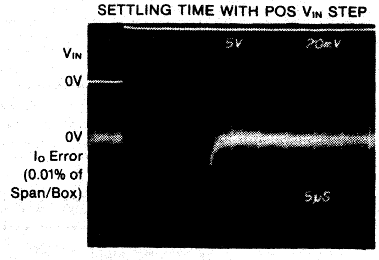
TOTAL OUTPUT ERROR vs TEMPERATURE



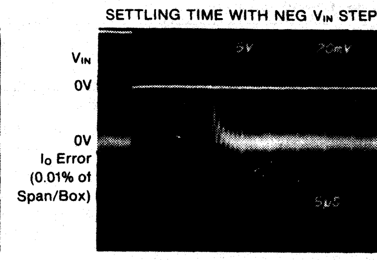
PULSE RESPONSE



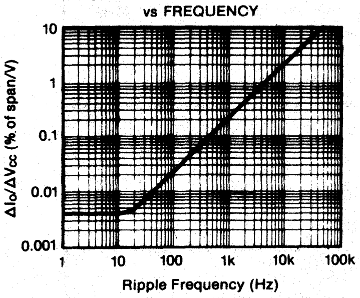
SETTLING TIME WITH POS V_{IN} STEP



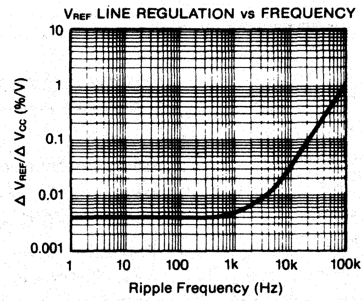
SETTLING TIME WITH NEG V_{IN} STEP



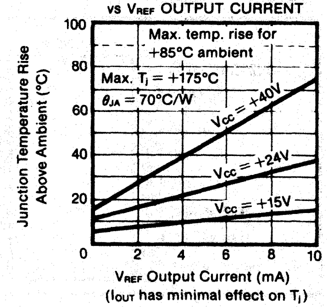
I_O POWER SUPPLY REJECTION vs FREQUENCY



V_{REF} LINE REGULATION vs FREQUENCY



JUNCTION TEMPERATURE RISE vs V_{REF} OUTPUT CURRENT



THEORY OF OPERATION

The XTR110 is designed to convert a high level input voltage into a positive output current.

A block diagram of the XTR110 is shown in Figure 1. The circuit contains four main functional blocks: (1) a precision resistor divider network (R_1–R_5), (2) a voltage-to-current converter (A_1, Q_1, R_6, R_7), (3) a current-to-current converter (A_2, R_8, R_9, Q_{EXT}), and (4) a precision +10V reference.

The precision divider network sums three input voltages to the noninverting input of A_1. These are V_{IN1} (10V full scale), V_{IN2} (5V full scale), and V_{REF} IN (for offsetting).

In the voltage-to-current converter, the op amp, A_1, forces its input voltage across the span setting resistors, R_6 and R_7. Since Q_1 is a high gain Darlington, base current error is negligible and all current flows to the current-to-current converter (into R_8). The transfer function including input divider is as follows:

$$I_{R8} = [(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}$$

where R_{SPAN} is the resistance from Q_1 emitter to common.

The current-to-current converter is the output section of the XTR110 transmitter. The voltage across the 500Ω resistor (R_8) is forced across the 50Ω resistor (R_9) by A_2 and the external MOSFET (Q_{EXT}). Since no current flows in the gate of the MOSFET, all current is delivered to the output. This current (I_{OUT}) is ten times the internal current through R_8. Use of the external transistor keeps power out of the precision IC to maintain accuracy.

The overall transfer function for the XTR110 transmitter is:

$$I_O = 10[(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}.$$

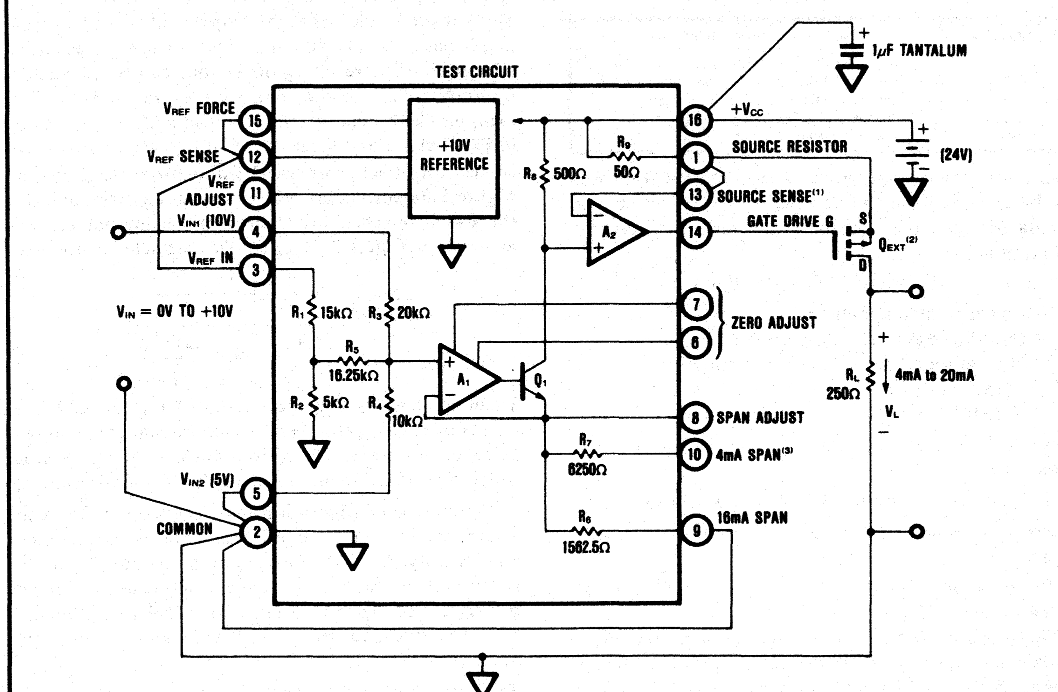
For output currents beyond 40mA an external resistor can be used in place of R_9.

The +10V reference provides input offsetting, e.g. 4mA offset for the 4ma to 20mA output configuration. The reference can deliver 10mA and is protected from shorts to common. Higher current can be provided for other applications by using an external NPN transistor connected to the sense and force pins.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection of the XTR110 is the standard 0V to +10V input; 4mA to 20mA output configuration is shown in Figure 1.



NOTES: (1) To maintain accuracy, make a separate direct connection between pins 1 and 13. (2) Q_{EXT} is any P-channel enhancement-mode power MOSFET with appropriate voltage and power rating. PNP bipolar transistors can be used with slight degradation in end-point accuracy and linearity. For recommended devices see section on external transistor. (3) For 20mA span, strap 4mA and 16mA pins together to common.

FIGURE 1. Block Diagram of the XTR110 in Basic Connection: 0V to +10V in, 4mA to 20mA out.

$+V_{CC}$ may originate at the XTR110 site or may be brought in as part of a three-wire twisted line. Be sure to use sufficient bypassing close to the XTR110 on the $+V_{CC}$ line.

EXTERNAL TRANSISTOR

Connections to the MOSFET are gate drive (pin 14) and source resistor (pin 1). To eliminate errors due to resistance in the connection between pin 1 and the source of the external transistor, connect pin 13 directly to pin 1 as shown in Figure 1.

The output of A2, pin 14, is intended to drive a MOSFET or PNP external pass transistor, and for that reason, is atypical of op amp outputs. The output stage can be visualized as a 300μA current source in parallel with an NPN collector. The NPN is the active element that, through feedback, determines where the gate drive should be set. It is capable of sinking over 15mA.

External MOSFET

The XTR110 can operate with a variety of output transistors having appropriate breakdown voltage and power rating which is influenced by package type. Some general observations on package thermal characteristics are listed in Table I.

TABLE I. External Transistor Package Type and Dissipation.

Package Type	Allowable Power Dissipation
TO-92	Lowest: Use minimum supply and at +25°C.
TO-237	Acceptable: Trade-off supply and temperature.
TO-39	Good: Adequate for majority of designs.
TO-220	Excellent: For prolonged maximum stress.
TO-3	Overkill: If nothing else is available.

Maximum power dissipation of the external transistor can be derived from the derating curve. It can also be calculated from the thermal characteristics using the equation below:

$$P_A = P_D - (T_A - 25)/\theta_{JA}$$

P_A = Power to be dissipated at T_A

T_A = Maximum ambient temperature

P_D = Maximum continuous power dissipation at +25°C ($I_D V_{DS}$)

θ_{JA} = Junction to ambient thermal resistance

(Refer to the manufacturer's data sheet for required numbers.)

Table II shows suitable MOSFET output transistors.

Summary of points to consider for selecting the transistor are:

1. Power rating—Equal to $1.5 \times P_A$ if possible, or at least equal to P_A.
2. Drain-source breakdown—Greater than maximum expected V_{DS}. This includes any additional voltage that may exist between the transmitter and receiver grounds.
3. Gate-source breakdown—Greater than $+V_{CC}$, because V_{CC} will be applied gate-to-source, under the condition of an open drain line (V_{GATE} then = 0V). Most MOSFETS will tolerate only 20V, but a zener (12V or more) connected gate-to-source will clamp the junction and remain off during normal operation.

TABLE II. Available P-Channel MOSFETs.

Manufacturer	Part No.	BV_{DSS}*	BV_{GS}*	Package
Ferranti	ZVP1304A	−40V	20V	TO-92
	ZVP1304B	−40V	20V	TO-39
	ZVP1306A	−60V	20V	TO-92
	ZVP1306B	−60V	20V	TO-39
International Rectifier	IRF9513	−60V	20V	TO-220
Motorola	MTP8P08	−80V	20V	TO-220
RCA	RFL1P08	−80V	20V	TO-39
	RFT2P08	−80V	20V	TO-220
Siliconix (preferred)	VP0300B	−30V	40V	TO-39
	VP0300L	−30V	40V	TO-92
	VP0300M	−30V	40V	TO-237
	VP0808B	−80V	40V	TO-39
	VP0808L	−80V	40V	TO-92
	VP0808M	−80V	40V	TO-237
Supertex	VP1304N2	−40V	20V	TO-220
	VP1304N3	−40V	20V	TO-92
	VP1306N2	−60V	20V	TO-220
	VP1306N3	−60V	20V	TO-92

*BV_{DSS}—Drain-source breakdown voltage. BV_{GS}—Gate-source breakdown voltage.

External PNP Transistor

A PNP bipolar transistor can also be used for the output, but will result in a slight drop in end-point accuracy and linearity. A TN2905 in a TO-237 package performs adequately. The resulting offset shift can be calculated by 4mA/beta, and the span shift by 16mA/beta. For example, with beta = 250 the offset shift will be 16μA (0.1% of span) and span shift 64μA (0.4% of span). To correct for offset error use the potentiometer shown in Figure 5. To correct for span error, use an external resistor, R_{PAD}, connected in parallel with the internal resistor, as shown in Figure 2. R_{PAD} can be calculated as follows:

$$R_{PAD} = \frac{1}{\frac{1}{50} - \frac{1}{50 \times \frac{\Delta Span}{Span}}}$$

Small nonlinearity degradation (0.01% typical at $24V_{CC}$) results from changes in beta caused by changes in power as collector current varies from 4mA to 20mA. A heat sink can be added to minimize the heat dissipation effect.

A Darlington configuration (two separate PNPs) can also be used with no degradation in end-point accuracy and linearity. A 0.047μF capacitor across pins 13 and 14 is required for stability as shown in Figure 3. Single-packaged Darlingtons with internal bleeder resistors are not recommended since they will severely degrade accuracy.

To select a bipolar transistor, follow the same points as for MOSFETs. Note, however, the base-emitter breakdown is not considered because this junction is forward biased should the collector open.

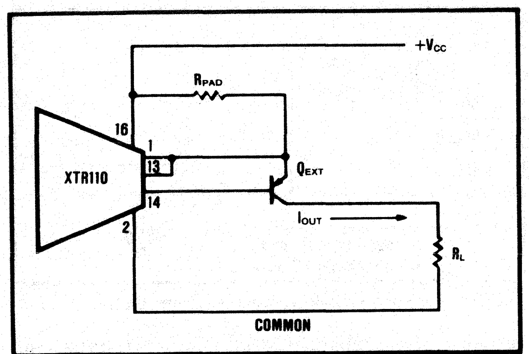


FIGURE 2. PNP Output Transistor (R_{PAD} corrects for span error caused by beta).

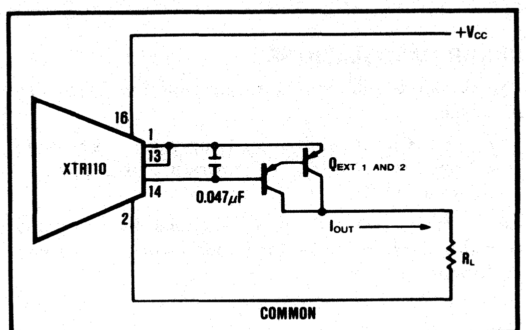


FIGURE 3. Darlington Output Composed of Two PNP Transistors.

COMMONS

Careful attention should be directed toward proper connection of the commons. All commons should be joined at one point as close to pin 2 of the XTR110 as possible. The exception is the I_{OUT} return. It can be returned to any place where it will not modulate the common at pin 2.

VOLTAGE REFERENCE

The reference voltage is accurately regulated at pin 12 (V_{REF} sense). To preserve accuracy, any load including pin 3 should be connected to this point.

The circuit in Figure 4 shows coarse and fine adjustment of the voltage reference.

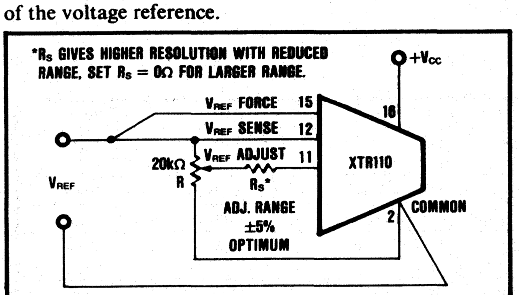


FIGURE 4. Optional Adjustment of Reference Voltage.

OFFSET (ZERO) ADJUSTMENT

The offset current can be adjusted by using the potentiometer, R_1, shown in Figure 5. The procedure is to set the input voltage to zero and then adjust R_1 to give 4mA at the output. For spans starting at 0mA, the following special procedure is recommended: set the input to a small nonzero value and then adjust R_1 to the proper output current. When the input is zero the output will be zero. Figures 6 and 7 show graphically how offset is adjusted.

SPAN ADJUSTMENT

The span is adjusted at the full-scale output current using the potentiometer, R_2, shown in Figure 5. This adjustment is interactive with the offset adjustment, and a few iterations may be necessary. For the circuit shown, set the input voltage to +10V full scale and then adjust R_2 to give 20mA full-scale output. Figures 6 and 7 show graphically how span is adjusted.

The values of R_2, R_3, and R_4 for adjusting the span are determined as follows: choose R_4 in series to slightly decrease the span; then choose R_2 and R_3 to increase the span to be adjustable about the center value.

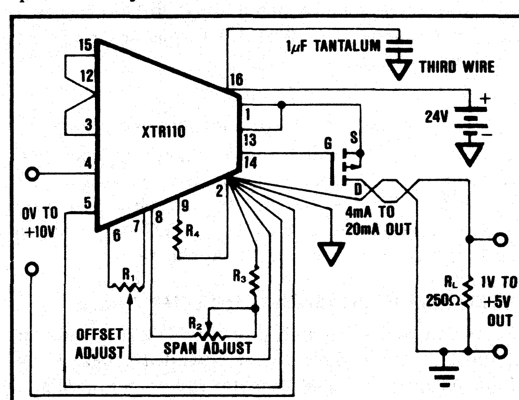


FIGURE 5. Offset and Span Adjustment Circuit for 0V to +10V Input, 4mA to 20mA Output.

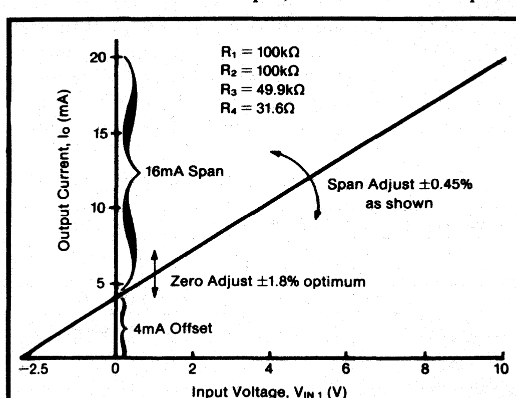


FIGURE 6. Zero and Span of 0V to +10V Input, 4mA to 20mA Output Configuration (see Figure 5).

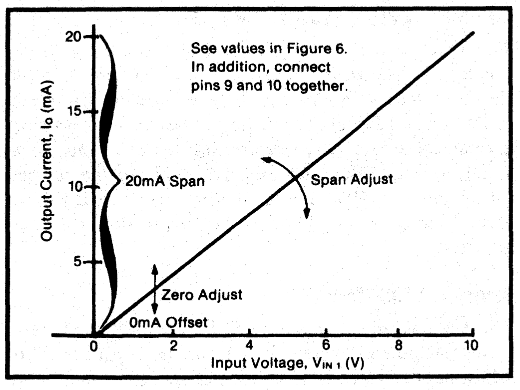


FIGURE 7. Zero and Span of 0V to $+10V_{IN}$, 0mA to 20mA Output Configuration (see Figure 5).

STANDARD CURRENT RANGES OR SPANS

Table III shows the pin connections for standard XTR110 current ranges.

EXTENDED SPAN

For spans beyond 40mA, the internal 50Ω resistor (R_9) may be replaced by an external resistor connected between pins 13 and 16.

Its value can be calculated as follows:

$$R_{EXT} = R_9\ (Span_{OLD}/Span_{NEW})$$

Since the internal thin-film resistors have a 20% absolute value tolerance, measure R_9 before determining the final value of R_{EXT}. Self-heating of R_{EXT} can cause nonlinearity. Therefore, choose one with a low TC and adequate power rating. See Figure 12 for application.

EXTENDED REFERENCE CURRENT DRIVE

The current drive capability of the XTR110's internal reference is 10mA. This can be extended if desired by adding an external NPN transistor shown in Figure 8.

LOW TEMPERATURE COEFFICIENT (TC) OPERATION

Although the precision resistors in the XTR110 track within 1ppm/°C, the output current depends upon the absolute temperature coefficient of any one of the resistors, R_6, R_7, R_8, and R_9. Since the absolute TC of the resistors is 20ppm/°C, maximum, the TC of the output current can have 20ppm/°C drift. For low TC operation, zero TC resistors can be substituted for either the span resistors (R_6 or R_7) or for the source resistor (R_9) but not both.

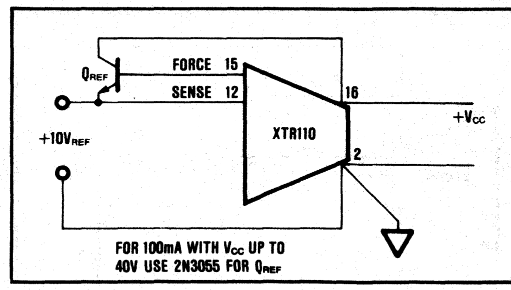


FIGURE 8. Extended Reference Current Drive.

ERROR CALCULATIONS

Errors can be calculated by considering these key parameters:

1. Offset Current (Initial, vs Temperature, vs Supply)
2. Span Error (Initial, vs Temperature, vs Supply)
3. Nonlinearity

Lower errors can readily be obtained by externally adjusting the initial offset and span errors to zero (see Performance Curves).

TYPICAL APPLICATIONS

The XTR110 is ideal for a variety of applications requiring high noise immunity current-mode signal transmission. The precision +10V reference is convenient and can be exciting for bridges and transducers. Selectable ranges make it very useful as a precision programmable current source. The compact design and low price of the XTR110 allow versatility with a minimum of external components and design engineering expense.

Figures 9 through 13 show typical applications of the XTR110.

TABLE III. Pin Connections for Standard Ranges.

Input Range (V)	Output Range (mA)	Pin 3	Pin 4	Pin 5	Pin 9	Pin 10
0 - 10 2 - 10	0 - 20 4 - 20	Com	Input	Com	Com	Com
0 - 10	4 - 20	+10V Ref	Input	Com	Com	Open
0 - 10	5 - 25	+10V Ref	Input	Com	Com	Com
0 - 5 1 - 5	0 - 20 4 - 20	Com	Com	Input	Com	Com
0 - 5	4 - 20	+10V Ref	Com	Input	Com	Open
0 - 5	5 - 25	+10V Ref	Com	Input	Com	Com

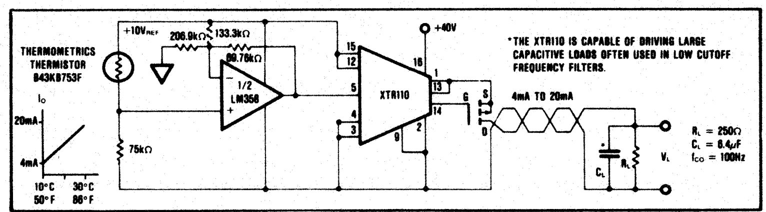


FIGURE 9. 4mA to 20mA Single-Supply Thermistor Transmitter for Energy Management Systems.

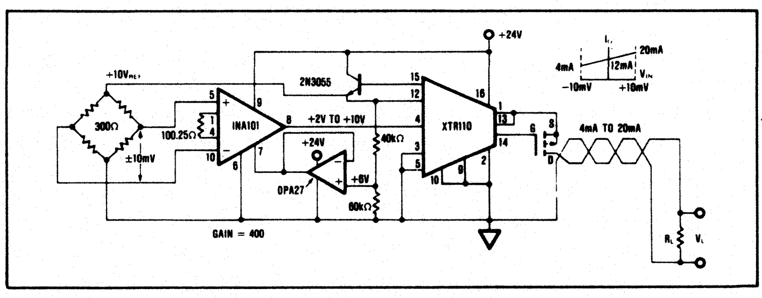


FIGURE 10. 4mA to 20mA Single-Supply Bridge Transmitter.

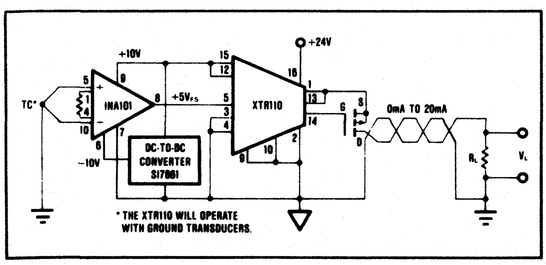


FIGURE 11. 0mA to 20mA Single-Supply Thermocouple Transmitter.

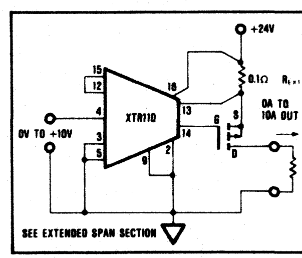


FIGURE 12. 0A to 10A High Current Voltage-to-Current Converter.

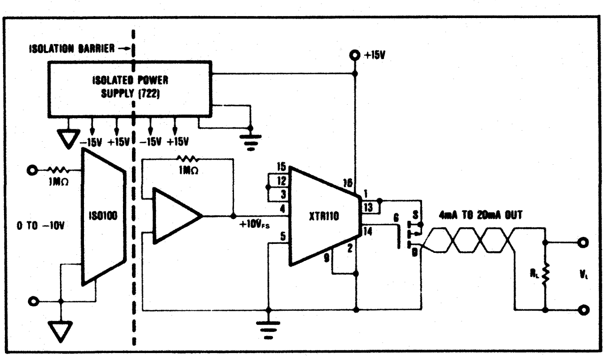


FIGURE 13. Isolated 4mA to 20mA Channel

HIGH PERFORMANCE DICE BACKED BY BURR-BROWN'S TRADITION OF QUALITY

Many of Burr-Brown's high-performance monolithic products are available in die form.

All Burr-Brown dice products are the same as those used in our high quality, high performance monolithic and hybrid devices and are proven in demanding applications throughout the world. The dice are manufactured and tested at our Tucson Microtechnology facility using the most advanced equipment and methods available, assuring total control of quality and reliability for every product.

The state-of-the-art performance achieved by these precision monolithic products reflects Burr-Brown's unmatched technical capabilities in:

> Low-noise processing / High-stability nichrome thin-film resistors / Active laser trimming / Dielectric isolation / Patented circuit design

At Burr-Brown, concern for quality is a fundamental part of wafer processing. Dice are 100% visually inspected according to MIL-STD-883, Method 2010 Condition B. All wafers are 100% probe tested to specified electrical test limits.

The data sheets and process descriptions provide detailed information on these quality dice.

INTEGRATED CIRCUIT DICE

QUALITY

Visual Inspection: All dice and wafers are 100% visually inspected to MIL-STD-883, Method 2010, Condition B. Dice receive an additional in-process Quality Control inspection to 0.65% AQL.

Probe Tests: All wafers are 100% electrically probe tested to the electrical probe test limits specified in the die data sheet. Due to possible parametric shifts during die separation and assembly, these specifications are not guaranteed after assembly.

Unprobed Parameters: Parameters not specified on the device data sheet are not probed or guaranteed. The dice performance will typically be equivalent to its corresponding part numbered packaged device.

PACKAGING

Package: Dice are packaged face-up in individually compartmented anti-static plastic carriers (waffle packs) and are oriented for automated assembly. Carriers are heat sealed in plastic bags with a dry atmosphere.

Marking: Each die carrier is marked with:

1. Burr-Brown part number
2. Lot number
3. Wafer number
4. QA seal and date
5. Quantity
6. QC identification number

If required, customer part number and order number can be marked on each package.

Storage: High humidity and corrosive atmospheres can cause oxidation or corrosion of the aluminum metalization on wire bond pads. Dice should be stored in a clean dry environment and should be protected from static damage. Storage in a dust-free cabinet with a dry nitrogen atmosphere is recommended.

DIE HANDLING PRECAUTIONS

Static Damage: All integrated circuits can suffer damage from electrostatic discharge. Even precision bipolar devices can suffer subtle parametric damage (increased offset voltage, drift, noise, etc.) if precautions are not adequate. Anti-static work stations are recommended when handling or assembling precision semiconductor devices.

Atmosphere: Die carriers should be opened only in a dust-free environment with a dry non-corrosive atmosphere.

Handling: Although each die is protected by a thick (8000Å minimum) glassivation layer, care should be taken to keep from scratching the surface of the die. Carriers must not be opened for inspection by unqualified personnel. Anti-static protection is recommended when handling or assembling dice.

HYBRID CIRCUIT ASSEMBLY RECOMMENDATIONS

Die Attach: Die attach with silver conductive epoxy or polyimide is recommended to minimize assembly shifts and preserve the accuracy and precision inherent in the die.

Burr-Brown dice are gold-backed and can be eutectically die-attached using a 98/2 gold/silicon preform and a die/substrate temperature of 400°C to 430°C. Exposure time to die attach temperatures should be minimized as permanent parametric shifts can occur.

Assembly in hermetic packages under adequate moisture control is recommended in order to preserve parametric performance and stability.

Wire Bond: Wire bonding may be done with 1.25 mil 99.99% pure gold wire using thermo-sonic techniques or by ultrasonic bonders using 1.25 mil 99/1 aluminum/silicon wire. Wire bond pad size is 4 × 4 mils minimum and aluminum metalization thickness is 8000Å minimum.

ORDERING INFORMATION

Part Number: **OPA27 C D**

Basic device part number — OPA27
Grade/Temperature Range — C
(see data sheet for proper suffix)
Designation: Dice — D

Minimum Order: Dice are subject to minimum order quantities. Consult your local sales office for details on minimum order size and for pricing.

Returns: Returns must be authorized by Burr-Brown. If dice fail visual inspection according to MIL-STD-883, Method 2010, Condition B and 0.65% AQL the entire lot must be returned in their original carriers along with detailed documentation showing reason for rejection.

WAFER PROCESSING

Process Wafer

Gold Back Wafer

100% Wafer Visual Inspection

Sample Parametric Test

100% Probe Test/Laser Trim to
Data Sheet Electrical Limits

Saw Wafer

Deionized Water Rinse

Die Separation

Die Sort

100% Visual Inspection
MIL-STD-883, Method 2010, Condition B

Load In Carrier

In-Process QC Visual Inspection
MIL-STD-883, Method 2010, Condition B
(0.65 AQL)

In-Process QC Documentation Inspection

Seal In Carrier

Ship

BURR-BROWN®

DAC811 DIE

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER DIE

DESCRIPTION

The DAC811 is a complete single-chip integrated circuit microcomputer-compatible 12-bit digital-to-analog converter. The chip includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

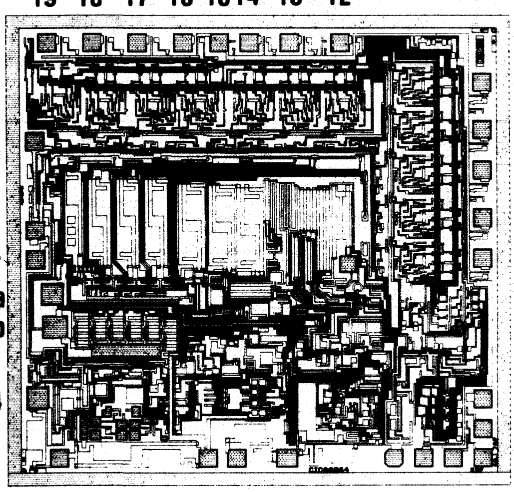
Microcomputer interfacing is facilitated by a double-buffered latch. The input latch is divided into three 4-bit nybbles to permit interfacing to 4-, 8-, 12- or 16-bit buses and to handle right- or left-justified data. The 12-bit data in the input latches is transferred to the D/A latch to hold the output value.

Input gating logic is designed so that loading the last nybble or byte of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from adjacent input latches to the D/A latch. This feature avoids spurious analog output values while using an interface technique that saves computer instructions.

DIE TOPOGRAPHY

19 18 17 16 15 14 13 12

20 21 22 23a 23b 24



11 10 9 8 7 6 5

25 26 27 28 1 2 3 4

Die Size: 134 × 128 mils
Bonding Pad Size: 4 × 4 mils
Backside Contact: Gold

Pad	Name	Function
1	V_{DD}	Logic Supply, +5V.
2	$\overline{WR}$	WRITE, command signal to load latches. Logic low loads latches.
3	$\overline{LDAC}$	LOAD D/A CONVERTER, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	NYBBLE A, enables $\overline{WR}$ to load input latch A (the most significant nybble). Logic low enables.
5	$\overline{N_B}$	NYBBLE B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	NYBBLE C, enables $\overline{WR}$ to load input latch C (the least significant nybble). Logic low enables.
7	D_{11}	DATA, Bit 12, MSB, positive true.
8	D_{10}	DATA, Bit 11.
9	D_9	DATA, Bit 10.
10	D_8	DATA, Bit 9.
11	D_7	DATA, Bit 8.
12	D_6	DATA, Bit 7.
13	D_5	DATA, Bit 6.
14	D_4	DATA, Bit 5.
15	DCOM	DIGITAL COMMON, V_{DD} supply return.
16	D_0	DATA, Bit 1, LSB.
17	D_1	DATA, Bit 2.
18	D_2	DATA, Bit 3.
19	D_3	DATA, Bit 4.
20	$+V_{CC}$	Analog Supply Input, +15V or +12V.
21	$-V_{CC}$	Analog Supply Input, −15V or −12V.
22	GAIN ADJ	To externally adjust gain.
23a, 23b	ACOM	ANALOG COMMON, $\pm V_{CC}$ supply return (connect together).
24	V_{OUT}	D/A converter voltage output.
25	10V RANGE	Connect to pin 24 for 10V Range.
26	SJ	SUMMING JUNCTION of output amplifier.
27	BPO	BIPOLAR OFFSET. Connect to pin 26 for Bipolar Operation.
28	REF OUT	6.3V reference output.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

$T_A = +25°C$, $\pm V_{CC} = 15V$ unless otherwise noted.

MODEL	DAC811JD			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
DIGITAL INPUT				
Resolution			12	Bits
Codes[2]		USB, BOB		
V_{IH}	+2.0		+15	VDC
V_{IL}	0.0		+0.8	VDC
I_{IH}, $V_I = +2.7V$			+10	μA
I_{IL}, $V_I = +0.4V$			±20	μA
TRANSFER CHARACTERISTICS				
ACCURACY				
Linearity Error		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	±1	LSB
Gain Error[3]		±0.1	±0.2	%
Offset Error[3][4]		±10	±30	mV
OUTPUT				
ANALOG OUTPUT				
Voltage Range ($\pm V_{CC}$ =15V)[6]:				
Unipolar		0 to +10		V
Bipolar		±5, ±10		V
Output Current	±5			mA
Short Circuit to Common Duration		Indefinite		
REFERENCE VOLTAGE				
Voltage	+6.2	+6.3	+6.4	V
Source Current Available for External Loads	+2.0			mA
Short Circuit to Common Duration		Indefinite		
POWER SUPPLY REQUIREMENTS				
Voltage: $+V_{CC}$	+11.4	+15	+16.5	VDC
$-V_{CC}$	−11.4	−15	−16.5	VDC
V_{DD}	+4.5	+5	+5.5	VDC
Current (no load):				
$+V_{CC}$		+16	+25	mA
$-V_{CC}$		−23	−35	mA
V_{DD}		+8	+15	mA
Potential at DCOM with Respect to ACOM[7]			±0.5	V
Power Dissipation		625	800	mW
TEMPERATURE RANGE				
Specification:	0		+70	°C

NOTES: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (3) Adjustable to zero with external trim potentiometer. (4) Error at input code 000_{16} for both unipolar and bipolar ranges. (5) FSR means Full Scale Range and is 20V for the ±10V range. (6) Minimum supply voltage required for ±10V output swing is ±13.5V. Output swing for ±11.4V supplies is at least −8V to +8V. (7) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$	0 to +18V
$-V_{CC}$ to ACOM	0 to −18V
V_{DD} to DCOM	0 to +7V
V_{DD} to ACOM	±7V
ACOM to DCOM	±7V
Digital Inputs to DCOM	−0.4V to +18V
External Voltage Applied to 10V Range Resistor	±12V
REF OUT	Indefinite short to ACOM
External Voltage Applied to DAC Output	−5V to +5V
Storage Temperature	−65°C to +150°C
Junction Temperature	+175°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGING

DAC811 dice are visually inspected to MIL-STD-883, method 2010, Test Condition B and are shipped in sealed carriers.

ORDERING INFORMATION

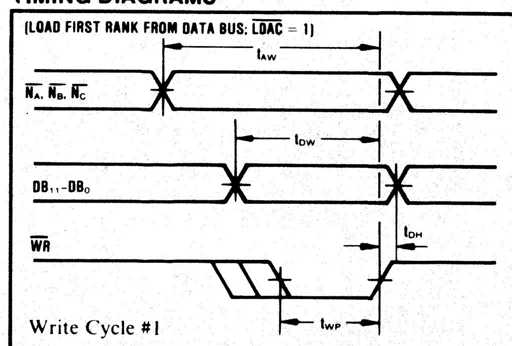
DAC811 J D

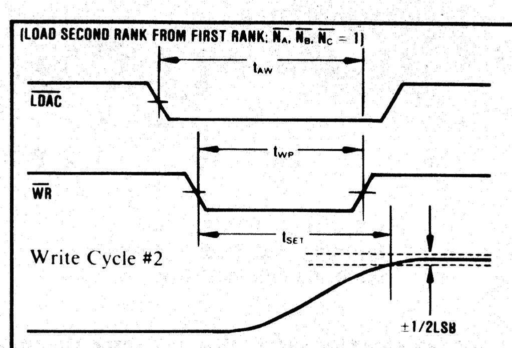
Basic model number

Grade/temperature range
J = 0°C to 70°C

Package code
D = die

TIMING DIAGRAMS





TIMING SPECIFICATIONS

Digital Interface Timing

T_{WP}, $\overline{WR}$ pulse width (min) 50ns
$T_{AW}1$, $\overline{N_X}$ and $\overline{LDAC}$ valid to end of $\overline{WR}$ (min) 50ns
T_{DW}, data valid to end of $\overline{WR}$ (min) 80ns
T_{DM}, data valid hold time (min) 0ns

OPERATION

DAC811 is a complete single IC chip12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 1.

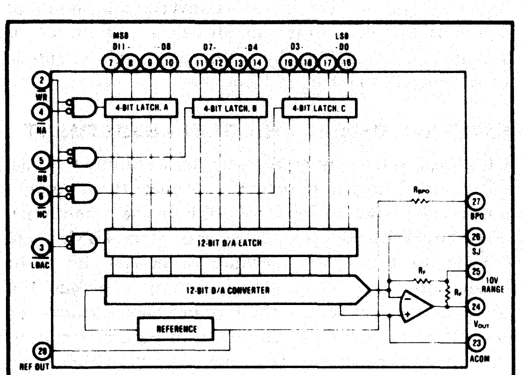


FIGURE 1. DAC811 Block Diagram.

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by N_A, N_B, N_C and WR. N_A, N_B, and N_C are internally NORed with WR so that the input latches transmit data when both N_A (or N_B, N_C) and WR are at logic "0". When either N_A (or N_B, N_C) or WR go to logic "1", the input data is latched into the input registers and held until both N_A (or N_B, N_C) and WR go to logic "0".

The D/A latch is controlled by LDAC and WR. LDAC and WR are internally NORed so that the latches transmit data to the D/A switches when both LDAC and WR are at logic "0". When either LDAC or WR are at logic "1", the data is latched in the D/A latch and held until LDAC and WR go to logic "0".

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for all latches is given in Table I.

GAIN AND OFFSET ADJUSTMENTS

Figures 2 and 3 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

TABLE I. DAC811 Interface Logic Truth Table.

$\overline{WR}$	$\overline{N_A}$	$\overline{N_B}$	$\overline{N_C}$	$\overline{LDAC}$	OPERATION
1	X	X	X	X	No Operation
0	0	1	1	1	Enables Input Latch 4MSB's
0	1	0	1	1	Enables Input Latch 4 Middle Bits
0	1	1	0	1	Enables Input Latch 4 LSB's
0	1	1	1	0	Loads D/A Latch From Input Latches
0	0	0	0	0	All Latches Transparent

"X" = Don't Care

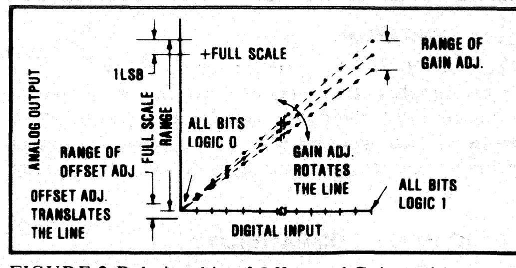


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter

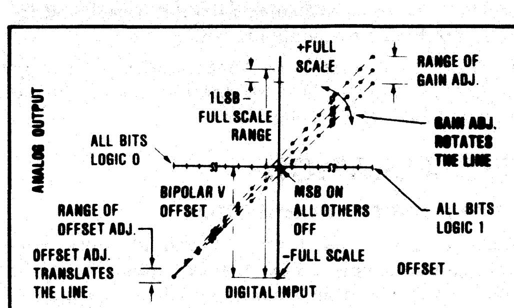


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the Offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table II for corresponding codes.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages.

TABLE II. Digital Input/Analog Output, $\pm V_{CC} = \pm 15V$.

DIGITAL INPUT	ANALOG OUTPUT VOLTAGE		
	0 to +10V	±5V	±10V
12-Bit Resolution MSB LSB ↓ ↓			
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5.0000V	0.0000V	0.0000V
011111111111	+4.9976V	−0.0024V	−0.0049V
000000000000	0.0000V	−5.0000V	−10.0000V
1LSB	2.44mV	2.44mV	4.88mV

±12V OPERATION

The DAC811 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12V supplies, the output swing should be restricted to ±8V in order to meet specifications.

LOGIC INPUT COMPATIBILITY

The DAC811 digital inputs are TTL, LSTTL, and 54/74HC CMOS-compatible over the operating range of V_{DD}. The input switching threshold remains at the TTL threshold over the supply range.

The logic input current over temperature is low enough to permit driving the DAC811 directly from the outputs of 4000B 54/74C CMOS devices.

INSTALLATION

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram, Figure 4. These capacitors (1μF to 10μF tantalum recommended) should be located close to the DAC811.

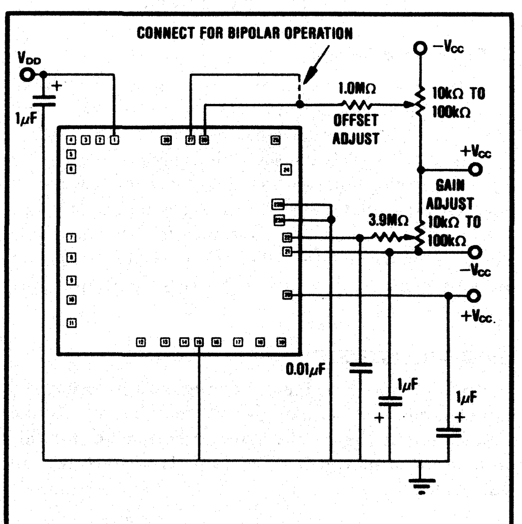


FIGURE 4. Power Supply, Gain, and Offset Potentiometer Connections.

The DAC811 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The Analog Common (pad 23) and Digital Common (pad 15) should be connected together at one point. Separate returns minimize current flow in low level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output, therefore, some caution is required in applying these common connections. The Analog Common is the high quality return for the D/A converter and should be connnected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 4. TCR of the potentiometers should be 100ppm/°C or less. The 1.0MΩ and 3.9MΩ resistors (20% tolerance or better) should be located close to the DAC811 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 5, may be substituted in each case. The Gain Adjust is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pickup in all applications, including those not employing external gain adjustment.

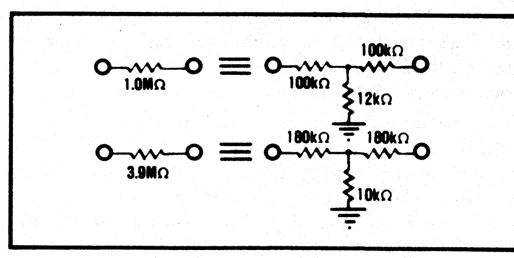


FIGURE 5. Equivalent Resistances.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC811 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 6. Connections for the output ranges are listed in Table III.

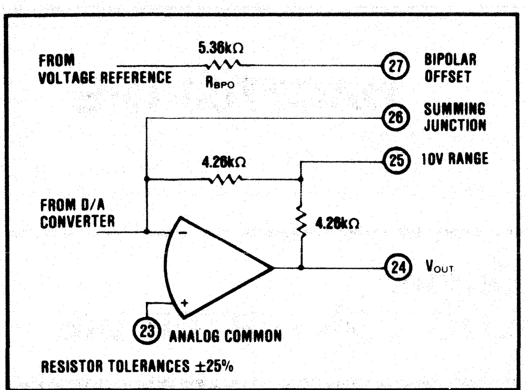


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

TABLE III. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 25 To	Connect Pin 27 To
0 to +10V	USB	24	23
±5V	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

BURR-BROWN®

DAC7700 DIE

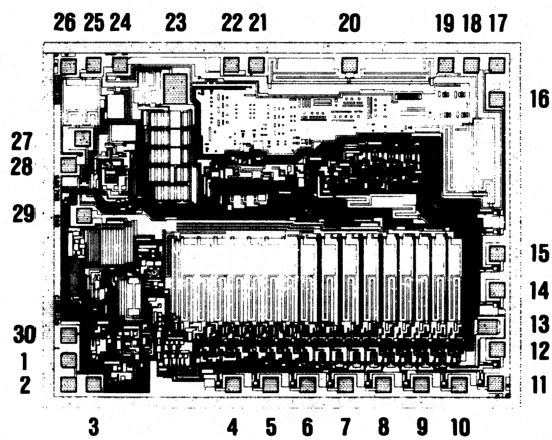
Current Output
16-BIT DIGITAL-TO-ANALOG CONVERTER DIE

DESCRIPTION

The DAC7700KD is complete 16-bit digital-to-analog converter that includes a precision buried-zener voltage reference on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.003% of full-scale range.

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to −2mA and ±1mA are available.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Bit 1 (MSB) Input	16	Bit 15 Input
2	Bit 2 Input	17	Bit 16 Input
3	Bit 3 Input	18	R_{FB} − 10kΩ
4	Bit 4 Input	19	No Connection
5	Bit 5 Input	20	R_{FB} − 10kΩ
6	Bit 6 Input	21	+5V Supply
7	Bit 7 Input	22	Digital Ground
8	Bit 8 Input	23	Analog Ground
9	Bit 9 Input	24	Current Output
10	Bit 10 Input	25	Bipolar Offset
11	Bit 11 Input	26	Gain Adjust
12	Bit 12 Input	27	+15V Supply
13	−15V Supply	28	Reference Output
14	Bit 13 Input	29	−15V Supply
15	Bit 14 Input	30	Zener test point. Do not use.

Die size: 153 × 120 mils
Bonding pad size: 4 × 4 mils
Backside contact: gold

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS [1]

At $T_A = +25°C$ and $\pm V_{CC} = 15V$, $V_{DD} = +5V$ unless otherwise noted.

MODEL	DAC7700KD			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
DIGITAL INPUT				
Resolution			16	Bits
Digital Inputs				
V_{IH}	+2.4		$+V_{CC}$	V
V_{IL}	−1.0		+0.8	V
I_{IH}, $V_I = +2.7V$			+40	μA
I_{IL}, $V_I = +0.4V$		−0.35	−0.5	mA
TRANSFER CHARACTERISTICS				
ACCURACY[2]				
Linearity Error[3]		±0.0015	±0.003	% of FSR[4]
Differential Linearity Error[3]		±0.003	±0.006	% of FSR
Gain Error[5]		±0.07	±0.15	%
Zero Error[5] [6]		+1	+2	μA
Monotonicity	14	15		Bits
OUTPUT				
Unipolar (CSB Code)[8]		0 to −2		mA
Output Impedance[8]		4		kΩ
Bipolar (COB Code)[8]		±1		mA
Output Impedance[8]		2.45		kΩ
Compliance Voltage		±2.5		V
REFERENCE VOLTAGE				
Voltage	+6.0	+6.3	+6.6	V
Source Current Available for External Loads		+2.5		mA
POWER SUPPLY REQUIREMENTS				
Voltage:				
$+V_{CC}$	11.4	15	16.5	V
$-V_{CC}$	11.4	15	16.5	V
V_{DD}	+4.5	+5	+16.5	V
Current (no load)				
$+V_{CC}$		+10	+25	mA
$-V_{CC}$		−13	−25	mA
V_{DD}			+8	mA
Power Dissipation ($V_{DD} = +5.0V$)[9]		365	790	mW
TEMPERATURE RANGE				
Specification:	0		70	°C

PERFORMANCE CHARACTERISTICS

Parameters included are for design information and are not guaranteed or subject to test.

PARAMETER	MIN	TYP	MAX	UNITS
DRIFT (over specification temperature range)				
Total Error Over Temperature Range (all models)[10]		±.08	±0.15	% of FSR
Total Full Scale Drift:				
Unipolar models		±10	±30	ppm of FSR/°C
Bipolar models		±10	±25	ppm of FSR/°C
Gain Drift (all models)		±10	±25	ppm/°C
Zero Drift:				
Unipolar models		±2.5	±5	ppm of FSR/°C
Bipolar models		±5	±12	ppm of FSR/°C
Differential Linearity Over Temp.[3]			+0.009, −0.006	% of FSR
Linearity Error Over Temp.[3]			±0.006	% of FSR

PERFORMANCE CHARACTERISTICS (CONT)

PARAMETER	MIN	TYP	MAX	UNITS
Reference Temperature Coefficient			25	ppm/°C
SETTLING TIME (to ±0.003% of FSR)[7] Full Scale Step (2mA),				
10 to 100Ω load		350	1000	nsec
1kΩ load		1	3	μsec

NOTES: (1) All dice are 100% probe tested and guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) DAC7700KD is specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) ±0.0015% of full-scale range is equivalent to 1LSB in 16-bit resolution. ±0.003% of full-scale range is equivalent to 1LSB in 15-bit resolution. ±0.006% of full-scale range is equivalent to 1LSB in 14-bit resolution. (4) FSR means full-scale range and is 20V for the ±10V range, 10V for the 0 to +10V range. FSR is 2mA for the ±1mA range and the 0 to +2mA range. (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the zero point. (6) Error at input code $FFFF_H$ for CSB operation, $7FFF_H$ for COB operation. (7) Maximum represents the 3σ limit. Not 100% tested for this parameter. (8) Tolerance on output impedance and output current is ±30%. (9) Power dissipation is an additional 40mW when V_{DD} is operated at +15V. (10) With gain and zero errors adjusted to zero at +25°C.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Common	0V, +18V
$-V_{CC}$ to Common	0V, −18V
V_{DD} to Common	0V, +18V
Digital Data Inputs to Common	−1V, +18V
Reference Out to Common	Indefinite Short to Common
External Voltage Applied to R_F	±18V
Power Dissipation	1000mW
Storage Temperature	−60°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGING

DAC7700 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B, and are shipped in sealed carriers.

ORDERING INFORMATION

DAC7700 K D

Basic Model Number — DAC7700

Grade/Temperature Range — K
K = 0°C to +70°C

Package Code — D
D = Die

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 1, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor may be needed from Gain Adjust to Common to reduce noise pickup. Refer to Figures 2 and 3 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.

Zero Adjustment

For unipolar (CSB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that produces zero output voltage or current. See Table I for corresponding codes and the Connection Diagram, Figure 4, for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

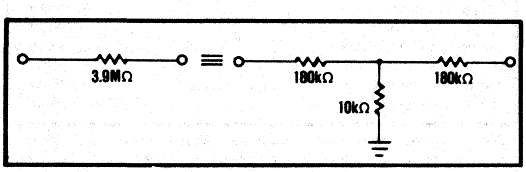


FIGURE 1. Equivalent Resistances.

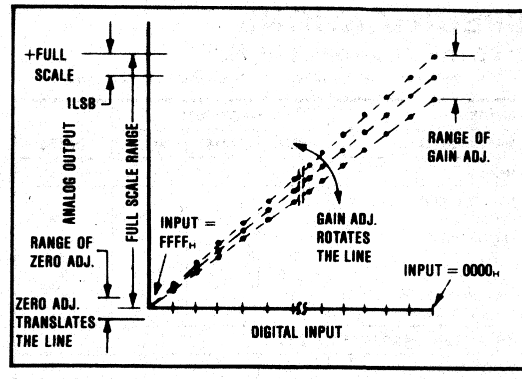


FIGURE 2. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters.

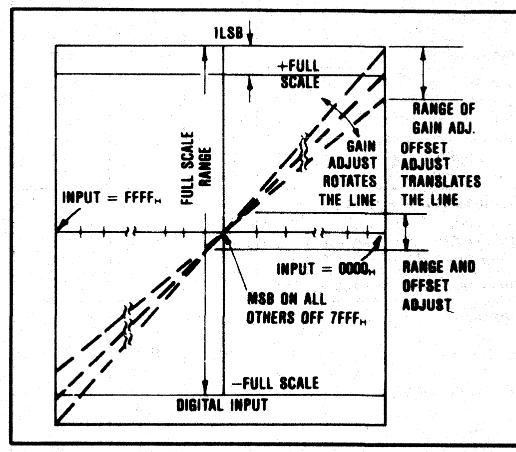


FIGURE 3. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters.

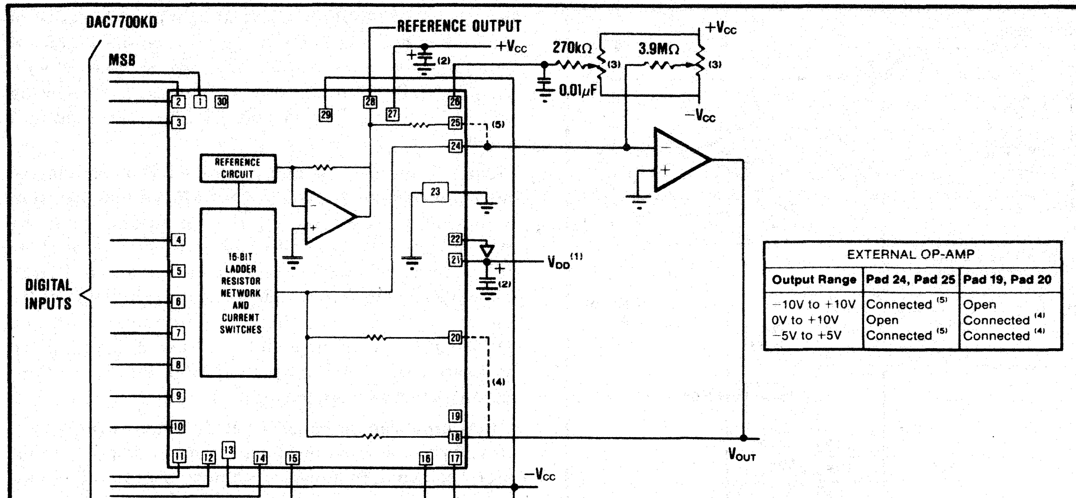
TABLE I. Digital Input and Analog Output Relationships.

CURRENT OUTPUT MODES

	Analog Output						
	Unipolar, 0 to −2mA			Bipolar, ±1mA			
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	Units
One LSB	0.031	0.061	0.122	0.031	0.061	0.122	μA
0000_H	−1.99997	−1.99994	−1.99988	−0.99997	−0.99994	−0.99988	mA
$FFFF_H$	0	0	0	+1.00000	+1.00000	+1.00000	mA
$7FFF_H$	−1.00000	−1.00000	−1.00000	0	0	0	mA

VOLTAGE OUTPUT MODES (WITH EXTERNAL OP-AMP)

	Analog Output									
	Unipolar, 0 to +10V			Bipolar, ±10V			Bipolar, ±5V			
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	Units
One LSB	153	305	610	305	610	1224	153	305	610	μV
0000_H	+9.99985	+9.99969	+9.99939	+9.99969	+9.99939	+9.99878	+4.99985	+4.99969	+4.99939	V
$FFFF_H$	0	0	0	−10.0000	−10.0000	−10.0000	−5.0000	−5.0000	−5.0000	V
$7FFF_H$	+5.00000	+5.00000	+5.00000	0	0	0	0	0	0	V



EXTERNAL OP-AMP		
Output Range	**Pad 24, Pad 25**	**Pad 19, Pad 20**
−10V to +10V	Connected (5)	Open
0V to +10V	Open	Connected (4)
−5V to +5V	Connected (5)	Connected (4)

NOTES: (1) Can be tied to $+V_{CC}$ instead of having separate V_{DD} supply; this will increase power dissipation approximately 100mW. (2) Decoupling capacitors are 0.1μF to 1μF. (3) Potentiometers are 10kΩ to 100kΩ. (4) Make this connection for 10V full-scale range. Leave open for 20V full-scale range. (5) Make this connection for bipolar operation. Leave open for unipolar operation.

FIGURE 4. Connection Diagram.

Gain Adjustment

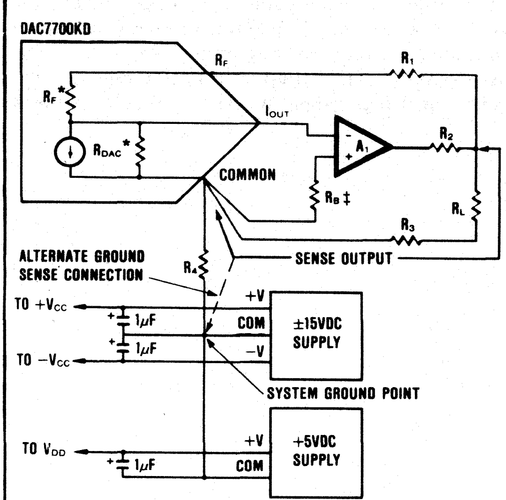
Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table 1 for positive full scale voltages and Figure 4 for gain adjustment circuit connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter connected for a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

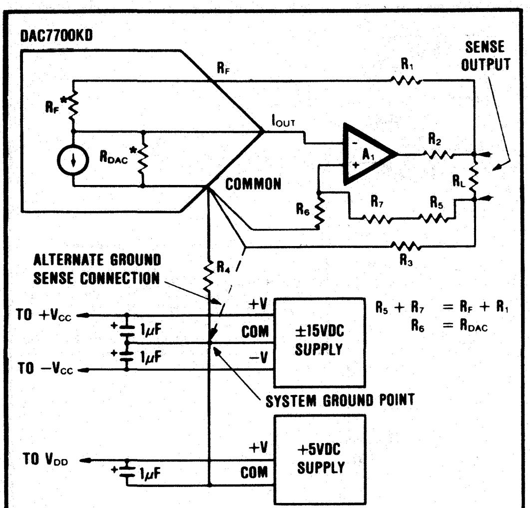
In Figures 5 and 6, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located



*	RB	RF	RDAC
Bipolar	2.45kΩ	10kΩ	2.45kΩ
Unipolar	4.0kΩ	5kΩ	4kΩ

‡ R_B should be equal to the output impedance at the current output to compensate for the bias current drift of A_1. Use standard 10%, 1/4W carbon composition or equivalent resistors.

FIGURE 5. Preferred External Op Amp Configuration.



*

	R_F	R_{DAC}
Bipolar	10kΩ	2.45kΩ
Unipolar	5kΩ	4kΩ

FIGURE 6. Differential Sensing Output Op Amp Configuration.

as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the common pad. Sensing the output voltage at the system ground point is permissible with the DAC7700 because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20µA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times$ 2mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 5 and 6.

Figures 5 and 6 show two methods of connecting the current output model DAC7700 with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

If the output cannot be sensed at Common or the system ground point as mentioned above, the differential output circuit shown in Figure 6 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 6 can be reduced to the one shown in Figure 5. Again the effect of R_4 is negligible.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

BURR-BROWN®

DAC7701 DIE

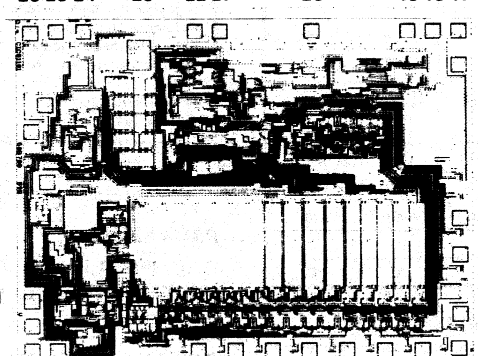
Voltage Output
16-BIT DIGITAL-TO-ANALOG CONVERTER DIE

DESCRIPTION

The DAC7701KD is a complete 16-bit digital-to-analog converter that includes a precision buried-zener voltage reference and a low-noise, fast-settling output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.003% of full-scale range.

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V and ±10V are available.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Bit 1 (MSB) Input	16	Bit 15 Input
2	Bit 2 Input	17	Bit 16 Input
3	Bit 3 Input	18	R_{FB} – 10kΩ
4	Bit 4 Input	19	Voltage Output
5	Bit 5 Input	20	R_{FB} – 10kΩ
6	Bit 6 Input	21	+5V Supply
7	Bit 7 Input	22	Digital Ground
8	Bit 8 Input	23	Analog Ground
9	Bit 9 Input	24	Current Output
10	Bit 10 Input	25	Bipolar Offset
11	Bit 11 Input	26	Gain Adjust
12	Bit 12 Input	27	+15V Supply
13	−15V Supply	28	Reference Output
14	Bit 13 Input	29	−15V Supply
15	Bit 14 Input	30	Zener test point. Do not use.

Die size: 153 × 120 mils
Bonding pad size: 4 × 4 mils
Backside contact: gold

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS

At $T_A = +25°C$ and $\pm V_{CC} = 15V$, $V_{DD} = +5V$ unless otherwise noted.

MODEL	DAC7701KD			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
DIGITAL INPUT				
Resolution			16	Bits
Digital Inputs				
V_{IH}	+2.4		$+V_{CC}$	V
V_{IL}	−1.0		+0.8	V
I_{IH}, $V_I = +2.7V$			+40	µA
I_{IL}, $V_I = +0.4V$		−0.35	−0.5	mA
TRANSFER CHARACTERISTICS				
ACCURACY				
Linearity Error[2]		±0.0015	±0.003	% of FSR[3]
Differential Linearity Error[2]		±0.003	±0.006	% of FSR
Gain Error[4]		±0.07	±0.15	%
Zero Error[3] [5]		±10	±20	mV
Monotonicity	14	15		Bits
OUTPUT				
Unipolar (CSB Code)		0 to +10		V
Bipolar (COB Code)		±10		V
Output Current		±5		mA
Output Impedance		0.15		Ω
Short Circuit to Common Duration		Indefinite		
REFERENCE VOLTAGE				
Voltage	+6.0	+6.3	+6.6	V
Source Current Available for External Loads		+2.5		mA
POWER SUPPLY REQUIREMENTS				
Voltage:				
$+V_{CC}$	11.4	15	16.5	V
$-V_{CC}$	11.4	15	16.5	V
V_{DD}	+4.5	+5	+16.5	V
Current (no load)				
$+V_{CC}$		+16	+30	mA
$-V_{CC}$		−18	−30	mA
V_{DD}		+4	+8	mA
Power Dissipation ($V_{DD} = +5.0V$)[8]		530	940	mW
TEMPERATURE RANGE				
Specification:	0		70	°C

PERFORMANCE CHARACTERISTICS

Parameters included are for design information and are not guaranteed or subject to test.

PARAMETER	MIN	TYP	MAX	UNITS
DRIFT (over specification temperature range)				
Total Error Over Temperature Range (all models)[9]		±.08	±0.15	% of FSR
Total Full Scale Drift:				
Unipolar models		±10	±30	ppm of FSR/°C
Bipolar models		±10	±25	ppm of FSR/°C
Gain Drift (all models)		±10	±25	ppm/°C
Zero Drift:				
Unipolar models		±2.5	±5	ppm of FSR/°C
Bipolar models		±5	±12	ppm of FSR/°C
Differential Linearity Over Temp.[2]			+0.009, −0.006	% of FSR

PERFORMANCE CHARACTERISTICS (CONT)

PARAMETER	MIN	TYP	MAX	UNITS
Linearity Error Over Temp.[2]			±0.006	% of FSR
Reference Temperature Coefficient			25	ppm/°C
SETTLING TIME (to ±0.003% of FSR)[6]				
Full Scale Step 2kΩ load		4	8	µsec
1LSB Step at Worst-Case Code[7]		2.5		µsec
Slew Rate		10		V/µsec

NOTES: (1) All dice are 100% probe tested and guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) ±0.0015% of full-scale range is equivalent to 1LSB in 16-bit resolution. ±0.003% of full-scale range is equivalent to 1LSB in 15-bit resolution. ±0.006% of full-scale range is equivalent to 1LSB in 14-bit resolution. (3) FSR means full-scale range and is 20V for the ±10V range, 10V for the 0 to +10V range. FSR is 2mA for the ±1mA range and the 0 to +2mA range. (4) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the zero point. (5) Error at input code $FFFF_H$ for CSB operation, $7FFF_H$ for COB operation. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$. (8) Power dissipation is an additional 40mW when V_{DD} is operated at +15V. (9) With gain and zero errors adjusted to zero at +25°C.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Common	0V, +18V
$-V_{CC}$ to Common	0V, −18V
V_{DD} to Common	0V, +18V
Digital Data Inputs to Common	−1V, +18V
Reference Out to Common	Indefinite Short to Common
External Voltage Applied to R_F	±18V
External Voltage Applied to D/A Output	−5V to +5V
V_{OUT}	Indefinite Short to Common
Power Dissipation	1000mW
Storage Temperature	−60°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGING

DAC7701KD dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B, and are shipped in sealed carriers.

ORDERING INFORMATION

DAC7701 K D

Basic Model Number

Grade/Temperature Range
K = 0°C to +70°C

Package Code
D = Die

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 1, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor may be needed from Gain Adjust to Common to reduce noise pickup. Refer to Figures 2 and 3 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.

Zero Adjustment

For unipolar (CSB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that produces zero output voltage or current. See Table I for corresponding codes and the Connection Diagram, Figure 4, for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

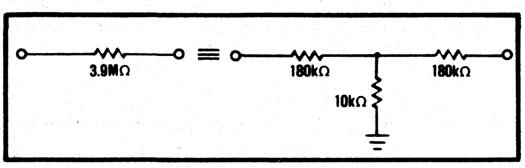


FIGURE 1. Equivalent Resistances.

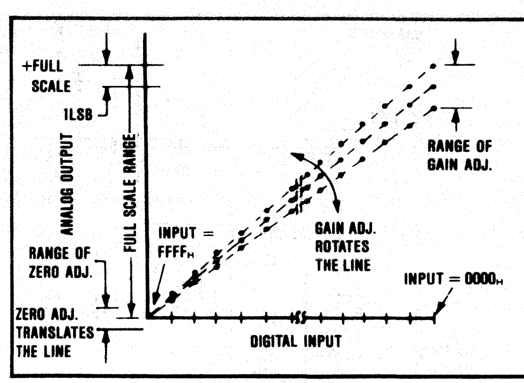


FIGURE 2. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters.

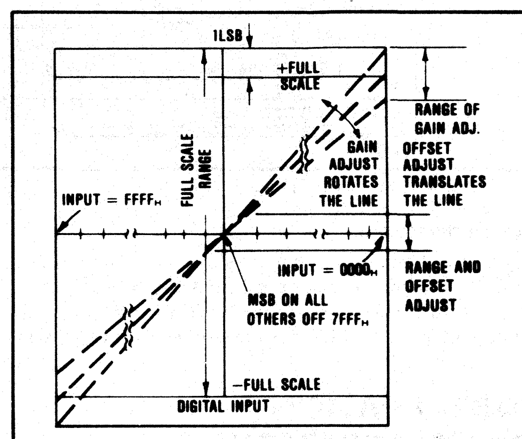
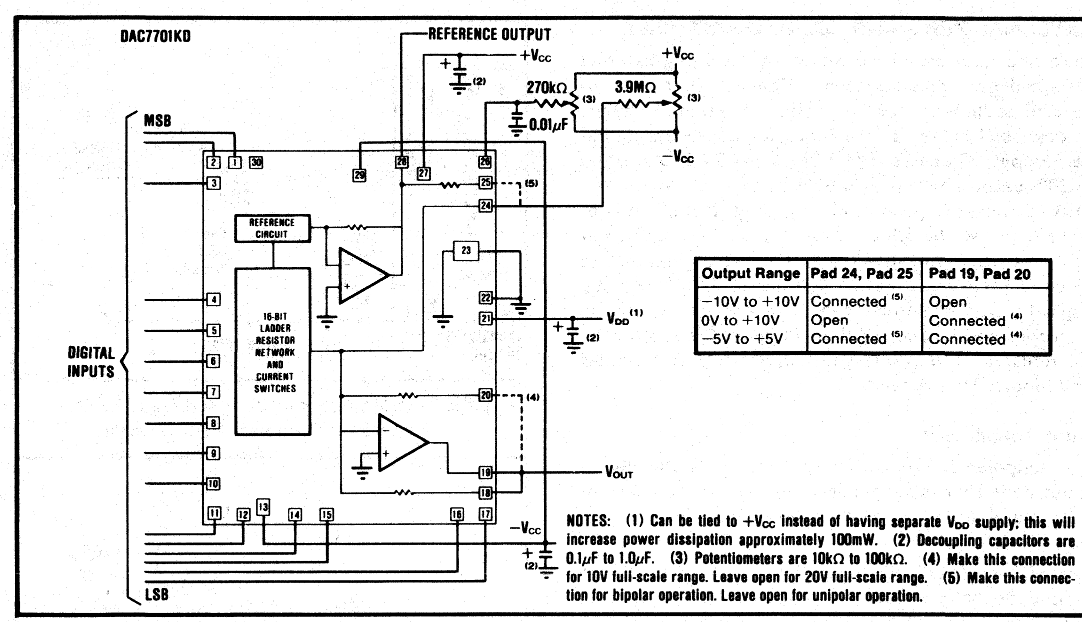


FIGURE 3. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters.

TABLE I. Digital Input and Analog Output Relationships.

VOLTAGE OUTPUT MODES										
	Analog Output									
Digital Input Code	Unipolar, 0 to +10V			Bipolar, ±10V			Bipolar, ±5V			Units
	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	
One LSB	153	305	610	305	610	1224	153	305	610	μV
0000$_H$	+9.99985	+9.99969	+9.99939	+9.99969	+9.99939	+9.99878	+4.99985	+4.99969	+4.99939	V
FFFF$_H$	0	0	0	−10.0000	−10.0000	−10.0000	−5.0000	−5.0000	−5.0000	V
7FFF$_H$	+5.00000	+5.00000	+5.00000	0	0	0	0	0	0	V



Output Range	Pad 24, Pad 25	Pad 19, Pad 20
−10V to +10V	Connected [5]	Open
0V to +10V	Open	Connected [4]
−5V to +5V	Connected [5]	Connected [4]

NOTES: (1) Can be tied to $+V_{CC}$ instead of having separate V_{DD} supply; this will increase power dissipation approximately 100mW. (2) Decoupling capacitors are 0.1μF to 1.0μF. (3) Potentiometers are 10kΩ to 100kΩ. (4) Make this connection for 10V full-scale range. Leave open for 20V full-scale range. (5) Make this connection for bipolar operation. Leave open for unipolar operation.

FIGURE 4. Connection Diagram.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table I for positive full scale voltages and Figure 4 for gain adjustment circuit connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter connected for a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figure 5, lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed during initial calibration. R_2 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_1 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_1 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_3 is negligible.

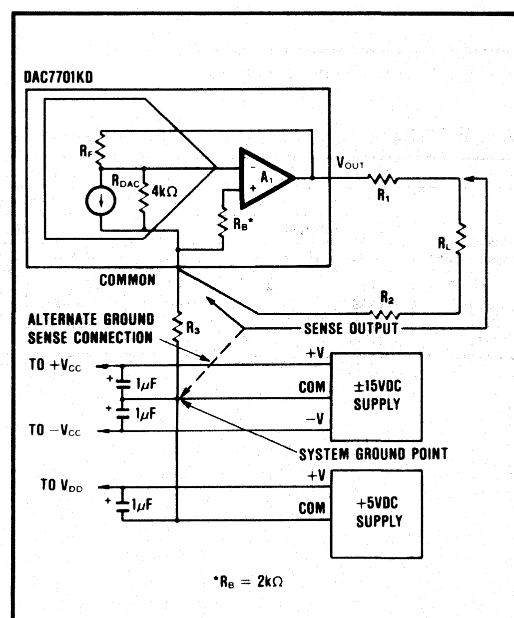


FIGURE 5. Output Circuit for Voltage Models.

In many applications it is impractical to sense the output voltage at the common pad. Sensing the output voltage at the system ground point is permissible with the DAC7701 because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_3 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_3 ($R_3 \times$ 2mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figure 5.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

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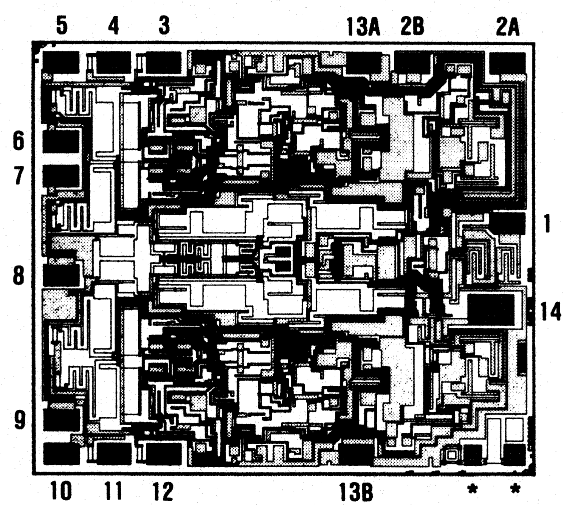
INA101 DIE

Very-High Accuracy
INSTRUMENTATION AMPLIFIER DIE

DESCRIPTION

The INA101 is a high accuracy, monolithic instrumentation amplifier. It consists of three precision operational amplifiers featuring a laser-trimmed thin-film resistor network. High input impedance, low noise, very-low drift, and high accuracy give outstanding performance in demanding instrumentation applications.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Output	8	A_1 Output
2A	$+V_{CC}$	9	A_2 Output
2B	$+V_{CC}$	10	Gain Set A_2
3	−Input	11	Gain Sense A_2
4	Gain Sense A_1	12	+Input
5	Gain Set A_1	13A	$-V_{CC}$
6	V_{OS} Trim A_1	13B	$-V_{CC}$
7	V_{OS} Trim A_1	14	Common

Die Size: 120 × 106 mils

Bonding Pad Size: 5 × 5 mils

Backside Contact: Gold

*Do Not Connect

NOTES: (1) The back of the die should not be used for the $-V_{CC}$ connection. (2) Bond from either pad 13A or pad 13B to $-V_{CC}$. (3) Bond from pad 2A and pad 2B separately to $+V_{CC}$.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At $T_{DIE} = +45°C$ and $\pm V_{CC} = 15V$ unless otherwise specified.[2]

PARAMETER	CONDITIONS	INA101AD MIN	TYP	MAX	UNITS
GAIN EQUATION	Gain = 1 + (40k/R_G)				
GAIN ERROR	Gain = 1			±0.1	% of FS
	Gain = 10			±0.2	% of FS
	Gain = 100			±0.25	% of FS
	Gain = 1000			±0.5	% of FS
RATED OUTPUT					
Voltage		±10			V
Current	$V_O = \pm 10V$	±5			mA
OFFSET					
Input Stage	G = 1000			±100	µV
vs Temperature	G = 1000			±4	µV/°C
vs Supply (PSR)	G = 1	90			dB
Output Stage				±600	µV
vs Temperature				±30	µV/°C
INPUT BIAS CURRENT				±30	nA
COMMON-MODE REJECTION	$V_{IN} = \pm 10VDC$				
	G = 1 DC	76			dB
	G = 1000	100			dB
POWER SUPPLY					
Voltage	Derated	±5		±18	V
Current	$I_O = 0mADC$			±8.5	mA

NOTES: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) +45°C is used to simulate die temperature of an assembled part at ambient temperature of +25°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$\pm V_{CC}$
Differential Input Voltage	$\pm V_{CC}$
Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Continuous
Junction Temperature	+150°C

PACKAGING

INA101 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

ORDERING INFORMATION

INA101 A D

Basic model number — INA101

Grade/temperature range — A
A = −25°C to +85°C

Package code — D
D = Die

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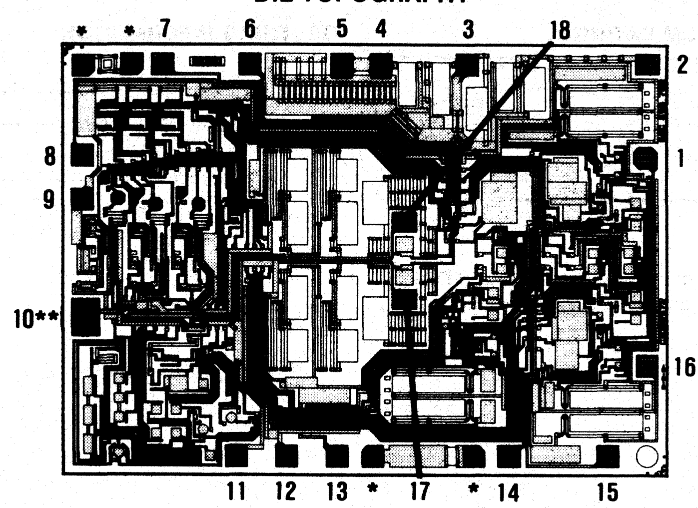
INA102 DIE

Low Power High Accuracy INSTRUMENTATION AMPLIFIER DIE

DESCRIPTION

The INA102 is a high accuracy, monolithic instrumentation amplifier designed for signal conditioning applications where low quiescent power is desired. On-chip laser-trimmed thin-film resistors provide excellent gain/temperature stability and excellent CMRR. Gains of 1, 10, 100, or 1000 may be conveniently selected by strapping appropriate pads together.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Offset Adjust	10	Common
2	× 10	11	Output
3	× 100	12	$+V_{CC}$
4	× 1000	13	Filter
5	× 1000 Gain Sense	14	−In
6	Gain Sense	15	+In
7	Gain Set	16	Offset Adjust
8	CMR Trim	17	A_1 Output
9	$-V_{CC}$	18	A_2 Output

Die Size: 142 × 104 mils

Bonding Pad Size: 5 × 5 mils

Backside Contact: Gold

*Do Not Connect

**Glass covers the lower 1/3 of this pad.

NOTE: The back of the die should not be used for the $-V_{CC}$ connection.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At $T_{DIE} = +25°C$ $\pm V_{CC} = 15V$ unless otherwise specified.

		INA102AD			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
GAIN EQUATION[2]	Externally Set		$1 + (40k/R_G)$		V/V
PAD-STRAPPABLE GAINS			$\times$ 1, 10, 100, 1000		V/V
GAIN ERROR[2]	Gain = 1 = 10 = 100 = 1000			±0.1 ±0.1 ±0.25 ±0.75	% of FS % of FS % of FS % of FS
RATED OUTPUT Voltage Current	 $V_O = 10V$	 ±10 ±1			 V mA
OFFSET Input Stage Output Stage	 G = 1000			 ±300 ±400	 μV μV
INPUT BIAS CURRENT				50	nA
COMMON MODE REJECTION	$V_{IN} = \pm 10VDC$ G = 1 G = 1000	 74 80			 dB dB
POWER SUPPLY Voltage Current	 Derated $I_O = 0mADC$	 ±3.5		 ±18 ±750	 V μA

NOTES: (1) All dice are 100% probe-tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) If an external gain set resistor (R_G) is used for intermediate gains, it can be a major source of gain error. Gain error specifications are for pin-strapped gains only.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range, Differential & Common-mode	$\pm V_{CC}$
Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Continuous
Junction Temperature	+150°C

PACKAGING

INA102 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

ORDERING INFORMATION

INA102 A D

Basic model number — INA102

Grade/temperature range — A
A = −25°C to +85°C

Package code — D
D = Die

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OPA27 DIE

Ultra-Low Noise Precision OPERATIONAL AMPLIFIER DIE

DESCRIPTION

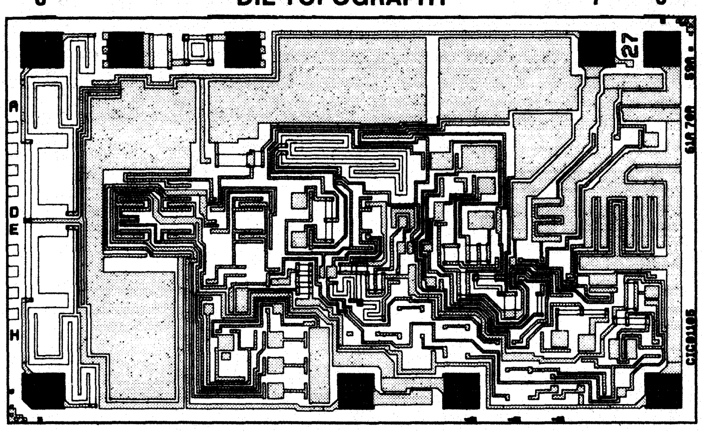
The OPA27 is an ultra-low noise, high precision operational amplifier. It is an improved replacement for the industry-standard OP-27.

Laser-trimmed thin-film resistors provide excellent long-term stability and allow superior offset voltage compared to common zener-zap trim techniques.

A unique bias current cancellation circuit (patent pending) allows bias and offset current specifications to be met over the full −55°C to +125°C temperature range.

DIE TOPOGRAPHY

8 7 6



1 2 3 4

Pad	Function
1	Offset Trim
2	Inverting Input
3	Noninverting Input
4	Negative Supply and Substrate

Pad	Function
5	None
6	Output
7	Positive Supply
8	Offset Trim

Die Size: 99 × 61 mils

Bonding Pad Size: 5 × 5 mils

Backside Contact: Gold

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +25°C and $\pm V_{CC}$ = 15V unless otherwise specified.

PARAMETER	CONDITIONS	OPA27CD/OPA27GD MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage				±60	µV
Average Drift			±0.3		µV/°C
Supply Rejection	$\pm V_{CC}$ = 4V to 18V	95			dB
				18	µV/V
BIAS CURRENT					
Input Bias Current				±80	nA
Input Offset Current				75	nA
VOLTAGE RANGE					
Common-Mode Input Range			±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	100			dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	118			dB
RATED OUTPUT					
Voltage Output	$R_L \geq 2k\Omega$	±11.5			V
	$R_L \geq 600\Omega$	±10.0			V
Short-Circuit Current		±17		±60	mA
POWER SUPPLY					
Current, Quiescent	I_O = 0mADC			±5.7	mA

NOTE: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22VDC
Input Voltage[1]	±22VDC
Differential Input Voltage[2]	±0.7VDC
Differential Input Current[2]	±25mA
Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration	Continuous
Junction Temperature	+150°C

(1) For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage. (2) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

PACKAGING

OPA27 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

ORDERING INFORMATION

OPA27 X D

Basic model number

Grade/temperature range
C = −55°C to +125°C
G = −25°C to +85°C

Package code
D = die

BURR-BROWN®

OPA37 DIE

Ultra-Low Noise Precision OPERATIONAL AMPLIFIER DIE

DESCRIPTION

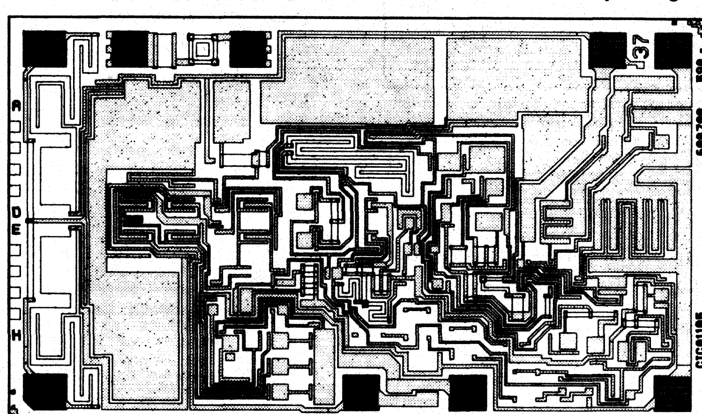
The OPA37 is an ultra-low noise, high precision operational amplifier. It is an improved replacement for the industry-standard OP-37.

Laser-trimmed thin-film resistors provide excellent long term stability and allow superior offset voltage compared to common zener-zap trim techniques.

A unique bias current cancellation circuit (patent pending) allows bias and offset current specifications to be met over the full −55°C to +125°C temperature range.

The uncompensated OPA37 requires a gain ≥5 for loop stability.

8 **DIE TOPOGRAPHY** 7 6



1 2 3 4

Pad	Function	Pad	Function
1	Offset Trim	5	None
2	Inverting Input	6	Output
3	Noninverting Input	7	Positive Supply
4	Negative Supply and Substrate	8	Offset Trim

Die Size: 99 × 61 mils

Bonding Pad Size: 5 × 5 mils

Backside Contact: Gold

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At $T_{DIE} = +25°C$ and $\pm V_{CC} = 15V$ unless otherwise specified.

PARAMETER	CONDITIONS	OPA37CD/OPA37GD MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage				±60	µV
Average Drift			±0.3		µV/°C
Supply Rejection	$\pm V_{CC} = 4V$ to 18V	95			dB
				18	µV/V
BIAS CURRENT					
Input Bias Current				±80	nA
Input Offset Current				75	nA
VOLTAGE RANGE					
Common-Mode Input Range			±11		V
Common-Mode Rejection	$V_{IN} = \pm 10VDC$	100			dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	118			dB
RATED OUTPUT					
Voltage Output	$R_L \geq 2k\Omega$	±11.5			V
	$R_L \geq 600\Omega$	±10.0			V
Short-Circuit Current		±17		±60	mA
POWER SUPPLY					
Current, Quiescent	$I_O = 0mADC$			±5.7	mA

NOTE: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22VDC
Differential Input Voltage[1]	±0.7VDC
Differential Input Current[1]	±25mA
Input Voltage Range[2]	±22VDC
Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration	Continuous
Junction Temperature	+150°C

(1) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
(2) For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

PACKAGING

OPA37 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

ORDERING INFORMATION

OPA37 X D

Basic model number — OPA37

Grade/temperature range — X
C = −55°C to +125°C
G = −25°C to +85°C

Package code — D
D = die

BURR-BROWN®

OPA111 DIE

Precision Dielectrically-Isolated FET *Difet*™ OPERATIONAL AMPLIFIER DIE

DESCRIPTION

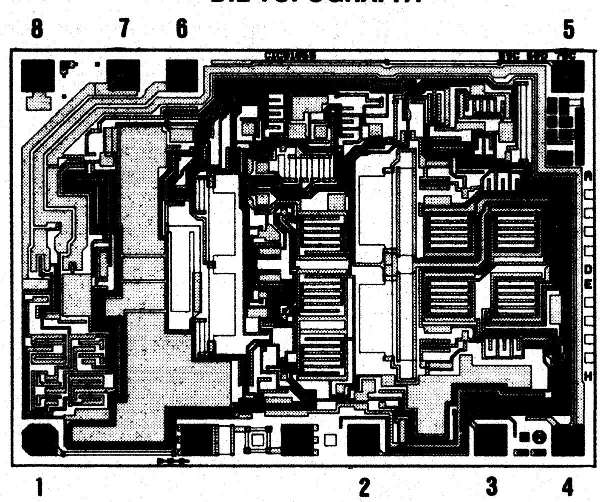
The OPA111 is a precision monolithic dielectrically-isolated FET (*Difet*™) operational amplifier.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser-trimming of thin film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patent pending). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Offset Trim	5	Offset Trim
2	Inverting Input	6	Output
3	Noninverting Input	7	Positive Supply
4	Negative Supply	8	Substrate*

Die Size: 96 × 71 mils
Bonding Pad Size: 5 × 5 mils
Backside Contact: Gold

*This dielectrically-isolated substrate is normally connected to common.

Difet™ Burr-Brown Corp. BIFET® National Semiconductor Corp.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At $T_{DIE} = +25°C$ and $\pm V_{CC} = 15V$ unless otherwise specified. Pad 8 connected to common.

PARAMETER	CONDITIONS	OPA111AD MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage	$V_{CM} = 0VDC$			±500	µV
Average Drift	$T_{DIE} = +25°C$ to $+85°C$			±15	µV/°C
Supply Rejection	$\pm V_{CC} = 5V$ to $15V$	86			dB
				50	µV/V
BIAS CURRENT					
Input Bias Current	$V_{CM} = 0VDC$				
	$T_{DIE} = +85°C$			±750	pA
	$T_{DIE} = +25°C$		±0.8		pA
VOLTAGE RANGE					
Common-Mode Input Range		±10			V
Common-Mode Rejection	$V_{IN} = \pm 10VDC$	86			dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	105			dB
RATED OUTPUT					
Voltage Output	$R_L = 2k\Omega$	±10			V
Short-Circuit Current		±10		±60	mA
POWER SUPPLY					
Current, Quiescent	$I_O = 0mADC$			±4.5	mA

NOTE: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18VDC
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration	Continuous
Junction Temperature	+175°C

PACKAGING

OPA111 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

ORDERING INFORMATION

OPA111 A D

Basic model number

Grade/temperature range
A = −25°C to +85°C

Package code
D = die

BURR-BROWN®

OPA2111 DIE

Precision Dielectrically-Isolated FET *Difet*™ DUAL OPERATIONAL AMPLIFIER DIE

DESCRIPTION

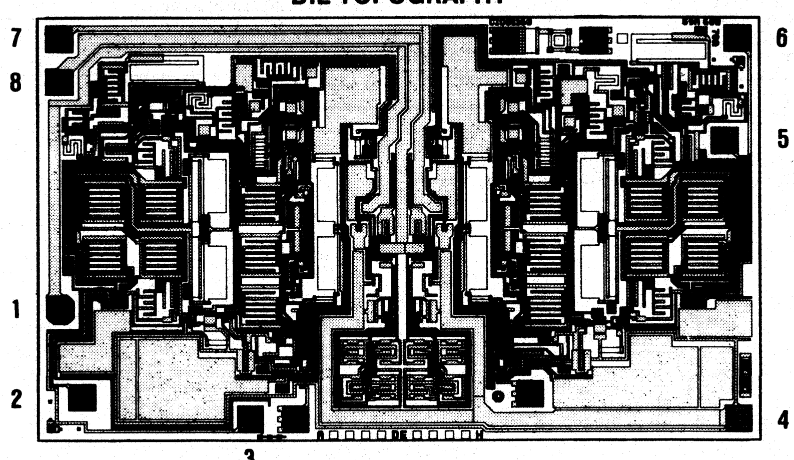
The OPA2111 is a precision dual monolithic dielectrically-isolated FET (*Difet*™) operational amplifier.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser-trimming of thin film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patent pending). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Output A	5	Noninverting Input B
2	Inverting Input A	6	Inverting Input B
3	Noninverting Input A	7	Output B
4	Negative Supply	8	Positive Supply

Die Size: 138 × 84 mils

Bonding Pad Size: 5 × 5 mils

Backside Contact: Gold

NOTE: This dielectrically-isolated substrate is normally connected to positive supply or left floating.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +25°C and $\pm V_{CC}$ = 15V unless otherwise specified.

PARAMETER	CONDITIONS	OPA2111AD MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage	V_{CM} = 0VDC			±500	μV
Average Drift	T_{DIE} = +25°C to +85°C			±15	μV/°C
Supply Rejection	$\pm V_{CC}$ = 10V to 18V	84			dB
				63	μV/V
BIAS CURRENT					
Input Bias Current	V_{CM} = 0VDC				
	T_{DIE} = +85°C			±1	nA
	T_{DIE} = +25°C		±2		pA
VOLTAGE RANGE					
Common-Mode Input Range		±10			V
Common-Mode Rejection	V_{IN} = ±10VDC	88			dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	105			dB
RATED OUTPUT					
Voltage Output	$R_L = 2k\Omega$	±10			V
Short-Circuit Current		±10		±60	mA
POWER SUPPLY					
Current, Quiescent	I_O = 0mADC			±9	mA

NOTE: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18VDC
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration	Continuous
Junction Temperature	+175°C

PACKAGING

OPA2111 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

ORDERING INFORMATION

OPA2111 A D

Basic model number — OPA2111

Grade/temperature range — A
A = −25°C to +85°C

Package code — D
D = die

BURR-BROWN®

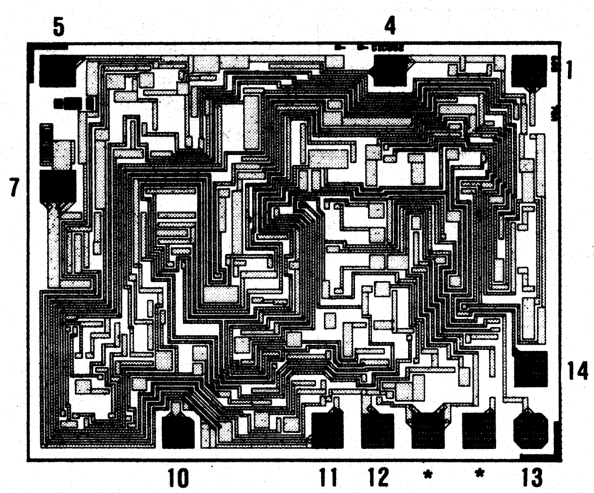
VFC32 DIE

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER DIE

DESCRIPTION

The VFC32 is a monolithic voltage-to-frequency converter circuit including precision input integrator op amp, comparator, one-shot, and switched current source. It is capable of accurate voltage-to-frequency and frequency-to-voltage conversion at frequencies to 500kHz.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Inverting Integrator Input	11	Common
4	$-V_{CC}$	12	$+V_{CC}$
5	One-shot Capacitor	13	V_{OUT}
7	f_{OUT}	14	Noninverting Integrator Input
10	Comparator Input	*	DO NOT CONNECT

Die Size: 89 × 72 mils (2.26 × 1.83mm)

Bonding Pad Size: 5 × 5 mils (0.127 × 0.127mm)

Backside Contact: Gold

NOTE: The junction-isolated substrate is connected to $-V_{CC}$. Any electrical connection to the back side must be returned to the die's $-V_{CC}$ connection.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +25°C and $\pm V_{CC}$ = 15V unless otherwise noted.

PARAMETER	CONDITIONS	VFC32BD MIN	TYP	MAX	UNITS
V/F TRANSFER FUNCTION					
Input Range		0		0.25	mA
Gain Error	f = 10kHz		5		%
Nonlinearity	f = 10 kHz		0.005		%
Gain Drift	f = 10 kHz		50		ppm/°C
Maximum Operating Frequency				500	kHz
INTEGRATOR AMPLIFIER					
V_{OS}			1	4	mV
V_{OS} Drift			5		µV/C
I_B Inverting Input			20	100	nA
Noninverting Input			100	250	nA
CM Range		−10		0	V
V_{OUT} Range		0		10	V
OPEN COLLECTOR OUTPUT					
V_{OL}	I_{OUT} = 8mA		0.2	0.4	V
I_{OH}, (off leakage)			0.01	2	µA
POWER SUPPLY					
Operating Range		±11		±20	V
Quiescent Current			5.5	6.5	mA

NOTE: (1) All dice are 100% probe tested to the above specification limits. Due to possible wafer saw and assembly shifts, parameters are not guaranteed for assembled units.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±22V
F_{OUT} Currrent Sink	50mA
Output Current, V_{OUT}	20mA
Input Voltage, ±In	$\pm V_{CC}$
Comparator Input	$\pm V_{CC}$
Temperature Range, Storage	−65°C to 150°C

PACKAGING

Die are visually inspected to MIL-STD-883, method 2010, Test condition B. and are shipped in sealed carriers.

ORDERING INFORMATION

VFC32 B D

Basic model number — VFC32

Grade/temperature range — B
B = −25°C to +85°C

Package code — D
D = Die

BURR-BROWN®

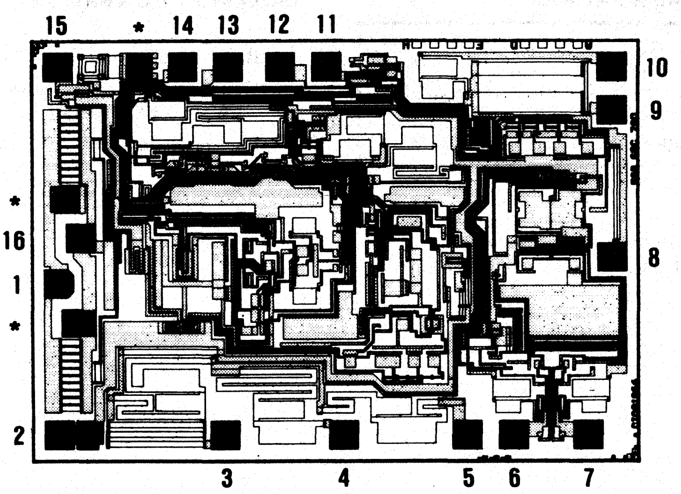
XTR110 DIE

Precision VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER DIE

DESCRIPTION

The XTR110 is a precision monolithic voltage-to-current converter. It can convert standard 0V to +10V or 0V to +5V inputs into 4mA to 20mA, or 5mA to 25mA outputs. The required external MOS transistor keeps heat outside the die to optimize performance under all output conditions. The XTR110 features a precision +10V reference output. The XTR110 can be used as a current-mode transmitter or a programmable current source.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Source Resistor	9	16mA Span
2	Common	10	4mA Span
3	V_{REF} In	11	V_{REF} Adjust
4	$V_{IN\ 1}$ (10V)	12	V_{REF} Sense
5	$V_{IN\ 2}$ (5V)	13	Source Sense
6	Offset Adjust	14	Gate Drive
7	Offset Adjust	15	V_{REF} Force
8	Span Adjust	16	$+V_{CC}$

Die Size: 109 × 78 mils

Bonding Pad Size: 5 × 5 mils

Backside Contact: Gold

*Do Not Connect

NOTE: The back of the die should not be used for the common connection.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At $T_{DIE} = +25°C$ and $+V_{CC} = 24V$ and $R_L = 250\Omega$ unless otherwise specified.

		XTR110AD			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSFER FUNCTION	$I_O = 10[(V_{REF}\ IN/16) + (V_{IN\,1}/4) + V_{IN\,2}/2)]/R_{SPAN}$				
INPUT RANGE $V_{IN\,1}$ $V_{IN\,2}$	I_O = Specified Range	 0 0		 +10 +5	 V V
OUTPUT CURRENT	(2)	4		20	mA
OFFSET CURRENT ERROR	(2) (3) $I_O = 4mA$			±0.4	% of Span
SPAN ERROR[4]	(2)(3) $I_O = 20mA$			±0.6	% of Span
NONLINEARITY	$4mA \leq I_O \leq 20mA$		±0.005	±0.025	% of Span
VOLTAGE REFERENCE Output Voltage Output Current[5]	 No Load	 +9.95 +10	 +10	 +10.05	 V mA
Power Supply Voltage Current	 Excluding I_O	 +13.5		 +40 +4.5	 V mA

NOTES: (1) All die are 100% probe tested at wafer level and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) Including internal reference. External transistor is required. (3) Offset current and span error are strong functions of wire bond resistance and package internal interconnect resistance. The die have been trimmed for optimum results when 1-mil aluminum wire is used in a 16-pin side brazed package or equivalent. Consult Burr-Brown for recommended layout. (4) Span is the change in output current resulting from a full scale change in input voltage. (5) Reference current drive can be extended by using an external NPN transistor.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +40V
Input Voltage Range .... $+V_{CC}$
Storage Temperature Range .... −65°C to +150°C
Output Short-Circuit Duration Gate
Drive and V_{REF} Force .... Continuous to common and $+V_{CC}$
Output Current Using Internal 50Ω resistor 40mA
Junction Temperature .... +150°C

ORDERING INFORMATION

XTR110 A D

Basic model number — XTR110
Grade/temperature range — A
A = −25°C to +85°C
Package code — D
D = Die

PACKAGING

XTR110 die are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

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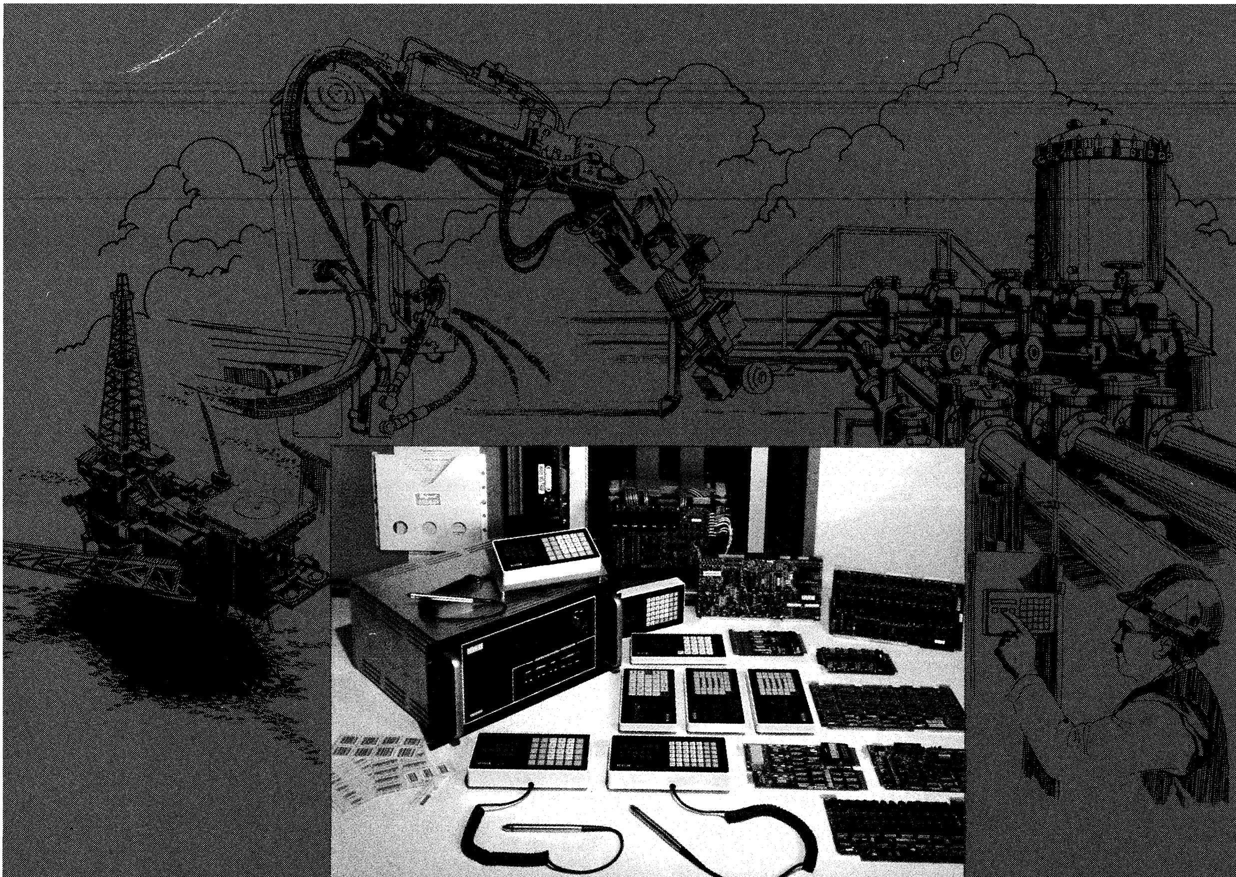

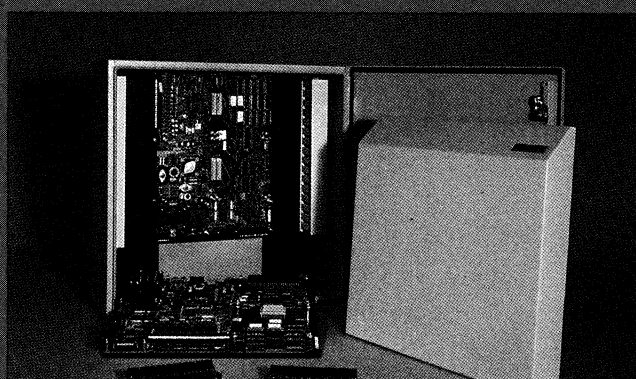

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